

Alpha PCI 164–266/300

User's Manual

Order Number: EK–AL266-UM. A01

This manual describes the Alpha PCI 164-266 (order number EBP40–AN) and Alpha PCI 164-300 (order number EBP41–AN) motherboards configured for the Microsoft Windows NT operating system.

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Maynard, Massachusetts**

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About This Manual

This manual describes Digital's Alpha PCI 164–266/300 microprocessor motherboard, a module for computing systems based on the Alpha 21164 microprocessor and the DECchip 21171 chipset.

Audience

This guide is intended for system designers and others who are intending to embed a compute engine into their system. It is written to assist the designer in familiarization with the predominant features of Digital's real-time motherboards and Digital's Alpha family of microprocessors.

Scope

This manual describes the features, configuration, and installation of the Alpha PCI 164–266/300. This manual does not include specific bus specifications (for example, PCI or ISA buses). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix B for information about how to order additional documentation.

Content

This manual contains the following chapters and appendixes:

- Chapter 1, Introduction to the Alpha PCI 164–266/300, is an overview of the Alpha PCI 164–266/300, including its components, uses, and features.
- Chapter 2, System Configuration and Connectors, describes the user environment configuration; board connectors and functions; jumper functions; and identifies jumper and connector locations.
- Chapter 3, Starting and Using the Alpha PCI 164–266/300, lists additional hardware and software requirements, provides information on how to configure the hardware and software, and describes the motherboard startup procedures.

- Chapter 4, Functional Description, describes some of the functional elements of the Alpha PCI 164–266/300, such as flash ROM contents, interrupt assignments, and power distribution.
- Chapter 5, Alpha PCI 164–266/300 Requirements, Power, and Parameters, describes the Alpha PCI 164–266/300 power and environmental requirements, and identifies major board components.
- Appendix A, Supporting Vendor Products, lists suggested vendor sources for supporting components, such as, power supply, SIMMs, enclosure, and so forth.
- Appendix B, Technical Support and Additional Documentation, describes how to order associated literature.

Document Conventions

This section provides the conventions used in this document.

Caution: Cautions indicate potential damage to equipment or data.

Note: Notes provide additional information.

Numbering: All numbers are decimal or hexadecimal unless otherwise indicated. In case of ambiguity, a subscript indicates the radix of nondecimal numbers. For example, 19 is a decimal number, but 19_{16} and 19A are hexadecimal numbers.

Extents: Extents are specified by a single number, or a pair of numbers in angle brackets (< >) separated by a colon (:) and are inclusive. For example, bits <7:3> specify an extent including bits 7, 6, 5, 4, and 3. Multiple bit fields are shown as extents.

Register Figures: Register figures have bit and field position numbering starting at the right (low-order) and increasing to the left (high-order).

Signal Names: Signal names in text are printed in boldface lowercase type. For example, “. . . bits **data<127:0>** are delivered to the Bcache SIMM connectors . . . ”

Introduction to the Alpha PCI 164–266/300

This chapter provides an overview of the Alpha PCI 164–266/300 motherboard and describes the Alpha PCI 164–266/300, its components, features, and uses.

1.1 System Components and Features

The Alpha PCI 164–266/300 is implemented in industry-standard parts and uses a 266 or 300 MHz Alpha 21164 microprocessor. The functional components are shown in Figure 1–1 and are introduced in the following subsections.

1.1.1 DECchip 21171 Core Logic Chipset

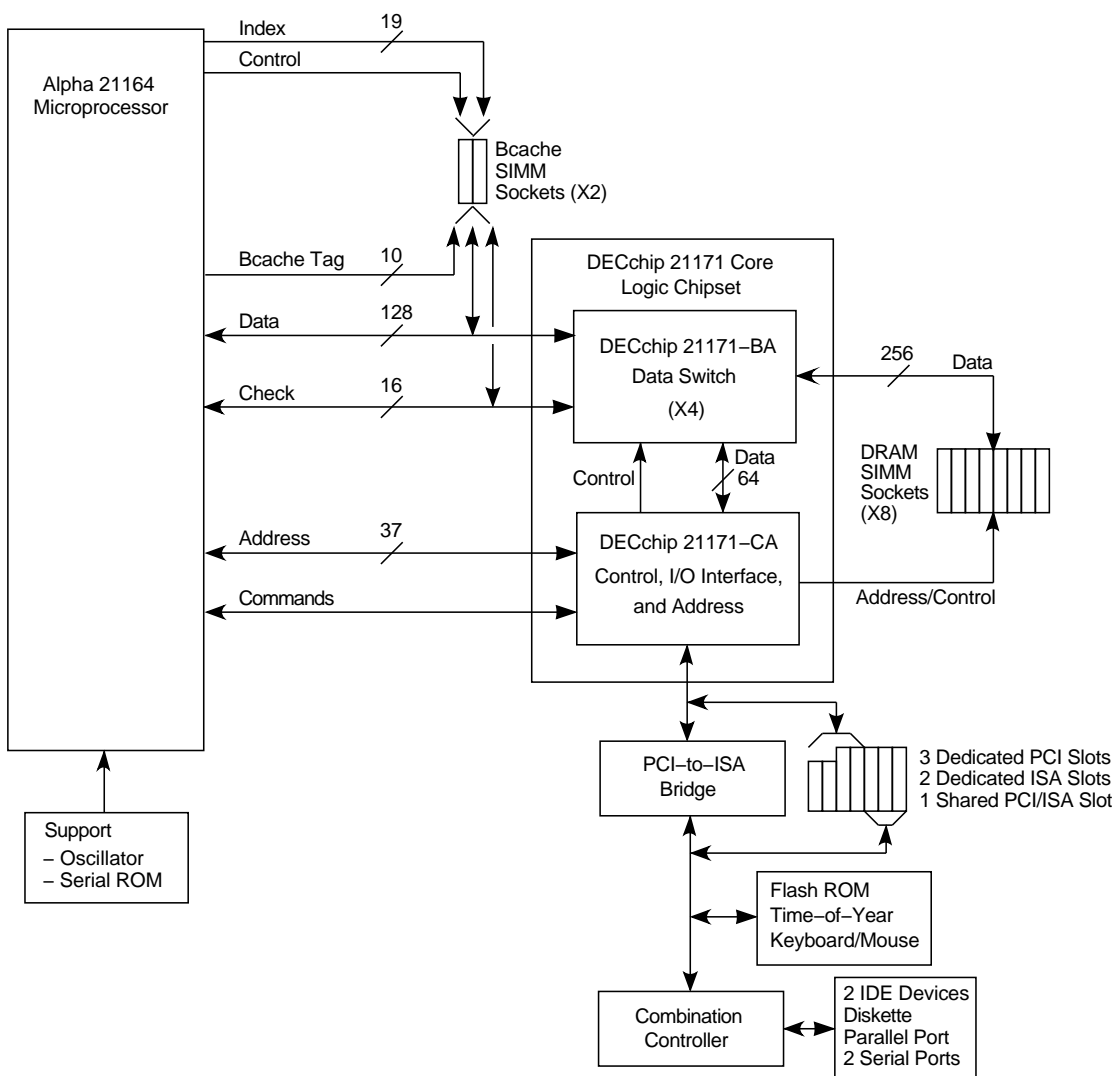
The 21164 is supported by the DECchip 21171 (21171) chipset. The 21171 consists of the following two application-specific integrated circuit (ASIC) types:

- One copy of the DECchip 21171-CA control, I/O interface, and address chip (CIA) provides the interface between the 21164, main memory (addressing and control), and the peripheral component interconnect (PCI) bus. It also provides the data switch companion chips with control information to direct the data flow.
- Four copies of the DECchip 21171-BA data switch chip (DSW) provide the memory interface data path and route PCI data through the CIA chip.

The chipset includes the majority of functions required to develop a high-performance PC or workstation, requiring minimum discrete logic on the module. It provides flexible and generic functions to allow its use in a wide range of systems.

1.1 System Components and Features

Figure 1-1 Alpha PCI 164-266/300 Functional Block Diagram



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1.1 System Components and Features

1.1.2 Memory Subsystem

The dynamic random-access memory (DRAM) provides 32MB to 512MB with a 256-bit data bus. The memory is contained in one bank of eight commodity single inline memory modules (SIMMs). Single- or double-sided SIMMs may be used. Each SIMM is 36 bits wide, with 32 data bits and 4 check bits, with 70 ns or less access. Table 1–1 lists the SIMM sizes supported and the corresponding main memory size for 256-bit arrays.

Table 1–1 Main Memory Sizes

SIMM Size	Eight SIMMs (256-Bit Array)
1M × 36	32MB
2M × 36	64MB
4M × 36	128MB
8M × 36	256MB
16M × 36	512MB

All eight SIMM connectors (J3 through J10) must be populated. See Figure 2–3 and Table 2–2.

1.1.3 L3 Bcache Subsystem Overview

The board-level external L3 backup cache (Bcache) subsystem supports multiple cache sizes and access times. Cache sizes supported are 2MB with Alpha cache SIMMs populated with 128K × 8 SRAMs, and 4MB and 8MB with SIMMs populated with 512K × 8 SRAMs. Speeds of 6 ns to 15 ns can be used.

The Alpha PCI 164–266/300 has a 2MB 10-ns Bcache SIMM.

1.1.4 PCI Interface Overview

The Alpha PCI 164–266/300 PCI interface is the main I/O bus for the majority of functions (SCSI interface, graphics accelerator, and so on). The PCI interface provides a selectable PCI speed between 25 MHz and 33 MHz (based on the 21164 clock divisor). An onboard PCI-to-ISA bridge is provided through an Intel 82378ZB Saturn I/O (SIO) chip.

The PCI bus has three dedicated PCI expansion slots (one 64-bit and two 32-bit) and one shared 64-bit PCI/ISA slot.

1.1 System Components and Features

1.1.5 ISA Interface Overview

The ISA bus has two dedicated slots and a third shared ISA/PCI slot. It provides the following system support functions:

- Mouse and keyboard controller functions—provided by an Intel 8242 chip.
- An IDE interface, a diskette controller, two universal asynchronous receiver-transmitters (UARTs) with full modem control, and a bidirectional parallel port—provided by a National 87312 combination chip.
- A time-of-year (TOY) function—provided by a Dallas Semiconductor DS1287 chip.
- Operating system support—provided by a 1MB flash ROM that contains firmware and debug monitor code.

Users can develop code on a host system, and load software into the Alpha PCI 164–266/300 through a serial line, diskette, or Ethernet board. In addition, sectors of the flash ROM can be programmed for application-specific purposes.

1.1.6 Miscellaneous Logic

The Alpha PCI 164–266/300 contains the following miscellaneous components:

- Clocks
 - A 26.66-MHz oscillator and phase-locked loop (PLL) clock generator provide a clock source to the 21164 microprocessor and system.
 - A 14.3-MHz crystal and frequency generator provide a clock source for ISA devices.
- Serial ROM
 - A Xilinx XC17128 serial ROM (SROM) contains initial code that is loaded into the 21164 instruction cache (Icache) on power-up. A serial line interface is also provided to allow direct connection to a terminal line for debugging purposes.
- Programmable array logic (PAL) devices for the following functions:
 - One PAL for utility bus (Ubus) decoding
 - One PAL for interrupts
 - Two PAL devices for memory row address strobe (RAS) bank generation and buffering

1.1 System Components and Features

1.1.7 Software Support

The Alpha PCI 164–266/300 supports the Microsoft Windows NT operating system through a firmware console. This console is resident on the module (the ARC console for Windows NT) in 1MB of flash ROM. In addition to the console supporting the operating system, the console provides code for power-up testing and initialization. There is also a debug monitor.

The basic debug monitor supports the following functions:

- Download files through serial and Ethernet ports and diskette.
- Load data from a ROM through the debug monitor.
- Examine and deposit the Alpha PCI 164–266/300 system registers, a few 21164 internal processor registers (IPRs), and I/O mapped registers.
- Examine and modify DRAM and I/O mapped memory.
- Disassemble CPU instructions in memory.
- Transfer control to programs in memory.
- Perform native debugging operations, including breakpoints and single stepping.
- Perform full source-level debugging operations by using DECladebug software running on a host communicating through an Ethernet connection.
- Perform a memory image dump.

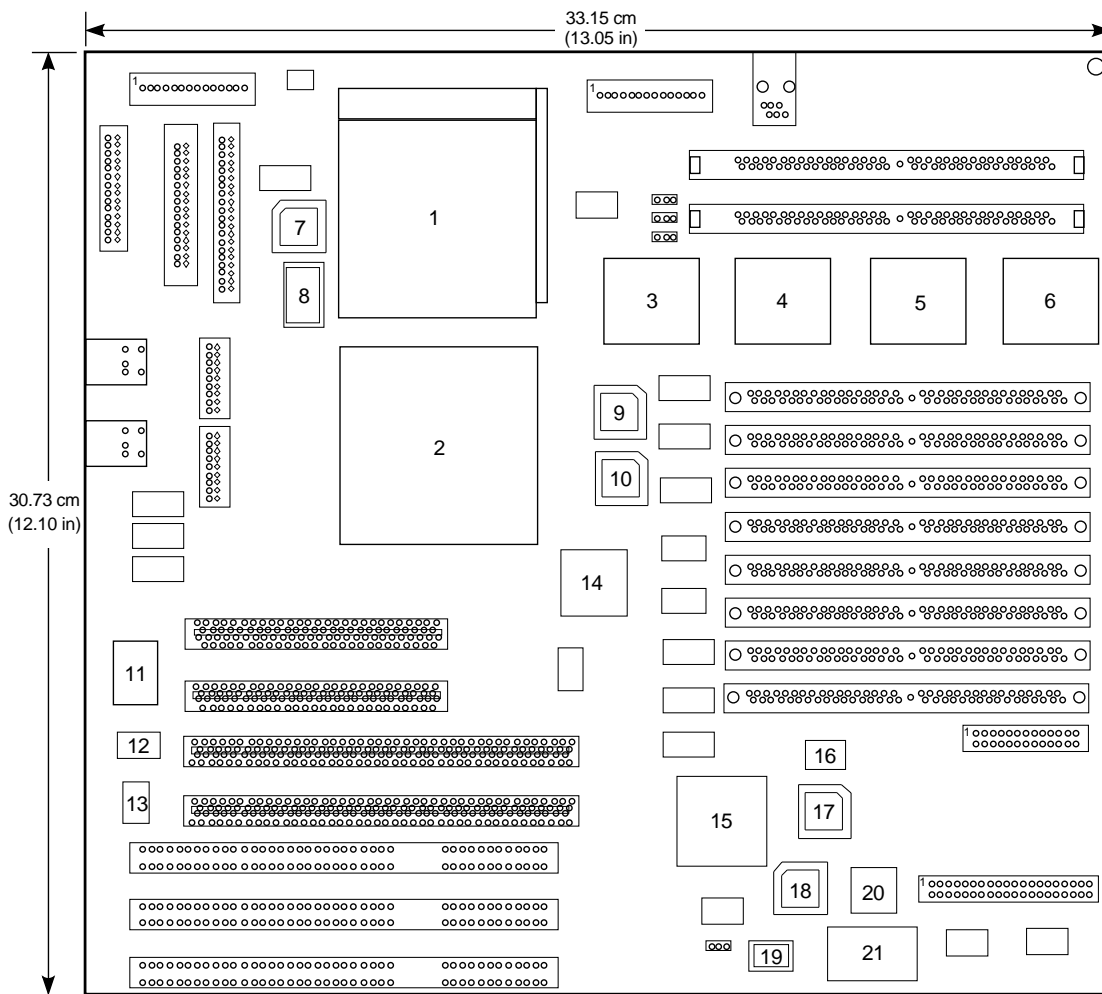
The debug monitor is described in detail in the *Alpha Microprocessors Motherboard Debugs Monitor User's Guide*.

1.1.8 Component Layout

Figure 1–2 shows the Alpha PCI 164–266/300 board component layout and dimensions.

1.1 System Components and Features

Figure 1-2 Board Component Layout



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1.2 Alpha PCI 164-266/300 Summary

The features of the Alpha PCI 164-266/300 are listed and described in Table 1-2.

1.2 Alpha PCI 164–266/300 Summary

Table 1–2 Alpha PCI 164–266/300 Features Summary

Characteristic	Description												
Operating Systems													
Supported operating systems	Microsoft Windows NT V3.51 or higher												
System Characteristics													
CPU and clock speed	Alpha 21164 at 266 or 300 MHz												
CPU upgradable	ZIF socket for Alpha 21164 upgrade												
Instruction issue	Up to 4 instructions issued per clock cycle												
Word size	64 bits												
Address size	40-bit physical address, 43-bit virtual address												
Floating-point format	VAX (F and G) and IEEE (S and T) data types												
Memory (DRAM)	Minimum DRAM 32MB plus ECC Maximum DRAM 512MB plus ECC												
Memory (ROM)	1MB flash ROM												
External L2 cache	Configurable for 2MB, 4MB, 8MB (128-bit data)												
Memory bus width	256 bits plus ECC												
Performance metrics	The Alpha PCI 164–266/300 performance is listed here: <table border="1"> <thead> <tr> <th>Alpha 21164</th> <th>Bcache</th> <th>SPECint92</th> <th>SPECfp92</th> </tr> </thead> <tbody> <tr> <td>266 MHZ</td> <td>2MB, 10ns</td> <td>300.6</td> <td>417.4</td> </tr> <tr> <td>300 MHZ</td> <td>2MB, 10ns</td> <td>335 (estimated)</td> <td>460 (estimated)</td> </tr> </tbody> </table>	Alpha 21164	Bcache	SPECint92	SPECfp92	266 MHZ	2MB, 10ns	300.6	417.4	300 MHZ	2MB, 10ns	335 (estimated)	460 (estimated)
Alpha 21164	Bcache	SPECint92	SPECfp92										
266 MHZ	2MB, 10ns	300.6	417.4										
300 MHZ	2MB, 10ns	335 (estimated)	460 (estimated)										
Graphics													
Graphics options	Refer to the Microsoft <i>Hardware Compatibility List</i> for Windows NT to determine which graphics cards are supported. See Section B.2 for information on how to obtain the listing.												

(continued on next page)

1.2 Alpha PCI 164–266/300 Summary

Table 1–2 (Cont.) Alpha PCI 164–266/300 Features Summary

Characteristic	Description
Input/Output	
Input device interfaces	PS/2 style keyboard and mouse
Serial	Two RS423-compatible (9-position) serial communications ports
Parallel	One parallel (Centronics compatible) communications port
Bus options	Total of 6 option slots
PCI bus	Supports two 64-bit PCI options slots at 5V and two 32-bit PCI option slots at 5V
ISA bus	Supports three 16-bit ISA option slots
IDE	One IDE interface supporting up to 2 drives
Diskette	One 82077-compatible diskette controller supporting up to 2 drives with 1.44MB and 2.88MB formats
Environmental Characteristics (Operating)	
Operating temperature	10°C to 40°C (50°F to 104°F)
Maximum rate of (dry bulb) temperature change	11°C/hour ±2°C/hour (20°F/hour ±4°F/hour)
Relative humidity	10%–90% noncondensing
Maximum wet bulb	32°C (90°F)
Minimum dew point	2°C (36°F)
EMC compliance	Compliance certification is the responsibility of the system integrator. The Alpha PCI 164–266/300 was tested in industry-representative enclosures to prove feasibility of emissions compliance.
Shock and vibration	Passing of shock and vibration tests is dependent on the method used to mount the system board, the design of the enclosure, and how the enclosure is supported. Testing is the responsibility of the system integrator.
Physical Characteristics	
Form factor	Standard, full-size PC AT board
Width/depth	30.73 cm (12.10 in) × 33.15 cm (13.05 in)

System Configuration and Connectors

The Alpha PCI 164–266/300 uses jumpers to implement configuration parameters such as variations in L3 backup cache (Bcache) size, access timing, and speed, as well as boot parameters. These jumpers must be configured for the user's environment. Onboard connectors are provided for the I/O interfaces, single inline memory modules (SIMMs), and serial and parallel peripheral ports.

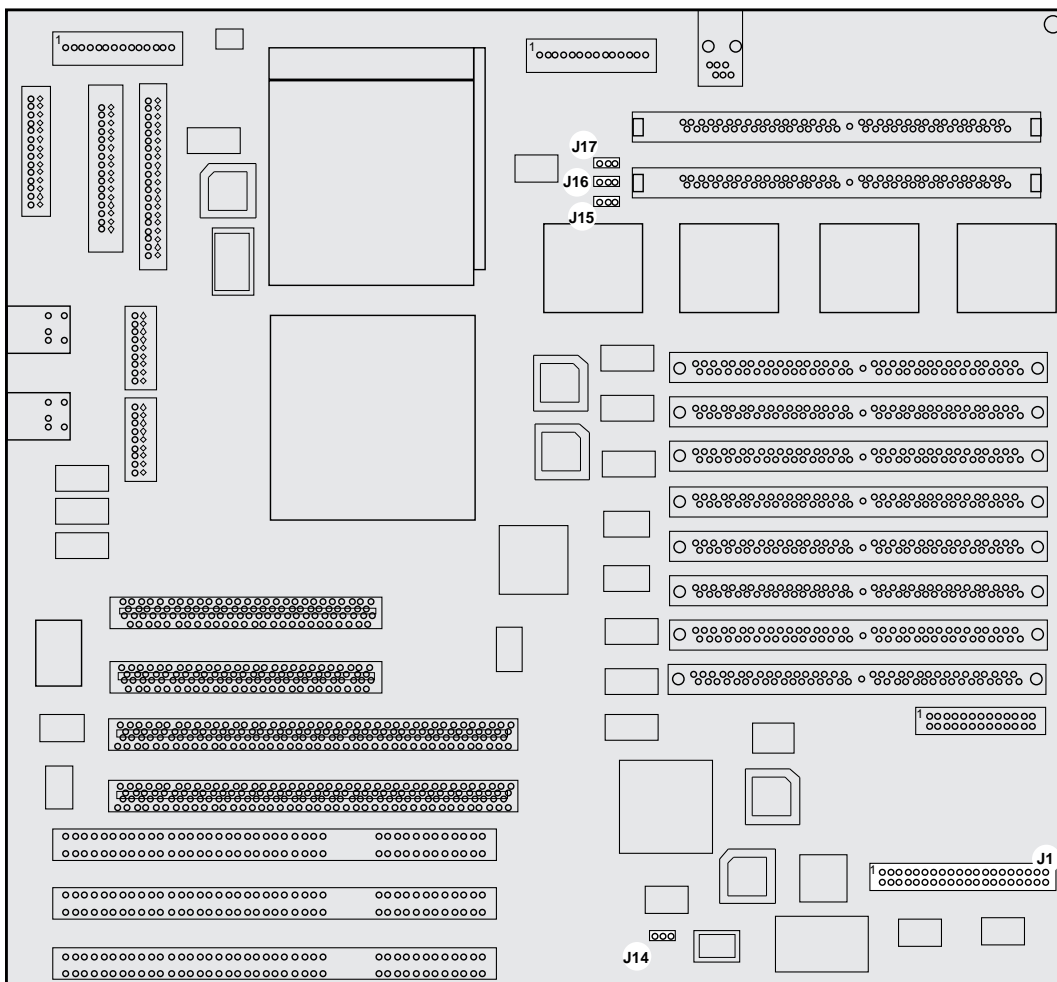
After the module is configured, power can be applied, and the debug monitor can be run. The debug monitor and its commands are described in the *Alpha Microprocessors Motherboard Debug Monitor User's Guide*. Appendix B provides information about other software design tools.

2.1 Configuration Jumpers

Figure 2–1 identifies the location of the software and hardware configuration jumpers, and Table 2–1 provides descriptions. Figure 2–2 provides a detailed view of the configuration jumpers and their function.

2.1 Configuration Jumpers

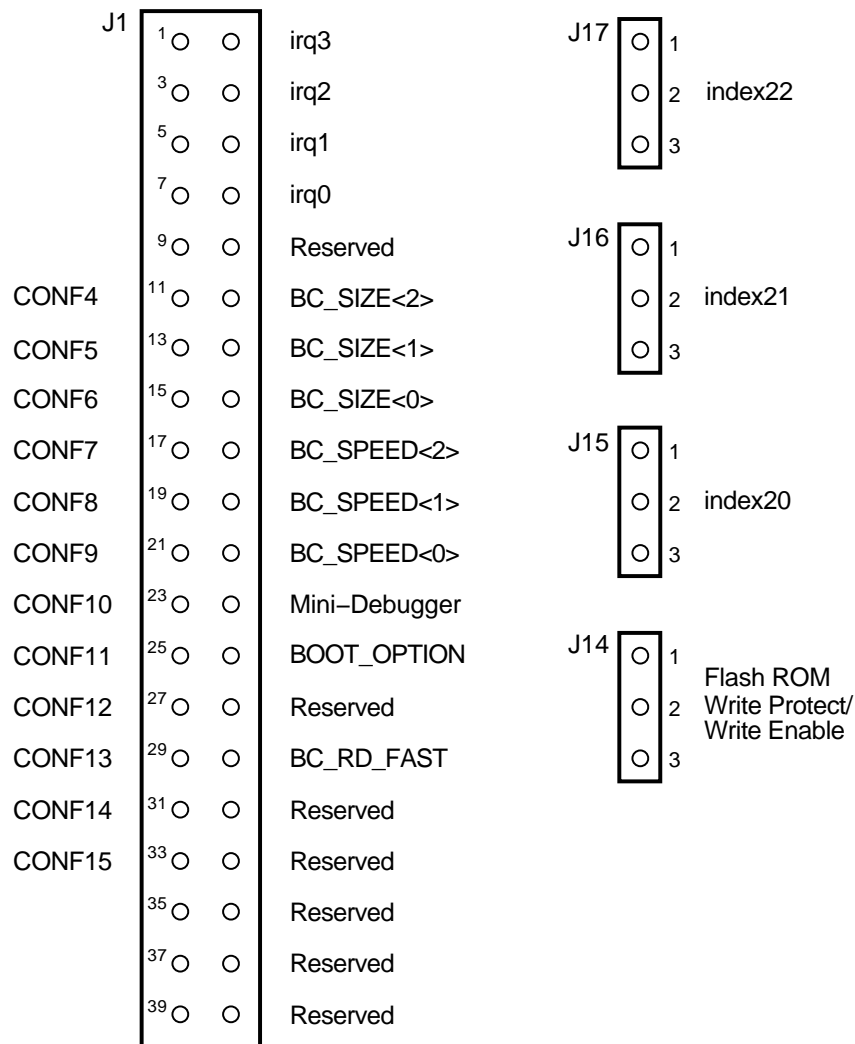
Figure 2–1 Alpha PCI 164–266/300 Jumper Locations



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2.1 Configuration Jumpers

Figure 2–2 Configuration Jumpers



MK-2306-04

2.1 Configuration Jumpers

Table 2–1 Configuration Jumper Position Descriptions

Feature	Jack/Jumper—Pins and Description				
System clock divisor	J1—1/2, —3/4, —5/6, —7/8				
	J1—1/2 (irq3)	J1—3/4 (irq2)	J1—5/6 (irq1)	J1—7/8 (irq0)	Ratio
	In	In	Out	Out	3
	In	Out	In	In	4
	In	Out	In	Out	5
	In	Out	Out	In	6
	In	Out	Out	Out	7
	Out	In	In	In	8
	Divisor 8 is used for 266 MHz.				
	Out	In	In	Out	9
	Divisor 9 is used for 300 MHz.				
	Out	In	Out	In	10
	Out	In	Out	Out	11
	Out	Out	In	In	12
	Out	Out	In	Out	13
Out	Out	Out	In	14	
Out	Out	Out	Out	15	

(continued on next page)

2.1 Configuration Jumpers

Table 2–1 (Cont.) Configuration Jumper Position Descriptions

Feature	Jack/Jumper—Pins and Description			
BC_SIZE<2:0>	J1—11/12 (CONF4), —13/14 (CONF5), —15/16 (CONF6)			
	These jumpers allow the Bcache to emulate the sizes specified in the following table. These jumpers are changed in conjunction with the appropriate index jumpers J17, J16, and J15.			
	CONF4 Pins 11/12	CONF5 Pins 13/14	CONF6 Pins 15/16	Bcache
	In	In	In	Reserved
	In	In	Out	Reserved
	In	Out	In	Reserved
	In	Out	Out	2MB (default)
	Out	In	In	4MB
	Out	In	Out	8MB
	Out	Out	In	Reserved
	Out	Out	Out	Reserved
Bcache size— index address bits <22:20>	J17, J16, J15			
	Jumper	2MB¹ (default)	4MB²	8MB²
	J17 (index22)	2 to 3	2 to 3	1 to 2
	J16 (index21)	2 to 3	1 to 2	1 to 2
	J15 (index20)	1 to 2	1 to 2	1 to 2

¹SIMMs populated with 128K × 8 or 512K × 8 SRAMs

²SIMMs populated with 512K × 8 SRAMs

(continued on next page)

2.1 Configuration Jumpers

Table 2–1 (Cont.) Configuration Jumper Position Descriptions

Feature	Jack/Jumper—Pins and Description																																				
BC_SPEED<2:0>	<p>J1—17/18 (CONF7), —19/20 (CONF8), —21/22 (CONF9)</p> <p>These jumpers select the Bcache timing parameters used to compute the BC_CONFIG register value. Select the jumper configuration that matches the access time for the SRAMs being used.</p> <table border="1"> <thead> <tr> <th>CONF7 Pins 17/18</th> <th>CONF8 Pins 19/20</th> <th>CONF9 Pins 21/22</th> <th>Bcache Speed</th> </tr> </thead> <tbody> <tr> <td>In</td> <td>In</td> <td>In</td> <td>Reserved</td> </tr> <tr> <td>In</td> <td>In</td> <td>Out</td> <td>6-ns SRAM timing</td> </tr> <tr> <td>In</td> <td>Out</td> <td>In</td> <td>8-ns SRAM timing</td> </tr> <tr> <td>In</td> <td>Out</td> <td>Out</td> <td>10-ns SRAM timing (default)</td> </tr> <tr> <td>Out</td> <td>In</td> <td>In</td> <td>12-ns SRAM timing</td> </tr> <tr> <td>Out</td> <td>In</td> <td>Out</td> <td>15-ns SRAM timing</td> </tr> <tr> <td>Out</td> <td>Out</td> <td>In</td> <td>Reserved</td> </tr> <tr> <td>Out</td> <td>Out</td> <td>Out</td> <td>Reserved</td> </tr> </tbody> </table>	CONF7 Pins 17/18	CONF8 Pins 19/20	CONF9 Pins 21/22	Bcache Speed	In	In	In	Reserved	In	In	Out	6-ns SRAM timing	In	Out	In	8-ns SRAM timing	In	Out	Out	10-ns SRAM timing (default)	Out	In	In	12-ns SRAM timing	Out	In	Out	15-ns SRAM timing	Out	Out	In	Reserved	Out	Out	Out	Reserved
CONF7 Pins 17/18	CONF8 Pins 19/20	CONF9 Pins 21/22	Bcache Speed																																		
In	In	In	Reserved																																		
In	In	Out	6-ns SRAM timing																																		
In	Out	In	8-ns SRAM timing																																		
In	Out	Out	10-ns SRAM timing (default)																																		
Out	In	In	12-ns SRAM timing																																		
Out	In	Out	15-ns SRAM timing																																		
Out	Out	In	Reserved																																		
Out	Out	Out	Reserved																																		
Mini-Debugger	<p>J1—23/24 (CONF10)</p> <p>The Alpha SROM Mini-Debugger is provided in the SROM. This jumper (In) causes the SROM initialization to trap to the Mini-Debugger (connector J13) after all initialization is complete, but before starting the execution of the system flash ROM code. The default position for this jumper is out.</p>																																				

(continued on next page)

2.1 Configuration Jumpers

Table 2–1 (Cont.) Configuration Jumper Position Descriptions

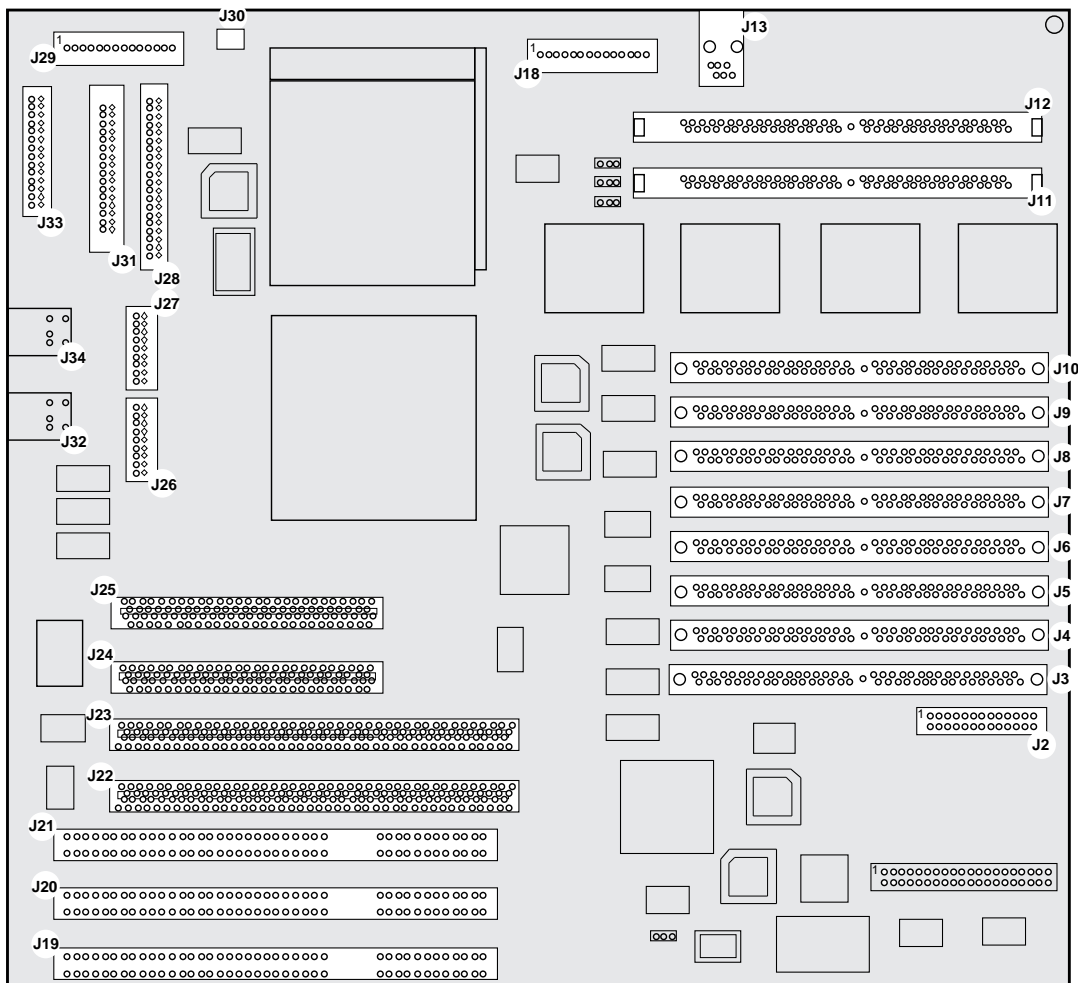
Feature	Jack/Jumper—Pins and Description						
BOOT_OPTION	<p>J1—25/26 (CONF11)</p> <p>This jumper selects the image to be loaded into memory from the system flash ROM. With the jumper out (bit = 1), the first image (debug monitor) is loaded. With the jumper in (bit = 0), alternate images can be loaded depending upon the value stored in TOY RAM location 0x3F. The default position for this jumper is in. For more information on the system ROM header and boot images, refer to Section 4.5.1.</p>						
BC_RD_FAST	<p>J1—29/30 (CONF13)</p> <p>This jumper forces a Bcache read speed setting of 1 cycle faster than nominal.</p> <table border="1"> <thead> <tr> <th>BC_RD_FAST</th> <th>Bcache Speed</th> </tr> </thead> <tbody> <tr> <td>In</td> <td>Make read speed 1 cycle faster</td> </tr> <tr> <td>Out</td> <td>Nominal read speed (default)</td> </tr> </tbody> </table>	BC_RD_FAST	Bcache Speed	In	Make read speed 1 cycle faster	Out	Nominal read speed (default)
BC_RD_FAST	Bcache Speed						
In	Make read speed 1 cycle faster						
Out	Nominal read speed (default)						
Flash ROM write-protect/write-enable jumper	<p>J14</p> <table border="1"> <thead> <tr> <th>Jumper Pins</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>1 to 2</td> <td>Flash ROM write-protect</td> </tr> <tr> <td>2 to 3</td> <td>Flash ROM write-enable (default)</td> </tr> </tbody> </table>	Jumper Pins	Function	1 to 2	Flash ROM write-protect	2 to 3	Flash ROM write-enable (default)
Jumper Pins	Function						
1 to 2	Flash ROM write-protect						
2 to 3	Flash ROM write-enable (default)						

2.2 Alpha PCI 164–266/300 Connectors

2.2 Alpha PCI 164–266/300 Connectors

Figure 2–3 shows the Alpha PCI 164–266/300 connectors and Table 2–2 describes them. Figure 2–4 provides a detail of header connector J2.

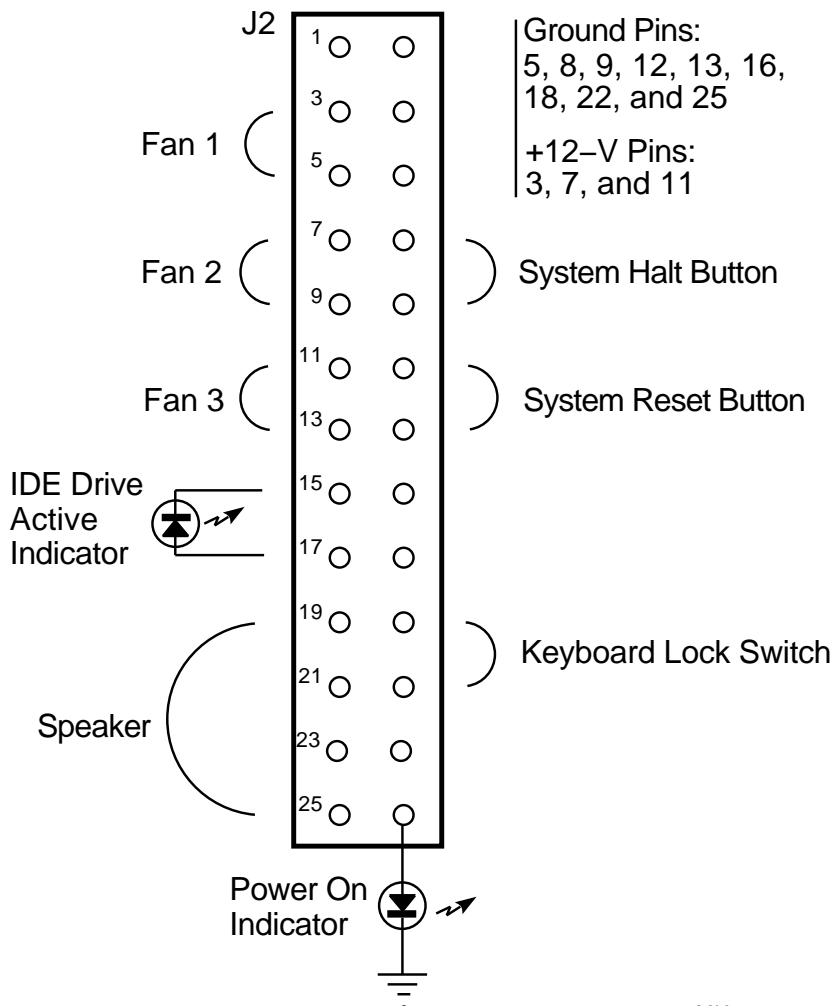
Figure 2–3 Alpha PCI 164–266/300 Connector Locations



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2.2 Alpha PCI 164-266/300 Connectors

Figure 2-4 Detail of Header Connector J2



MK-2306-27

2.2 Alpha PCI 164–266/300 Connectors

Table 2–2 Alpha PCI 164–266/300 Connector Descriptions

Connector	Pins	Description
Main Memory/Bcache SIMMs		
J10	72	DRAM 0 SIMM
J9	72	DRAM 1 SIMM
J8	72	DRAM 2 SIMM
J7	72	DRAM 3 SIMM
J6	72	DRAM 4 SIMM
J5	72	DRAM 5 SIMM
J4	72	DRAM 6 SIMM
J3	72	DRAM 7 SIMM
<p>Note: To fill a 256-bit data path, all SIMM connectors J3 through J10 must be populated.</p>		
J11	60	Bcache 0 SIMM
J12	60	Bcache 1 SIMM
<p>Note: Both Bcache SIMM connectors must be populated.</p>		
PCI Connectors		
J22	184	PCI64 connector 0
J23	184	PCI64 connector 1
J24	124	PCI32 connector 2
J25	124	PCI32 connector 3
ISA Connectors		
J19	98	ISA connector slot 0
J20	98	ISA connector slot 1
J21	98	ISA connector slot 2
Keyboard Connector		
J32	6	Keyboard connector

(continued on next page)

2.2 Alpha PCI 164–266/300 Connectors

Table 2–2 (Cont.) Alpha PCI 164–266/300 Connector Descriptions

Connector	Pins	Description
Mouse Connector		
J34	6	Mouse connector
National 87312 Combination Chip Connectors		
J33	26	Parallel port connector Connects to an external 25-pin connector.
J27	10	Serial communication port 1 connector Note: This connector can be used as a terminal port for the debug monitor.
J26	10	Serial communication port 2 connector
J31	34	Diskette drive connector (<i>eb164.28</i>)
J28	40	IDE drive connector (<i>eb164.29</i>)
SRAM Data/Clock		
J13	6	SRAM data/clock serial port input connector Note: This connector can be used as a terminal port for the Mini-Debugger.
J2	26	Header connector J2 is a straight double-row header with standard 0.025-in pins on 0.10-in centers. Connections to it may be made by means of individual 2- or 4-pin female plugs. Figure 2–4 provides a detail of header connector J2.
System Enclosure Fans		
J2–3/5, –7/9, –11/13	2 each	Up to three 12-V cooling fans may be connected to these pins.
IDE Drive Active Indicator		
J2–15/17	2	IDE drive active indicator pins

(continued on next page)

2.2 Alpha PCI 164–266/300 Connectors

Table 2–2 (Cont.) Alpha PCI 164–266/300 Connector Descriptions

Connector	Pins	Description
		Speaker
J2–19/21/23/25	—	Speaker connector pins
		Power On Indicator
J2–26	1	Power on indicator pin Connect LED from this pin to ground.
		System Halt Button
J2–8/10	2	System halt button pins
		System Reset Button
J2–12/14	2	System reset button pins
		Keyboard Lock Switch
J2–20/22	2	Keyboard lock switch pins

(continued on next page)

2.2 Alpha PCI 164–266/300 Connectors

Table 2–2 (Cont.) Alpha PCI 164–266/300 Connector Descriptions

Connector	Pins	Description	
J18	12	Power Connectors	
		Board power connector ¹	
		Pin	Voltage/Signal
		1	+3.3 V
		2	+3.3 V
		3	+3.3 V
		4	Ground
		5	Ground
		6	Ground
		7	Ground
		8	Ground
		9	Ground
		10	+3.3 V
11	+3.3 V		
12	+3.3 V		

¹Typically mates with two 6-pin power supply connectors.

(continued on next page)

2.2 Alpha PCI 164–266/300 Connectors

Table 2–2 (Cont.) Alpha PCI 164–266/300 Connector Descriptions

Connector	Pins	Description																										
J29	12	Board power connector ¹																										
		<table border="1"> <thead> <tr> <th>Pin</th> <th>Voltage/Signal</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>p_dcok</td> </tr> <tr> <td>2</td> <td>Vdd (+5 V)</td> </tr> <tr> <td>3</td> <td>+12 V</td> </tr> <tr> <td>4</td> <td>–12 V</td> </tr> <tr> <td>5</td> <td>Ground</td> </tr> <tr> <td>6</td> <td>Ground</td> </tr> <tr> <td>7</td> <td>Ground</td> </tr> <tr> <td>8</td> <td>Ground</td> </tr> <tr> <td>9</td> <td>–5 V</td> </tr> <tr> <td>10</td> <td>Vdd (+5 V)</td> </tr> <tr> <td>11</td> <td>Vdd (+5 V)</td> </tr> <tr> <td>12</td> <td>Vdd (+5 V)</td> </tr> </tbody> </table>	Pin	Voltage/Signal	1	p_dcok	2	Vdd (+5 V)	3	+12 V	4	–12 V	5	Ground	6	Ground	7	Ground	8	Ground	9	–5 V	10	Vdd (+5 V)	11	Vdd (+5 V)	12	Vdd (+5 V)
Pin	Voltage/Signal																											
1	p_dcok																											
2	Vdd (+5 V)																											
3	+12 V																											
4	–12 V																											
5	Ground																											
6	Ground																											
7	Ground																											
8	Ground																											
9	–5 V																											
10	Vdd (+5 V)																											
11	Vdd (+5 V)																											
12	Vdd (+5 V)																											
J30	3	<p>CPU fan power and sensor</p> <p>Caution: Fan sensor required.</p> <p>The fan <i>must</i> have a built-in sensor that drives a signal low while the fan spins. The sensor must be connected to pin J30–2. The fan supplied with the Alpha PCI 164–266/300 includes a fan sensor.</p>																										
<p>¹Typically mates with two 6-pin power supply connectors.</p>																												

3

Starting and Using the Alpha PCI 164–266/300

This chapter lists hardware, software, and accessories that users must obtain to completely furnish a functioning computer system. The chapter then describes how to configure the hardware and software. Finally, the chapter describes how to start and use the Alpha PCI 164–266/300.

3.1 Hardware Requirements

Before turning on the power to your Alpha PCI 164–266/300, you must provide the following components in addition to those supplied in the kit. The components needed depend upon the intended use of the Alpha PCI 164–266/300 board.

- Eight 72-pin, 36-bit, 5-V, DRAM SIMM memory modules (connectors J3 through J10). SIMMs must consist of identical devices. Digital recommends that all SIMMs be purchased from the same vendor.
- An industry-standard PC power supply that includes a 3.3-V dc output, rated at a minimum of 339 W (refer to Appendix A).
- A PS/2 compatible 101-key keyboard.
- A PS/2 compatible mouse.
- A supported PCI or ISA bus graphics card, cables, and a compatible monitor.
- A supported PCI or ISA bus SCSI controller and cables.
- An IDE or SCSI CD-ROM drive.
- An IDE or SCSI hard drive.
- A 3.5-in diskette drive and cable.
- A 9-pin serial line cable.

3.1 Hardware Requirements

- A terminal or a serial line connection to a host system with appropriate cables.

Refer to the *Alpha PCI 164-266/300 Digital UNIX and Microsoft Windows NT Installation Guide* from Digital and the *Hardware Compatibility List* for Windows NT available from Microsoft (see Section B.2) to determine which SCSI controllers and graphics cards are supported.

For more information about hardware requirements and for the location of board connectors and jumpers, see Chapter 2.

3.2 Software Requirements

The following software media is required to install and run the Windows NT operating system:

- A Windows NT 3.51 CD-ROM
- An Alpha PCI 164-266/300 Windows NT 3.51 installation diskette

3.3 Hardware Configuration

Once you have acquired the necessary hardware, it must be assembled into a system. This section lists the necessary steps. The system does not have to be assembled in the order presented.

Caution: Static-Sensitive Components

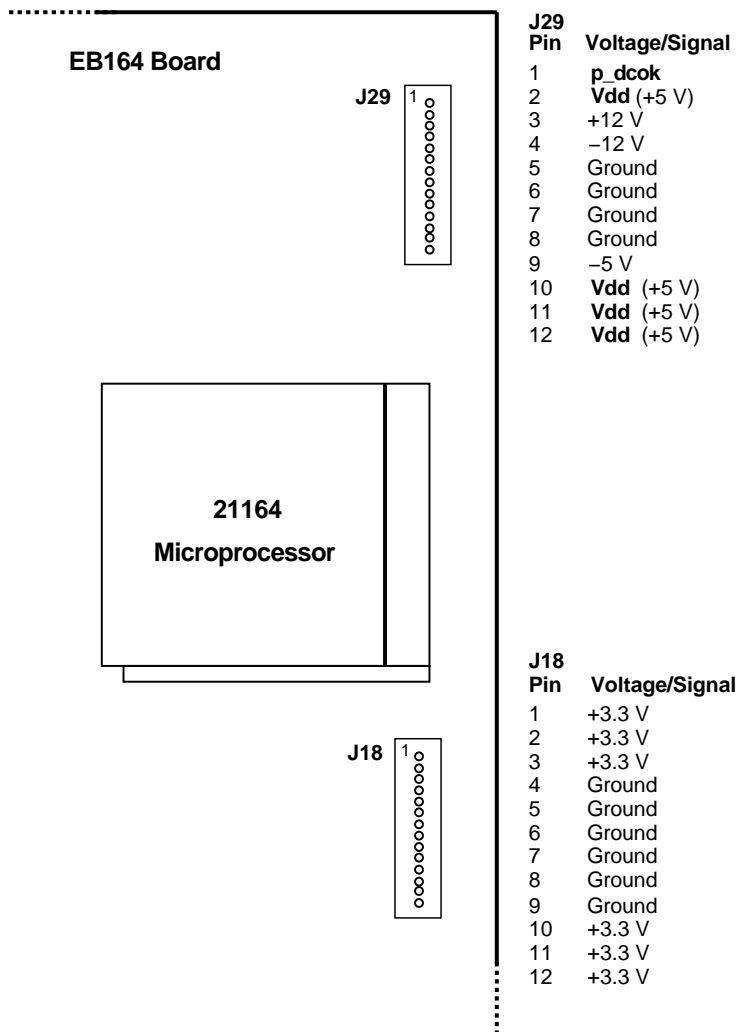
Due to the sensitive nature of electronic components to static electricity, Digital strongly advises that anyone handling the Alpha PCI 164-266/300 or any associated components wear a properly grounded antistatic wrist strap. Use of antistatic mats, ESD approved workstation, or exercising other good ESD practices is recommended.

3.3 Hardware Configuration

1. Install eight system memory DRAM SIMMs. Refer to Table 2–2 for socket locations.
 - a. **Observe antistatic precautions.** Handle SIMMs at the edges only to prevent damage.
 - b. SIMMs must be installed in groups of eight consisting of identical devices.
 - c. Hold the SIMM at an angle with the notch facing the key in the socket.
 - d. Firmly push the module into the connector and stand the module upright.
 - e. Make sure that the SIMM snaps into the metal locking clips on both ends.
2. If you intend to mount the motherboard in a system enclosure, do so now. Install the power supply into the enclosure first, then the motherboard. Appendix A lists a suggested enclosure and a suggested power supply. The enclosure you use should be able to accept a standard, full-size PC AT board.
3. Connect the power supply to the Alpha PCI 164–266/300 board, as shown in Figure 3–1, with standard power to J29, and with 3.3-V dc power to J18.
4. Connect the supplied 3.5-inch diskette drive. The 34-pin diskette drive cable goes from connector J31 on your Alpha PCI 164–266/300 to the diskette drive. The drive should be connected at the very end of the cable closest to the twist in the cable. Attach a power connector to the drive. Again, make sure to insert the connector in the proper orientation so that pin 1 on the cable matches pin 1 on the board header (as indicated on the module).
5. If you will be using any SCSI devices, such as a SCSI CD-ROM drive or hard disk, install the SCSI controller in any free PCI or ISA slot. Then connect the drives, being sure *only* the last drive connected to the cable is terminated, or use a cable terminator if the last drive does not have SCSI bus termination capability. Follow the drive manufacturer's installation instructions to set each drive on the bus to a unique ID number and each drive except the last to non-terminated. The primary drive on the bus should be a hard drive.
6. If you will be using one or more IDE CD-ROMs, hard drives, or other IDE devices, attach your IDE cable to connector J26 in the proper orientation. An IDE hard drive should be configured as the primary device on the IDE bus. Refer to the manufacturer's instructions for setting up the hard drive.

3.3 Hardware Configuration

Figure 3–1 Alpha PCI 164–266/300 Power Connectors



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3.3 Hardware Configuration

7. If you will be using an IDE hard drive, attach your IDE cable to connector J28 in the proper orientation and install your hard drive. The disk should be configured as the primary device on the IDE bus. Refer to the manufacturer's instructions for setting up the hard drive.
8. If you plan to use your Alpha PCI 164–266/300 on a network, install the Ethernet controller board in one of the PCI connectors as outlined in the controller's documentation.
9. Install the graphics card into either a PCI or ISA connector, depending on the card you are using. Connect the graphics card to a compatible monitor following the graphics card manufacturer's instructions.
10. Connect the keyboard cable to connector J32.
11. Connect the mouse cable to connector J34.
12. Connect the 9-pin serial port adapter cable, provided in the kit, to the COM1 connector at J27. Insert the connector in the proper orientation, so that pin 1 on the cable matches pin 1 on the board header (as indicated on the module).
13. Connect your terminal to the COM1 port, using a cable arrangement appropriate to your terminal. Set the terminal to 9600 baud, 8 data bits, 1 stop bit, no parity.
14. Connect miscellaneous items such as, enclosure fans, reset button, speaker, power indicator, hard drive active indicator (if using an IDE drive), keyboard lock switch, and so forth.

3.4 Software Configuration

Two firmware programs have been loaded into the Alpha PCI 164–266/300 1MB flash ROM. They are the debug monitor and the Windows NT ARC firmware. The debug monitor is a serial line monitor program used to perform software and hardware debug functions. The Windows NT ARC firmware is used to load and boot Windows NT. The Alpha PCI 164–266/300 system has been configured to start the Windows NT ARC firmware by default.

The serial ROM firmware uses a value stored in the nonvolatile RAM of the real-time clock to determine which firmware image to load. Once the Windows NT ARC firmware is running, you can switch to the debug monitor firmware.

3.4 Software Configuration

3.4.1 Starting Windows NT ARC Firmware

Start the Windows NT ARC firmware using the following procedure.

1. Verify that the jumper from J14-2 to J14-3 is inserted, allowing the flash ROM to be written. If the Windows NT ARC firmware is unable to write to flash ROM, it prints the device error message and stops.
2. Verify that the jumper at J1-25/26 is installed (see CONF11 on the module). The presence of the jumper at J1-25/26 forces the serial ROM firmware to load the alternate image selected by the value in the nonvolatile TOY RAM. The absence of this jumper overrides the value stored in the TOY RAM and causes the first image, the debug monitor, to be loaded.
3. Turn on the power to the Alpha PCI 164-266/300. After the power-up diagnostics are run, the ARC console boot menu appears on the graphics display.

If the ARC console boot menu does not appear, check the output of COM1 for error messages and review your hardware configuration.

You are ready for software installation. Refer to the *Alpha PCI 164-266/300 Digital UNIX and Microsoft Windows NT Installation Guide* for instructions.

3.4.2 Going to the Debug Monitor from Windows NT ARC Firmware

You can use either of the following two methods to access the debug monitor from the Windows NT ARC firmware.

- A. Use the ARC firmware menus to choose the debug monitor.
 1. At the Boot menu, choose **Supplementary menu...**
 2. At the Supplementary menu, choose **Setup the system...**
 3. At the Setup the system menu, choose **Machine specific setup...**
 4. At the Machine specific setup menu, choose **Debug Monitor**.
 5. Turn off the power to the Alpha PCI 164-266/300, then turn the power back on.
- B. Turn off the power to the Alpha PCI 164-266/300, remove the jumper from J1-25/26 (CONF11 on the module), then turn on the power to the Alpha PCI 164-266/300.

3.4 Software Configuration

3.4.3 Returning to ARC Firmware from the Debug Monitor

You can use one of the following methods to return to the Windows NT ARC firmware from the debug monitor:

- A. If you entered the debug monitor from the firmware using a firmware menu (described as choice A in Section 3.4.2) then use this procedure to return to the firmware.

The firmware contained in the serial ROM on your Alpha PCI 164–266/300 determines which firmware image is loaded from the flash ROM at power-up. The serial ROM firmware uses a value stored in the nonvolatile RAM of the real-time clock to determine which firmware image to load.

1. Use the following debug monitor command to select your operating system's firmware, by writing the value 1 to the TOY RAM (for Windows NT) : ¹

```
EB164> bootopt 1
```

```
O/S type selected: "The Windows NT Operating System"  
...Firmware type: "Windows NT Firmware"
```

To verify the selection:

```
EB164> bootopt
```

```
Predefined bootoptions are...
```

```
"0" "Alpha Evaluation Board Debug Monitor" "DBM"  
"1" "The Windows NT Operating System" "NT"  
"2" "OpenVMS" "VMS"  
"3" "Digital UNIX" "UNIX"
```

```
O/S type selected: "The Windows NT Operating System"  
...Firmware type: "Windows NT Firmware"
```

```
EB164>
```

Note

The Alpha PCI 164–266/300 does not support the OpenVMS operating system.

2. Turn off power to the Alpha PCI 164–266/300. Verify the presence of a jumper at J1–25/26 (see CONF11 on the module).

¹ The Alpha PCI 164–266/300 uses the same firmware as the Alpha EB164 evaluation board, so the firmware prompts appear as EB164>.

3.4 Software Configuration

3. Turn on the power to the Alpha PCI 164–266/300. After the power-up diagnostics are run, the chosen firmware's console boot menu appears on the graphics display.
- B. If you entered the debug monitor by turning off power and removing jumper J1-25/26 (described as choice B in Section 3.4.2), then use this procedure to return to the console firmware:
1. Turn off the power to the Alpha PCI 164–266/300, insert the jumper from J1-25/26 (CONF11 on the module).
 2. Turn on the power to the Alpha PCI 164–266/300. After the power-up diagnostics are run, the ARC console boot menu appears on the graphics display.
If the ARC console boot menu does not appear, check the output of COM1 for error messages and review your hardware configuration.

4

Functional Description

This chapter describes the operation of the Alpha PCI 164–266/300. The description introduces the DECchip 21171 ASIC support chipset and describes its implementation with the 21164 microprocessor, its supporting memory, and I/O devices. Figure 1–1 shows the Alpha PCI 164–266/300 major functional components.

Information, such as bus timing and protocol, found in other data sheets and reference documentation is not duplicated. See Appendix B for a list of supporting documents and order numbers.

Note

For detailed descriptions of bus transactions, chipset logic, and operation, refer to the *Alpha 21164 Microprocessor Hardware Reference Manual* and the *DECchip 21171 Core Logic Chipset Technical Reference Manual*.

For details of the PCI interface, refer to the *PCI System Design Guide*.

4.1 PCI Interrupts and Arbitration

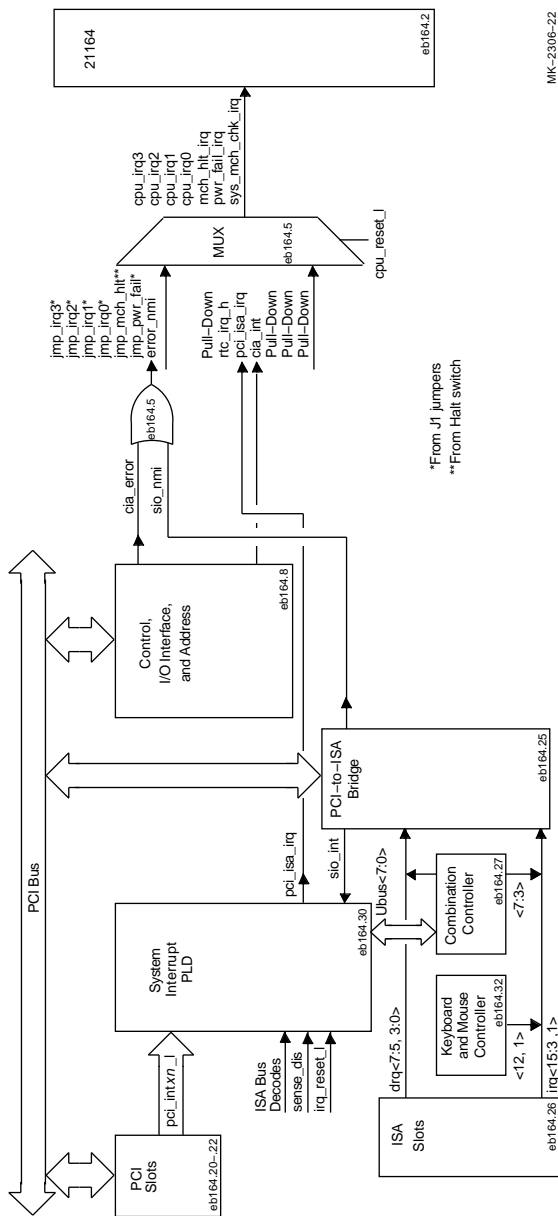
The following sections describe the Alpha PCI 164–266/300 interrupt and arbitration (arbiter) logic.

4.1.1 Interrupts

PCI-, ISA-, and CIA-generated interrupts are each described. Figure 4–1 shows the interrupt logic.

4.1 PCI Interrupts and Arbitration

Figure 4-1 Interrupt Logic



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4.1 PCI Interrupts and Arbitration

The PCI-to-ISA SIO bridge chip provides the functionality of two 8259 interrupt control devices. These ISA-compatible interrupt controllers are cascaded such that 14 external and two internal interrupts are available. The PCI interrupt acknowledge command should be used to read the interrupt request vector from the SIO.

However, the Alpha PCI 164–266/300 has more interrupt signals than the 14 external interrupts the SIO can handle. Therefore, all the ISA interrupts are sent to the SIO except for the two CIA interrupts, the time-of-year (TOY) interrupt, and the 16 PCI interrupts. They are sent to an external interrupt PAL. This PAL takes these interrupts, as well as an OR of the nonexistent memory (NMI) and error signals from the SIO, and generates **cpu_irq<3:0>**. During reset, **cpu_irq<3:0>** convey the system clocking ratios and delays, which are set by jumpers on J1.

Table 4–1 lists each system interrupt, its fixed interrupt priority level (IPL), and its Alpha PCI 164–266/300 implementation. Table 4–2 lists each SIO interrupt and its Alpha PCI 164–266/300 implementation.

Table 4–1 Alpha PCI 164–266/300 System Interrupts

21164 Interrupt	IPL ¹	Suggested Usage	Alpha PCI 164–266/300 Usage
cpu_irq<0>	20	Corrected system error	Corrected ECC error and sparse space reserved encodings detected by CIA
cpu_irq<1>	21	—	PCI and ISA interrupts
cpu_irq<2>	22	Interprocessor and timer interrupts	Time-of-year clock interrupt
cpu_irq<3>	23	—	Reserved
pwr_fail_irq	30	Powerfail interrupt	Reserved
sys_mch_chk_irq	31	System machine check interrupt	SIO NMI and CIA errors
mch_hlt_irq	—	Halt	Reserved

¹IPL = interrupt priority level (fixed)

4.1 PCI Interrupts and Arbitration

Table 4–2 PCI-to-ISA SIO Bridge Interrupts

Priority	Label	Controller	Internal/External	Interrupt Source
1	IRQ0	1	Internal	Internal timer 1
2	IRQ1	1	External	Keyboard
3–10	IRQ2	1	Internal	Interrupt from controller 2
3	IRQ8# ¹	2	External	Reserved
4	IRQ9	2	External	ISA bus pin B04
5	IRQ10	2	External	ISA bus pin D03
6	IRQ11	2	External	ISA bus pin D04
7	IRQ12	2	External	Mouse
8	IRQ13	2	External	Reserved
9	IRQ14	2	External	IDE
10	IRQ15	2	External	ISA bus pin D06
11	IRQ3	1	External	87312 combination controller
12	IRQ4	1	External	87312 combination controller
13	IRQ5	1	External	87312 combination controller
14	IRQ6	1	External	87312 combination controller
15	IRQ7	1	External	87312 combination controller

¹The # symbol indicates an active low signal.

Interrupt PLDs Function

The MACH210A PLD is an 8-bit I/O slave on the ISA bus at hex addresses 804, 805, and 806. This is accomplished by a decode of the three ISA address bits **sa<2:0>** and the three **ecas_addr<2:0>** bits.

Each interrupt can be individually masked by setting the appropriate bit in the mask register. An interrupt is disabled by writing a 1 to the desired position in the mask register. An interrupt is enabled by writing a 0. For example, bit <7> set in interrupt mask register 1 indicates that the INTB2 interrupt is disabled. There are three mask registers located at ISA addresses 804, 805, and 806.

An I/O read transaction at ISA addresses 804, 805, and 806 returns the state of the 17 PCI interrupts rather than the state of the masked interrupts. On read transactions, a 1 means that the interrupt source shown in Figure 4–2 has asserted its interrupt. The mask register can be updated by writing addresses 804, 805, or 806. The mask register is write-only.

4.1 PCI Interrupts and Arbitration

Figure 4-2 Interrupt and Interrupt Mask Registers

Interrupt and Interrupt Mask Register 1 (ISA Address 804h)

7	6	5	4	3	2	1	0
intb2	intb1	intb0	sio	inta3	inta2	inta1	inta0

Interrupt and Interrupt Mask Register 2 (ISA Address 805h)

7	6	5	4	3	2	1	0
intd2	intd1	intd0	intc3	intc2	intc1	intc0	intb3

Interrupt and Interrupt Mask Register 3 (ISA Address 806h)

7	6	5	4	3	2	1	0
RAZ	RAZ	RAZ	RAZ	RAZ	RAZ	RAZ	intd3

Notes: RAZ = Read-as-Zero, Read-Only
Interrupt Mask Register Is Write-Only

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4.1.2 Arbitration

Arbitration logic is implemented in the Intel 82378ZB Saturn I/O (SIO) chip. The arbitration scheme is flexible and software programmable. Refer to the Intel *82420/82430 PCIsset ISA and EISA Bridges* document for more information about programmable arbitration.

4.2 ISA Bus Devices

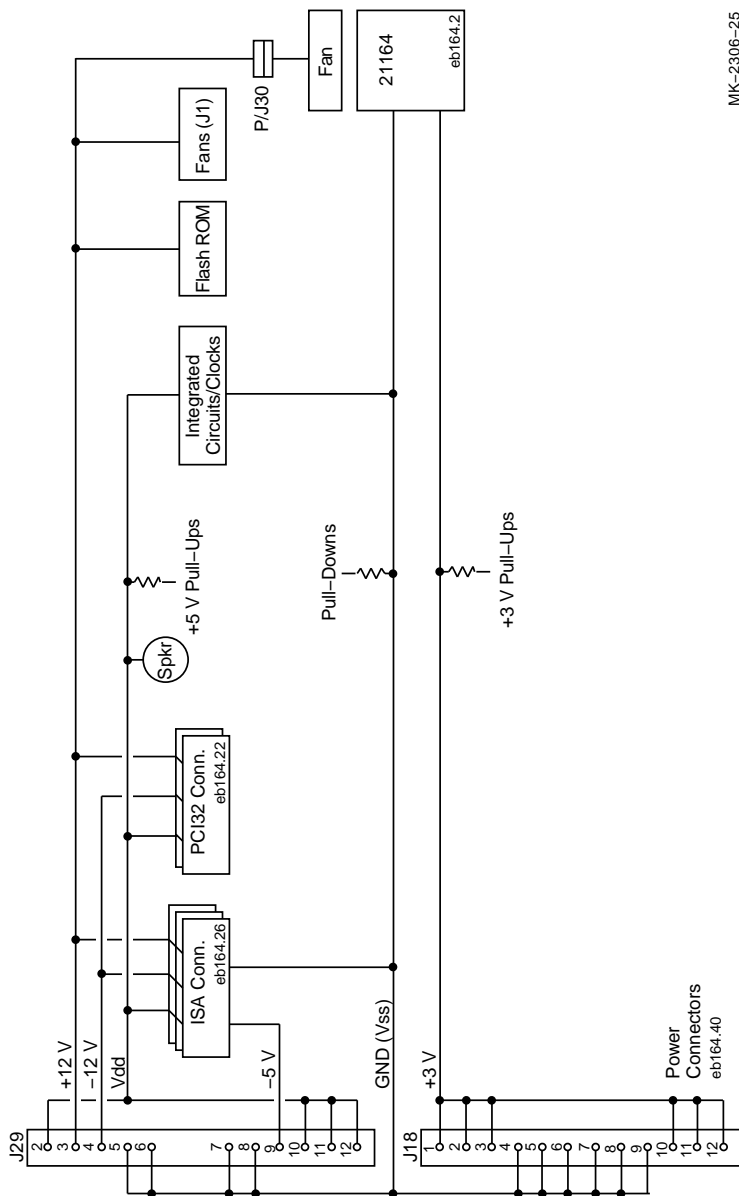
Two dedicated ISA expansion slots are provided in addition to the combination ISA/PCI slot. System support features such as serial lines, parallel port, integrated device electronics (IDE), and diskette controller are embedded on the module by means of an 87312 combination controller chip. Also shown is the utility bus (Ubus) with its system support devices.

4.3 dc Power Distribution

The Alpha PCI 164-266/300 derives its system power from a user-supplied PC power supply. The power supply must provide ± 12 V dc, ± 5 V dc, and +3.3 V dc. The dc power is supplied through power connectors J18 and J29. (See Figure 4-3.) Power is distributed to the board logic through dedicated power planes within the 6-layer board structure.

4.3 dc Power Distribution

Figure 4-3 dc Power Distribution



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4.3 dc Power Distribution

As shown in Figure 4-3, the +12 V dc, -12 V dc, and -5 V dc are supplied to ISA connectors J19, J20, and J21. The +12 V dc and -12 V dc are supplied to ISA connectors and PCI32 connectors J24 and J25. The +12 V dc is also supplied to the CPU fan connector J30, auxiliary fan connector pins on header J2, and to the flash ROM write-enable connector J14. +5 V (Vdd) is supplied to ISA connectors, PCI32 connectors and most of the board's integrated circuits. +3.3 V dc is supplied to the 21164 microprocessor.

4.4 PCI Devices

The Alpha PCI 164-266/300 uses the PCI bus as the main I/O bus for peripheral functions. The board implements the ISA bus as an expansion bus for system support functions and relatively slow peripheral devices.

The PCI bus supports multiplexed, burst mode, read and write transfers. It supports synchronous operation of between 25 MHz and 33 MHz. It also supports either a 32-bit or 64-bit data path with 32-bit device support in the 64-bit configuration. Depending upon the configuration and operating frequencies, the PCI bus supports anywhere between 100MB/s (25-MHz, 32-bit) to 264MB/s (33-MHz, 64-bit) peak throughput. The PCI bus provides parity on address and data cycles. Three physical address spaces are supported:

1. 32-bit memory space
2. 32-bit I/O space
3. 256-byte-per-agent configuration space

The bridge from the 21164 system bus to the 64-bit PCI bus is provided by the CIA chip. It generates the required 32-bit PCI address for 21164 I/O accesses directed to the PCI. It also accepts 64-bit double address cycles and 32-bit single address cycles. The 64-bit address support is subject to some constraints.

4.5 Flash ROM

4.5 Flash ROM

The flash ROM, sometimes called the system ROM, is a 1MB, nonvolatile, writable ROM. After the serial ROM (SROM) code initializes the Alpha PCI 164–266/300 system, the flash ROM code prepares the system for booting. The flash ROM headers, structure, and access methods are described here.

4.5.1 Special ROM Header

The SROM allows the system (flash) ROM to contain several different ROM images, each with its own header. The header informs the SROM where to load the image, and whether or not it has been compressed. The header is optional for system ROMs containing a single image. If the header does not exist, the complete 1MB system flash ROM is loaded and executed starting at physical address zero. Figure 4–4 shows the header content.

Figure 4–4 Special Header Content

31	0
Validation Pattern 5A5AC3C3	
Inverse Validation Pattern A5A53C3C	
Header Size (Bytes)	
Image Checksum	
Image Size (Memory Footprint)	
Decompression Flag	
Destination Address Lower Longword	
Destination Address Upper Longword	
Reserved<31:16>	Firmware ID<15:8> Header Rev<7:0>
Flash ROM Image Size	
Optional Firmware ID<31:0>	
Optional Firmware ID<63:32>	
Header Checksum (excluding this field)	

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4.5 Flash ROM

Table 4–3 describes each entry in the special header.

Table 4–3 Special Header Entry Descriptions

Entry	Description
Validation and inverse validation pattern	This quadword contains a special signature pattern used to validate that the special ROM header has been located. The pattern is 5A5AC3C3A5A53C3C.
Header size (bytes)	This longword provides the size of the header block, which varies among versions of the header specification. When the header is located, SROM code determines where the image begins based on the header size. Additional data added to the header is ignored by older SROM code. A header size of 32 bytes implies version 0 of the header specifications.
Image checksum	This longword is used to verify the integrity of the ROM.
Image size	The image size is used by the SROM code to determine how much of the system flash ROM should be loaded.
Decompression flag	The decompression flag informs the SROM code whether the ROM image was compressed. The SROM code contains routines that execute the decompression algorithm. Other compression and decompression schemes, which work independently from this scheme, may be employed.
Destination address	This quadword contains the destination address for the image. The SROM code loads the image at this address and begins execution.
Firmware ID	The firmware ID is a byte that specifies the firmware type. This information facilitates image boot options necessary to boot different operating systems.

Firmware Name	Firmware	
	Type	Description
Debug monitor	0	Alpha evaluation board debug monitor
Windows NT	1	Windows NT ARC firmware
Alpha SRM	2	Alpha System Reference Manual console

(continued on next page)

4.5 Flash ROM

Table 4–3 (Cont.) Special Header Entry Descriptions

Entry	Description
Header revision	The revision of the header specification used in this header. This is necessary to provide for changes to the header specification. Version 0 headers are identified by the size of the header (32 bytes).
Flash ROM image size	The flash ROM image size reflects the size of the image as it is contained in the flash ROM.
Optional firmware ID	This optional field can be used to provide additional firmware information such as firmware revision or a character descriptive string of up to 8 characters.
Header checksum	The checksum of the header. This is used to validate the presence of a header beyond the validation provided by the validation pattern.

4.5 Flash ROM

4.5.2 Flash ROM Structure

The Alpha PCI 164–266/300 loads and boots the first image (the debug monitor) if the BOOT_OPTION jumper (J1—25/26) is not installed.

If jumper J1—25/26 (BOOT_OPTION) is installed (see Figure 2–2), the Alpha PCI 164–266/300 reads the value at location 0x3F of the TOY RAM. The Alpha PCI 164–266/300 uses the value found there to determine which image will be selected (see Table 4–4). The selected image is loaded and executed.

Table 4–4 Flash ROM Image Selection

TOY RAM Value ¹	Firmware ID ²	Image Description
0x00	0	Evaluation board debug monitor firmware
0x01	1	Windows NT ARC firmware
0x02	2	Alpha SRM firmware (OpenVMS) ³
0x03	2	Alpha SRM firmware (Digital UNIX) ⁴
0x8 <i>n</i>	Not applicable	SROM code loads the <i>n</i> th image from flash ROM. If <i>n</i> =0, the SROM code loads the entire flash ROM contents. If <i>n</i> =1, 2, . . . , the SROM code loads the first image, second image, and so on.

¹Operating system type. Found at TOY RAM address 0x3F.

²Found in image header.

³The Alpha PCI 164–266/300 does not support OpenVMS.

⁴The current version of the Alpha PCI 164–266/300 does not support Digital UNIX.

If an image is specified and is not found, the Alpha PCI 164–266/300 loads the first image found in the flash ROM with a valid header. If no valid header is found, the entire 1MB flash image is loaded at address 0x00000000.

The following sequence of steps describes how to change the value stored in TOY RAM location 0x3F by using either the basic debug monitor commands or the debug monitor `bootopt` command.

4.5 Flash ROM

Changing TOY RAM Location 0x3F—Debug Monitor `bootopt` Command

Use the debug monitor `bootopt` command to change the value in location 3F. In the example shown here, the `bootopt` command is used to change the value in location 3F from 0 to 1:¹

```
EB164> bootopt ❶
Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"
O/S type selected: "Alpha Evaluation Board Debug Monitor"
...Firmware type: "DBM Firmware"
EB164> bootopt nt ❷
O/S type selected: "The Windows NT Operating System"
...Firmware type: "Windows NT Firmware"
EB164> bootopt ❸
Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"
O/S type selected: "The Windows NT Operating System"
...Firmware type: "Windows NT Firmware"
EB164>
```

- ❶ Use the debug monitor `bootopt` command to see the image choices and note which image is selected.
- ❷ Use the debug monitor `bootopt x` command to change the selected image from 0 to NT (1) The Alpha PCI 164–266/300 does not support OpenVMS. The current version of the Alpha PCI 164–266/300 does not support Digital UNIX.
- ❸ Use the debug monitor `bootopt` command to verify that the selected image has changed from 0 to the selected value.

¹ The Alpha PCI 164–266/300 uses the same firmware as the Alpha EB164 evaluation board, so the firmware prompts appear as EB164>.

4.5 Flash ROM

4.5.3 Flash ROM Access

The flash ROM can be viewed as two banks of 512KB each. At power-up the lower 512KB bank is accessed using the address range 86.FFF8.0000 to 86.FFFF.FFFF.

Setting address bit 19 (**flash_adr19**) allows you to access the higher 512KB of flash ROM. Write a 1 to the register at address 0x800 to set address bit 19. Manually deposit a 1 to address 0x800 or enter the following command from the debug monitor:

```
> wb 800 1
```

The address range for the higher bank is 86.FFF8.0000 to 86.FFFF.FFFF, the same as for the lower bank. Access is now to the higher bank and will continue until the Alpha PCI 164–266/300 is reset, or a 0 is written to the register at address 0x800.

Note

The write-enable jumper must be installed at J14—2/3 (see Figure 2–1 and Figure 2–2). This enables writing to the flash ROM.

5

Alpha PCI 164–266/300 Requirements, Power, and Parameters

This chapter describes the Alpha PCI 164–266/300 environmental requirements, power, and physical board parameters.

5.1 Power Requirements

The Alpha PCI 164–266/300 derives its main dc power from a user-supplied power supply. The board has a total power dissipation of 116 W, **excluding** any plug-in PCI and ISA devices. Table 5–1 lists the power requirement for each dc supply voltage.

The power supply must supply a **dcok** signal to the system reset logic.

Table 5–1 Power Supply dc Current Requirements

Voltage	Current ¹
+3.3 V dc	16.0 A
+5 V dc	10.0 A
–5 V dc	0 A
+12 V dc	1.0 A
–12 V dc	100.0 mA

¹Values indicated are for a fully populated Alpha PCI 164–266/300 system module excluding plug-in PCI and ISA devices, with a CPU clock speed of 266 MHz.

Caution: Fan Sensor Required

The 21164 cooling fan *must* have a built-in sensor that drives a signal low while the fan spins. The sensor is connected to Alpha PCI 164–266 /300 board connector J30.

5.1 Power Requirements

If the fan stops, the loss of the sensor signal puts the Alpha PCI 164–266/300 into a low power standby mode. This protects the Alpha PCI 164–266/300 under fan-failure conditions.

5.2 Environmental Requirements

The 21164 microprocessor is cooled by a small fan blowing directly into the chip's heat sink. The Alpha PCI 164–266/300 motherboard is designed to run efficiently using only this fan. Additional fans may be necessary depending upon cabinetry and I/O board requirements.

The Alpha PCI 164–266/300 is specified to run within the following environment:

Parameter	Specification
Operating temperature	10°C to 40°C (50°F to 104°F) ambient on the board
Storage temperature	–55°C to 125°C (–67°F to 257°F)
Relative humidity	10% to 90% with maximum wet bulb temperature 28°C (82°F) and minimum dew point 2°C (36°F)
Rate of (dry bulb) temperature change	11°C/hour \pm 2°C/hour (20°F/hour \pm 4°F/hour)

5.3 Physical Board Parameters

The Alpha PCI 164–266/300 board consists of a 6-layer printed-wiring board (PWB) with components mounted to side 1 only. The board is populated with integrated circuit packages together with supporting active and passive components. The Alpha PCI 164–266/300 is a standard, full-size PC AT board with the following dimensions:

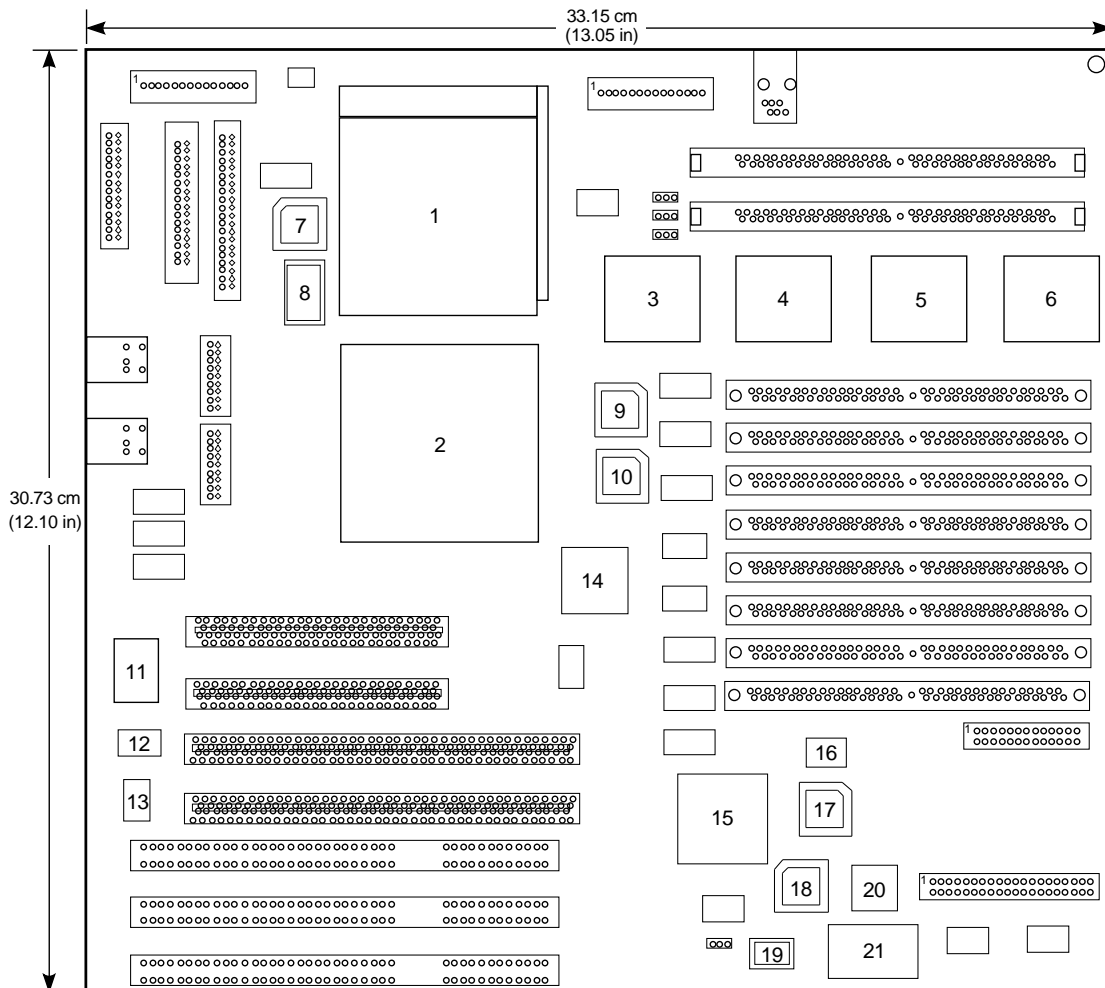
- Width: 30.73 cm (12.10 in)
- Length: 33.15 cm (13.05 in)
- Height: 6.00 cm (2.38 in)

The board can be used in certain desktop and deskside systems that have adequate clearance for the 21164 heat sink and fan. All ISA and PCI expansion slots are usable in standard desktop or deskside enclosures.

5.3 Physical Board Parameters

Figure 5–1 shows the board and component outlines, and identifies the major components. Table 5–2 lists the components. Refer to Chapter 2 for jumper and connector functions and locations.

Figure 5–1 Board Component Layout



MK-2306-32

5.3 Physical Board Parameters

Table 5–2 Board Component List

Locator Number	Component Number	Component Description
1	U42	Alpha 21164 microprocessor
2	U41	DECchip 21171-CA control, I/O interface, and address (CIA) chip
3	U32	DECchip 21171-BA data switch (DSW0) chip
4	U15	DECchip 21171-BA data switch (DSW2) chip
5	U10	DECchip 21171-BA data switch (DSW1) chip
6	U2	DECchip 21171-BA data switch (DSW3) chip
7	U50	TriQuint TQ2061 phase-locked loop (PLL) clock chip
8	U49	26.66-MHz clock oscillator
9	U31	Main memory row address strobe (RAS) PAL
10	U30	Main memory row address strobe (RAS) PAL
11	U58	National 87312 combination chip
12	U57	ISA clock frequency generator chip
13	X2	14.318-MHz clock oscillator
14	U33	Motorola 88PL117 phase-locked loop (PLL) system clock chip
15	U17	Intel 82378ZB PCI-to-ISA SIO bridge chip
16	U12	Xilinx serial ROM (initialization code) chip
17	U11	MACH210A interrupt request and PCI arbiter PAL
18	U13	Ubus decoder PAL
19	U14	Flash ROM chip
20	U7	Intel 8242 mouse and keyboard controller chip
21	U6	Dallas Semiconductor DS1287 time-of-year (TOY) clock chip

A

Supporting Vendor Products

To obtain components and accessories that are not included with your Alpha PCI 164–266/300 motherboard, Digital Equipment Corporation suggests the following vendors. In doing so, Digital does not warrant these components or guarantee that they will function in all configurations.

A.1 Products Not Included

The following products are not included in the Alpha PCI 164–266/300 motherboard kit.

- DRAM system memory—70 ns DRAM SIMMs (5 V, 72 pin)
1M × 36, 2M × 36, 4M × 36, 8M × 36, 16M × 36.

Note

The DRAM SIMMs must be $n \times 36$ SIMMs.

- Power supply—+3.3 V, ±5 V, ±12 V, available from:
 - Emacs Electronics USA, Inc.
1410 Gail Borden Place C-4
El Paso TX 79935
Phone: 915.599.2688
Part number: AP2-5300F (300 W)
 - Autec Power Systems
69 Moreland Rd
Simi Valley, CA 93065
Phone: 855.522.0888
Part number: PCB-3330-1010-D (339 W)

B

Technical Support and Additional Documentation

B.1 Technical Support

If you need technical support with your Alpha PCI Motherboard, contact your local Digital representative. Please provide your local representative with the model number and if possible a brief description of the problem you are encountering.

Additional technical documentation is available from Digital on the major Digital semiconductor components used on your PCI Motherboard. A complete list of these documents can be obtained from your local representative.

And be sure to visit Digital Equipment's home page at UIC:

<http://www.digital.com>

Select the Semiconductor InfoCenter for pointers to relevant technical documentation.

B.2 Ordering Third-Party Literature

B.2 Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI System Design Guide	PCI Special Interest Group 1-800-433-5177 (U.S.) 1-503-797-4207 (International) 1-503-234-6762 (FAX) http://www.teleport.com/~pc2/pcisigindex.shtml
PCI Local Bus Specification, Rev 2.1	PCI Special Interest Group (See previous entry.)
82420/82430 PCIsset ISA and EISA Bridges (includes 82378IB/ZB SIO) PN 290483	Intel Corporation Literature Sales P.O. Box 7641 Mt. Prospect, IL 60056 USA 1-800-628-8686 FaxBACK® Service 1-800-628-2283 BBS 1-916-356-3600 http://www.intel.com
UPI-41AH/42AH Universal Peripheral Interface 8-Bit Slave Microcontroller PN 210393	Intel Corporation (See previous entry.)
Flash Memory PN 210830	Intel Corporation (See previous entry.)
PC87311/PC87312 (SuperI/O II/III) Floppy Disk Controller with Dual UARTs, Parallel Port, and IDE Interface PN 11362	National Semiconductor Corporation 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052 USA 1-800-272-9959 http://www.national.com
Hardware Compatibility List	Contact Microsoft's Customer Service representatives at 1-800-426-9400, or access CompuServe Information Systems in Library 1 of the WINNT forum (GO WINNT) or Library 17 of the MSWIN32 forum (GO MSWIN32).

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