d i g i t a l ™

B2012-Series CPU Module Installation

EK–B2012–IN.A01

September 1993

This document illustrates the installation of the B2012 CPU module.

S2351

B2012

B2012 CPU Module

B2012 Overview

Description	The DEC 4000 AXP CPU is based on the DECchip 21064 microprocessor, a CMOS-4 superscalar, superpipelined implementation of the Alpha AXP architecture. DEC 4000 backup cache is a 4-MB direct-mapping physical write-back cache. The CPU supports the "snooping" protocol to allow for a dual-processor implementation.
Voltage	+5 V and +3.3 V
Current	+5 V: 13 A and +3.3 V: 14.5 A
Clock Speed	190 MHZ
Temperature	5°C (41°F)–35°C (98°F) (operational)
Relative humidity	10%–90%
Power	47.8 W (max)

Order number

B2012 CPU module	KN431–AA

Documentation

DEC 4000 AXP Technical Manual	EK–KN430–TM

————————— **Note** —————————

If you upgrade to a dual-processor system, both CPUs must have an identical clock speed rating.

Figure 1   B2012 CPU Module

Slot 0
Slot 1

Clock
Distribution
Connector

System
Bus
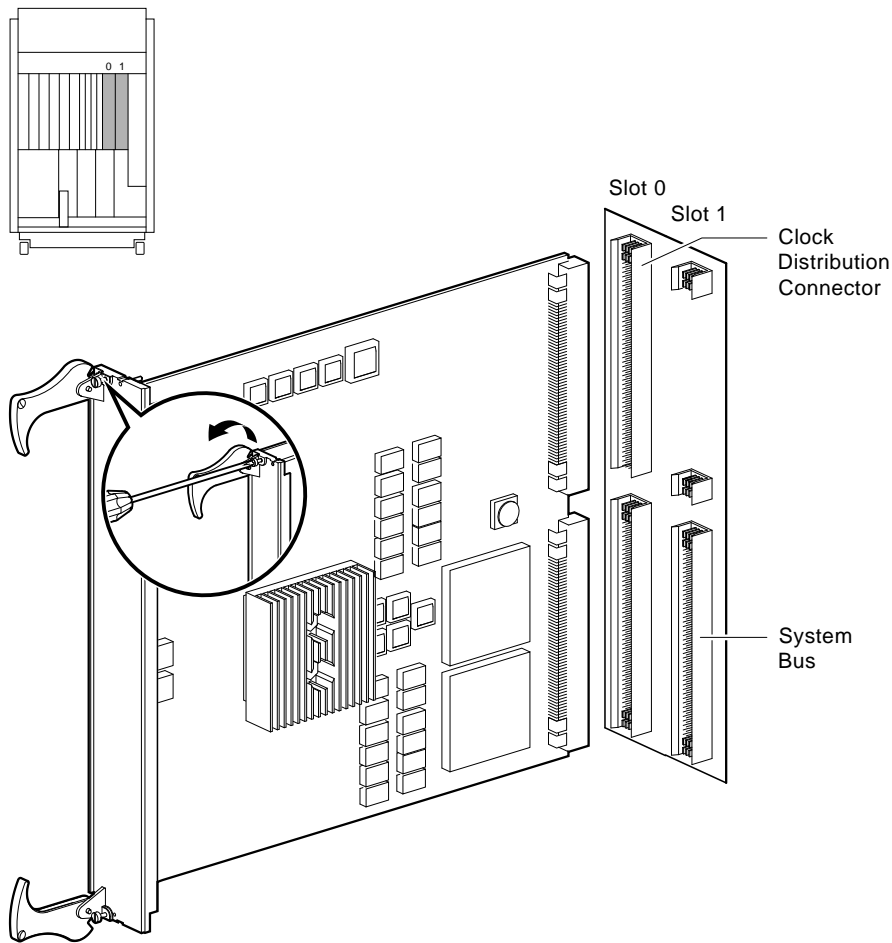
1 Insert first CPU into slot 0.

2 For SMP (symmetric multiprocessing) insert second CPU into slot 1.

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