Memory Channel

Service Information

Order Number: EK–PCIMC–SV. A01

This information is for field service engineers. It includes maintenance and service information for PCI Memory Channel subsystems and instructions for removal and replacement of field-replaceable units (FRUs).

Compaq Computer Corporation
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Intended Audience

This manual is written for field service engineers and self-maintenance customers who require information to maintain and service Memory Channel cluster hardware.

Document Structure

This manual uses a structured documentation design. Topics are organized into small sections for efficient reference. Each topic begins with an abstract. You can quickly gain a comprehensive overview by reading only the abstracts. Next is an illustration or example, which also provides quick reference. Last in the structure are descriptive text or instructions.

This manual has four chapters and two appendixes, as follows:

- **Chapter 1, Field-Replaceable Units,** gives specifications, maintenance, and removal and replacement information on the field-replaceable units and the rackmount option.
- **Chapter 2, Configuration Requirements,** describes hardware, firmware, and software requirements.
- **Chapter 3, Troubleshooting,** tells how to proceed if problems arise, and provides basic information on error log information, DECevent, and Memory Channel registers.
- **Chapter 4, Memory Channel Subsystem Configurations and DECevent,** displays cluster configuration and DECevent error reporting samples.
- **Appendix A, Updating Firmware,** explains how to run the Loadable Firmware Update (LFU) Utility.
- **Appendix B, Running the MC Exerciser,** describes how to run the Memory Channel Exerciser, used to provide online verification of the MC hardware.

NOTE: No hardware from earlier Memory Channel versions will interchange with this version.

Conventions

The AlphaServer 2100 console output is used as the default console in examples. Changes for other supported systems' consoles are noted only when the output varies considerably from the default example. For additional information on your systems' consoles, refer to your system user's guides.

All references to AlphaServer 8X00 systems also apply to GS 60/140 systems.

For More Information

Memory Channel Hardware Documentation

P/N	Title
EK–PCIMC–UG	*Memory Channel User's Guide*
EK–CCMFB–IN	*Memory Channel Installation Card*

Online Documentation Related to Memory Channel Systems

Address or URL	Information
http://www.digital.com/info/alphaserver/products.html or ftp://ftp.digital.com/pub/Digital/Alpha/systems/	Click on the system of your choice; then click on "docs/" and select the desired item.
http://ftp.digital.com/pub/Digital/Alpha/firmware or ftp://ftp.digital.com/pub/Digital/Alpha/firmware	Firmware information for the AlphaServer systems
http://www.digital.com/info/SOC	*DIGITAL Systems and Options Catalog* Hardware ordering and configuration guide
http://www.service.digital.com/DECevent/	DECevent home page.

DIGITAL UNIX Documentation Related to Memory Channel

P/N	Title
AA–ROJAC–TE	*TruCluster Software™ Products Release Notes*
AA–R88GA–TE	*TruCluster Software Products Hardware Configuration*
AA–R88HA–TE	*TruCluster Software Products Software Installation Guide*
AA–R88JA–TE	*TruCluster Software Products Administration Guide*
AA–R88KA–TE	*TruCluster Production Server Software Datagram Service Application Programming Interfaces Guide*
AA–QL8BC–TE	*TruCluster Production Server Software Application Programming Interfaces Guide*
AA–QTN4C–TE	*TruCluster Production Server Software Memory Channel Application Programming Interfaces Guide*
EK–BA350–CG	*StorageWorks™ Solutions*: *Configuration Guide*

OpenVMS Documentation Related to Memory Channel

P/N	Title
AA–Q28LB–TK	*Guidelines for OpenVMS Cluster Configurations*
AA–QSBTB–TE	*OpenVMS Version 7.1 Release Notes*

DECevent Documentation

P/N	Title
AA–QAA6C–TE	*DECevent Release Notes for DIGITAL UNIX Users*
AA–QU68B–TE	*DECevent Release Notes for OpenVMS*
AA–QAA4C–TE	*DECevent Analysis and Notification Utility for DIGITAL UNIX User and Reference Guide*
AA–Q73LD–TE	*DECevent Analysis and Notification Utility for OpenVMS User and Reference Guide*
AA-QAA5C–TE	*DECevent Event Management Utility for DIGITAL UNIX Installation Guide*
AA-Q73JD–TE	*DECevent Event Management Utility for OpenVMS Installation Guide*
AA–QAA3C–TE	*DECevent Translation and Reporting Utility for DIGITAL UNIX User and Reference Guide*
AA–Q73KD–TE	*DECevent Translation and Reporting Utility for OpenVMS User and Reference Guide*
AA–QE26C–TE	*The DECevent Graphical User Interface User's Guide*

Chapter 1

Field-Replaceable Units

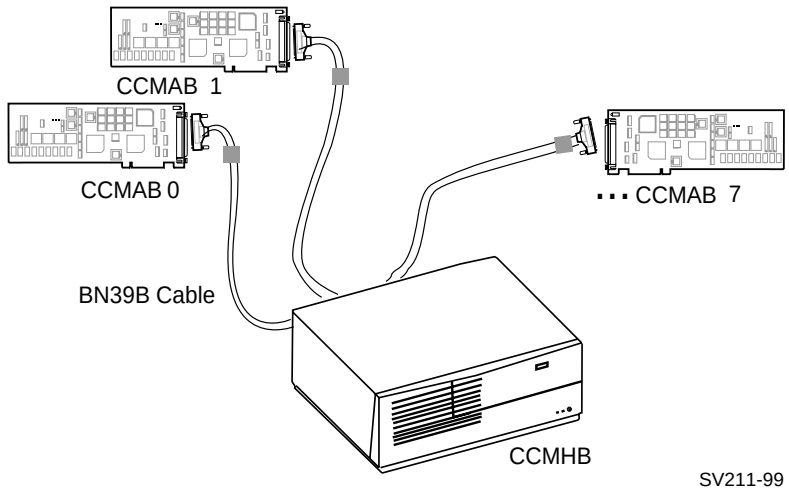
This chapter describes Memory Channel (MC) field-replaceable units (FRUs), their order numbers, location, and specifications. It describes the diagnostic LEDs and removal and replacement of each FRU. Sections include:

- Overview
- MC Field-Replaceable Units
- CCMAB Adapter
- Memory Channel Cables
- CCMFB Fiber Optics Module
- CCMHB Hub
- Hub Panel Removal
- CCMLB Linecard
- Hub Fan Assembly
- Hub Power Cords

1.1 Overview

A basic Memory Channel configuration consists of AlphaServer systems, with a CCMAB adapter module installed on each system's PCI bus, connected to a CCMHB hub by a link cable. When using fiber optics, the CCMFB optics module and BN34R fiber optics cable are used.

Figure 1-1 Sample Memory Channel Configuration

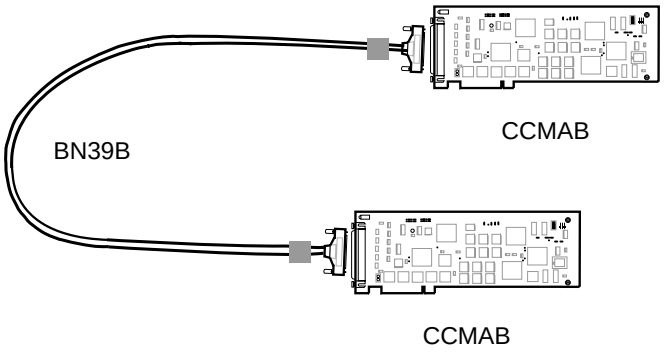


The CCMAB adapter is a standard PCI module supported on servers with PCI. The black BN39B link cable connects each CCMAB adapter to the CCMHB hub in standard hub mode or to another CCMAB in virtual hub mode. The cable is available in 1, 4, and 10 meter (3.3, 13.1, and 32.8 foot) lengths and is a 100-wire cable (50 twisted pairs). For greater separation, a fiber optics cable is used. Two CCMFB fiber optics modules, a BN34R fiber optics cable, and two BN39B-01 link cables are used when connecting two nodes using fiber optics.

Figure 1-1 shows a typical Memory Channel configuration, utilizing a hub which is required for three or more systems in an MC cluster. It consists of several AlphaServer systems, each having a CCMAB adapter module installed on the system's PCI bus. Each adapter module is connected to the CCMHB hub by a BN39B link cable.

With two AlphaServer systems, a virtual hub (no hub) configuration is also possible by connecting the two CCMAB adapters directly to each other using the link cable (see Figure 1-2).

Figure 1-2 Virtual Hub Memory Channel Configuration



NOTE: No hardware from earlier Memory Channel versions will interchange with the latest Memory Channel hardware; that is, the CCMAA adapter cannot be used with the CCMAB adapter.

For more information:

Section 1.3, CCMAB Adapter
TruCluster Software Hardware Configuration
Guidelines for OpenVMS Cluster Configurations

1.2 MC Field-Replaceable Units

Memory Channel FRUs include the CCMAB adapter module, the link cable, and the CCMHB hub. The hub has FRUs inside (linecards and fan assembly). Fiber optics FRUs are the CCMFB optics module and BN34R fiber optics cable.

Figure 1-3 Memory Channel FRUs

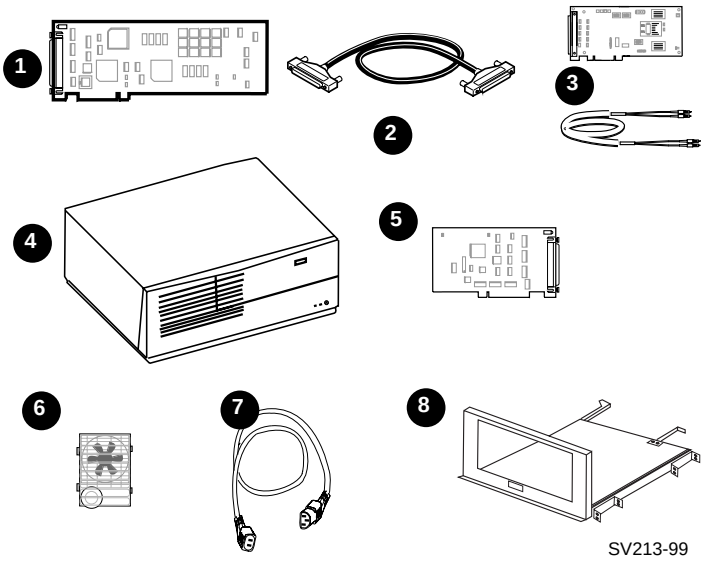


Table 1-1 Memory Channel Field-Replaceable Units

Part Number	Option Number	Description
54-24962-01	CCMAB-AA	PCI adapter module
17-04563-01, -02, -03	BN39B-01, -04, -10	Link cable (1m, 4m, 10m)
54-24970-01	CCMFB-AA	Fiber optics module
17-04773-06, -09	BN34R-10, -31	Fiber optics cable (10m, 31m)
	CCMHB-AA	Hub (with four linecards)
	CCMHB-BA	(without linecards)
54-24966-01	CCMLB-AA	Hub linecard
70-32987-01		Fan assembly
2T-MAVRK		Rackmount Installation Kit
See Section 1-10 for the hub power cord numbers		Power cord

The removal and replacement procedures for the following FRUs comprise the remainder of this chapter:

❶ CCMAB adapter module

❷ Link cable

❸ CCMFB fiber optics module and cable

❹ CCMHB hub

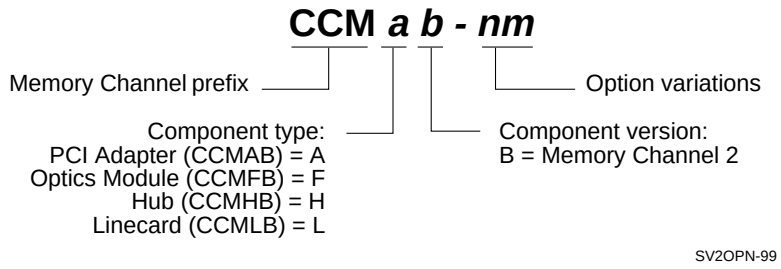
❺ CCMLB linecard

❻ Hub fan assembly

❼ Hub power cord

Installation procedures for the 2T-MAVRK-AA rackmount kit (see ❽, Figure 1-3) are included with the kit.

Memory Channel Option Nomenclature

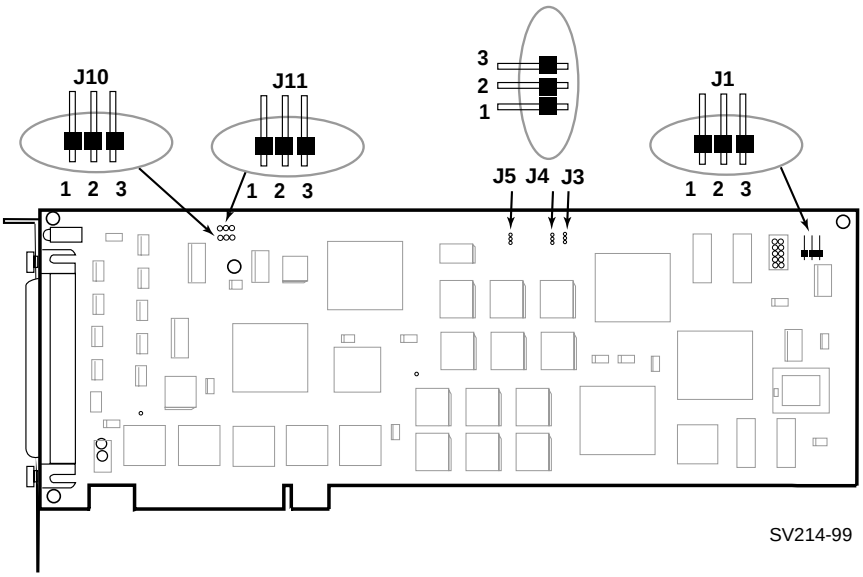


1.3 CCMAB Adapter

1.3.1 CCMAB Jumpers

The CCMAB adapter has jumpers that must be set for hub mode, Memory Channel window and page size, 8X00 mode, and fiber optics.

Figure 1-4 CCMAB Jumpers



The CCMAB adapter ships with the following default settings:

- J1, Hub mode – Standard hub mode
- J3, Window size – 128MB
- J4, Page size – 8KB
- J5, 8X00 – 8X00 mode NOT selected
- J10, Optics clock enable – No fiber
- J11, Fiber enable – No fiber

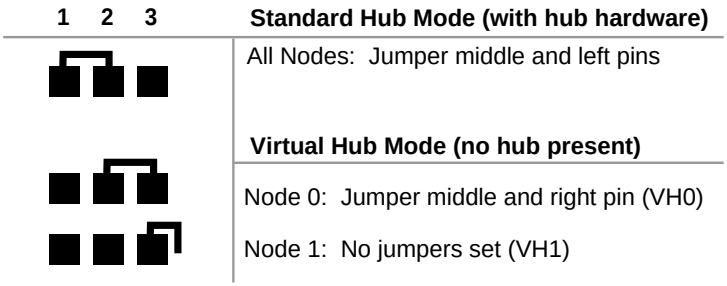
Whenever you install a CCMAB adapter, you must set the jumpers for your configuration. The jumper numbers are on the adapter next to the jumpers.

1. Use an ESD ground strap when handling the modules.
2. Unpack the CCMAB PCI adapter.
3. Hold the adapter by the edges and set it on a secure, static-free surface.
4. Set the CCMAB jumpers for your configuration. If you are installing a redundant configuration under DIGITAL UNIX, both the first and second CCMAB adapters are jumpered the same way within a system.

J1 - Hub Mode

J1 is used to configure the module for one of three modes of operation depending on the cluster configuration. In virtual hub (VH) mode, two systems are cabled together directly without a hub. In VH mode, the J1 jumper on one CCMAB adapter must be set to Virtual Hub Node 0 (VH0) and the J1 jumper on the other CCMAB to Virtual Hub Node 1 (VH1). The J1 setting determines the node ID.

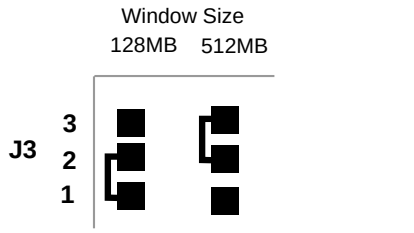
If the module is connected to a CCMHB hub (standard hub mode), then it is configured in standard (STD) mode and all CCMAB adapters must have the same J1 jumper configuration. If you are upgrading from a two-node virtual hub to a standard mode configuration with a CCMHB, check and change the J1 jumpers on all CCMAB adapters.



SV2J1-99

J3 - Window Size

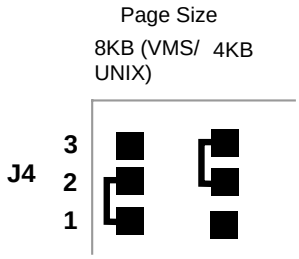
This jumper selects either 128MB or 512MB MC address space. The size must be determined by jumper, since firmware that allocates PCI address space does so at power-up. OpenVMS uses the 128MB setting and DIGITAL UNIX uses the 512 MB setting.



SV2J3-99

J4 - Page Size

Selects the size of each MC page. All nodes in the cluster must be configured with the same page size. Present operating systems use 8KB; 4KB is reserved for future use. This jumper may be overridden by the Module Configuration Register (MODCFG).



SV2J4-99

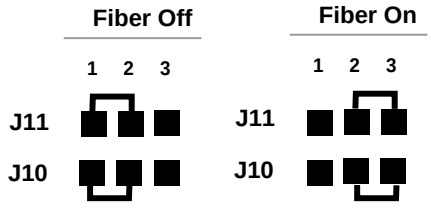
J5 - AlphaServer 8X00 Mode

Increases the maximum sustainable bandwidth of 8X00 platforms by 10MB/s. If this jumper is inadvertently set in any other platform, the maximum sustainable bandwidth will decrease by 10MB/s. This jumper may be overridden by the Module Configuration Register (MODCFG) in case it is not installed properly.

SV2J5-99

J10, J11 - Fiber Optics Mode

J10 (Optics Clock Enable) and J11 (Fiber Enable) must both be set the same way – *on* for fiber – when the CCMFB fiber optics module and BN34R fiber cable (see Section 1.5) are used.



SV2J1011-99

1.3.2 CCMAB Adapter PCI Slot Position

Determine the PCI slot for the CCMAB adapter carefully. Systems with multi-channel Memory Channel hardware must have the first module (mca0) in the lower slot position.

Table 1-2 CCMAB PCI Slot Position by System

AlphaServer	CCMAB Slot Position
800/1000	Any PCI slot
1000A	Highest three PCI slots (11, 12, 13)
2000 family	See Table 1-3
4100	OpenVMS: Any PCI slot DIGITAL UNIX 4.0F with TruCluster V1.6: Any PCI slot
8200/8400	In a DWLPA OpenVMS: DWLPA or DWLPB or both DIGITAL UNIX: Both CCMAB adapters must be on the same DWLPA/DWLPB, with mca0 in the lower slot. Note that the DWLPA has a 256MB mapping register. Each CCMAB takes 128 MB of mapping register space, so if you install two CCMABs in a DWLPA, mapping register space will all be allocated.

Figure 1-5 Bulkheads for AlphaServer 2000/2100/2100RM/2100A

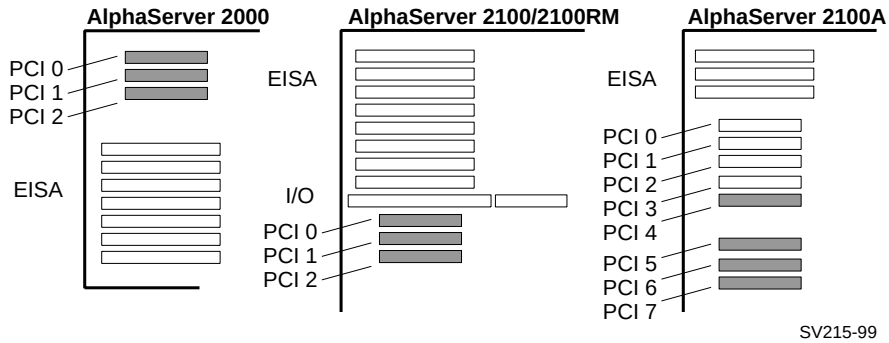


Table 1-3 Console ID and Bulkhead Numbers for PCI Slots

AlphaServer	2000	2100	2100 RM	2100A
PCI 0	Slot 1	Slot 6	Slot 8	Do not install CCMAB
PCI 1	Slot 2	Slot 7	Slot 7	Do not install CCMAB
PCI 2	Slot 3	Slot 8	Slot 6	Do not install CCMAB
PCI 3	—	—	—	Do not install CCMAB
PCI 4	—	—	—	Slot 6
PCI 5	—	—	—	Slot 7
PCI 6	—	—	—	Slot 8
PCI 7	—	—	—	Slot 9

1 Determine PCI slot position in each system

For DIGITAL UNIX in a multi-channel configuration, the first CCMAB adapter (to be mca0) must be in the lowest available slot the console sees. The second CCMAB (mcb0) adapter must be in the higher slot. This must be consistent across all members of the MC cluster. All mca0's are attached to one hub, all mcb0's are attached to the second hub.

For OpenVMS in a multi-channel configuration, the only restriction is that both CCMABs from one system may not be attached to the same hub. The placement of the CCMABs in the PCI bus relative to their hub connection is not important to OpenVMS.

Software Device ID Number to Physical Slot Number

Console software device IDs are mapped to physical slot locations within specific platforms in the following tables. In several cases, the numbers will be the same. "J" numbers, which refer to the slot indicators printed on the motherboard, are given when possible. The "J" number is positioned on the motherboard, next to the physical slot connector.

Definitions

- Software Device ID – the number defined by design engineering at platform design. The console derives the number by reading PCI address lines that are hardwired on a slot by slot basis.
- Physical Slot Number – viewed by physical positioning and PCI bus specifications.
- "J" number – refers to the physical slot labels etched on the motherboard.

AlphaServer 800

Software Device ID	Physical Slot and J Number
Slot 11	PCI 1 J9
Slot 12	PCI 2 J10
Slot 13	PCI 3 J11
Slot 14	PCI 4 J12

AlphaServer 1000

Software Device ID	Physical Slot
Slot 11	PCI 11
Slot 12	PCI 12
Slot 13	PCI 13

AlphaServer 1000A

Software Device ID	Physical Slot and J Number
Slot 11	PCI 11 J9
Slot 12	PCI 12 J10
Slot 13	PCI 13 J11
Slot 1	PCI 1 J12
Slot 2	PCI 2 J13
Slot 3	PCI 3 J14
Slot 4	PCI 4 J15

AlphaServer 1200

Software Device ID	Physical Slot and J Number
IOD0 Slot 2	PCI 0 – Slot 2 J26
IOD0 Slot 3	PCI 0 – Slot 3 J25
IOD0 Slot 4	PCI 0 – Slot 4 J24
IOD1 Slot 2	PCI 1 – Slot 2 J23
IOD1 Slot 3	PCI 1 – Slot 3 J22
IOD1 Slot 4	PCI 1 – Slot 4 J21

AlphaServer 2000

Software Device ID	Physical Slot and J Number
Slot 6	PCI 0 J16
Slot 7	PCI 1 J17
Slot 8	PCI 2 J18

AlphaServer 2100 – Pedestal

Software Device ID	Physical Slot and J Number
Slot 6	PCI 0 J25
Slot 7	PCI 1 J24
Slot 8	PCI 2 J23

AlphaServer 2100 – Rackmount

Software Device ID	Physical Slot
Slot 8	PCI 0
Slot 7	PCI 1
Slot 6	PCI 2

AlphaServer 2100A

Software Device ID	Physical Slot and J Number
Slot 2 *	PCI 0 J32
Slot 3 *	PCI 1 J31
Slot 4 *	PCI 2 J30
Slot 5 *	PCI 3 J28
Slot 6	PCI 4 J27
Slot 7	PCI 5 J25
Slot 8	PCI 6 J23
Slot 9	PCI 7 J22
*** = Do not install MEMORY CHANNEL**	

AlphaServer 4100

Software Device ID	Physical Slot and J Number
IOD0 Slot 2	PCI 0 – Slot 2 J4
IOD0 Slot 3	PCI 0 – Slot 3 J5
IOD0 Slot 4	PCI 0 – Slot 4 J6
IOD0 Slot 5	PCI 0 – Slot 5 J7
IOD1 Slot 2	PCI 1 – Slot 2 J8
IOD1 Slot 3	PCI 1 – Slot 3 J9
IOD1 Slot 4	PCI 1 – Slot 4 J10
IOD1 Slot 5	PCI 1 – Slot 5 J11

AlphaServer 4000

Software Device ID	Physical Slot and J Number
IOD0 Slot 2	PCI 0 – 2 J4
IOD0 Slot 3	PCI 0 – 3 J5
IOD0 Slot 4	PCI 0 – 4 J6
IOD0 Slot 5	PCI 0 – 5 J7
IOD1 Slot 2	PCI 1 – 2 J8
IOD1 Slot 3	PCI 1 – 3 J9
IOD1 Slot 4	PCI 1 – 4 J10
IOD1 Slot 5	PCI 1 – 5 J11

AlphaServer 4000 (Continued)

Software Device ID	Physical Slot and J Number
IOD2 Slot 2	PCI 2 – 2 J3
IOD2 Slot 3	PCI 2 – 3 J4
IOD2 Slot 4	PCI 2 – 4 J5
IOD2 Slot 5	PCI 2 – 5 J6
IOD3 Slot 2	PCI 3 – 2 J7
IOD3 Slot 3	PCI 3 – 3 J8
IOD3 Slot 4	PCI 3 – 4 J9
IOD3 Slot 5	PCI 3 – 5 J10

AlphaServer 8200/8400

Software Device ID	Physical Slot and J Number
Slot 0	PCI 0 J3
Slot 1	PCI 1 J5
Slot 2	PCI 2 J6
Slot 3	PCI 3 J8
Slot 4	PCI 4 J10
Slot 5	PCI 5 J12
Slot 6	PCI 6 J13
Slot 7	PCI 7 J15
Slot 8	PCI 8 J17
Slot 9	PCI 9 J19
Slot A	PCI 10 J20
Slot B	PCI 11 J22

2 Change the CCMAB adapter extender plate, if necessary

The adapter comes with a straight extender installed. Some systems require changing the extender to the angled bracket. Look at the physical slot you have chosen and change the extender plate if necessary.

1.3.3 CCMAB Adapter Removal and Replacement

The CCMAB adapter(s) are installed in the PCI slots as described in Section 1.3.2. Placement is checked using console commands. The adapter's end connector is attached to the PCI bulkhead. The BN39B cable is attached to the CCMAB connector.

Example 1-1 Check Adapter Placement

```
P00>>> init                                    ❶
VMS PALcode V1.20-3, OSF PALcode V1.22-1

starting console on CPU 0
Testing Memory bank 0
Testing Memory bank 1
Configuring Memory Modules
probing hose 0, PCI
probing PCI-to-EISA bridge, bus 1
bus 0, slot 0 -- ewa -- DECchip 21040-AA
bus 0, slot 1 -- pka -- NCR 53C810
bus 1, slot 6 -- vga -- Compaq Qvision
bus 0, slot 6 -- pkb -- DEC KZPSA
bus 0, slot 7 -- mca -- DEC PCI MC             ❷
bus 0, slot 8 -- mcb -- DEC PCI MC             ❷
AlphaServer 2100 Console V5.2-54, built on Aug 28 1998 at
19:58:46
```

Removal

To remove the CCMAB adapter, follow directions in your system owner's manual for removing and replacing PCI adapters. Use a ground strap when handling the module, and hold the module by the edges.

Replacement

If you are installing a redundant configuration, label each end of the cables with the system and adapter they connect (for example, "Node 1/mca0" and "Node 1/mcb0"). This labeling will save you time with checking for crossed rails as well as any future maintenance of the cluster.

1. Unpack the CCMAB PCI adapter and put it on a secure, static-free surface.
2. Set the CCMAB jumpers for your configuration (see Section 1.3.1). If you are installing a redundant configuration under DIGITAL UNIX, both the first and second CCMAB adapters are jumpered the same way within a system.
3. Line up the adapter with the system's connector and push down into position. Secure the CCMAB adapter at the backplane, tightening the screw to hold it. This connects the module to ground.
4. Attach the link cable (see Section 1.4) to the CCMAB adapter at the bulkhead. If you are using fiber optics, install and cable the CCMFB fiber optics module (see Section 1.5).
5. With a multi-channel configuration, install and cable the second adapter.
6. Replace system panels.

Check placement on PCI bus

❶ Power up each system. Enter an **init** command to start power-up tests. With an AlphaServer 8200/8400, enter the **show config** command to check the CCMAB adapter placement.

❷ Check the placement of the CCMAB adapters. Both should report to the console here. Check that the adapter designated mca0 resides in the lower slot. Check placement against system requirements (see 1 above).

1.3.4 Power Up and Check Status LEDs

After cabling the CCMAB adapters (Section 1.4), power up each system. Check the status LEDs on the CCMAB adapters and the CCMLB linecards, if present.

Two LEDs on each CCMAB adapter and CCMLB linecard show the connection status (see Figures 1-6 and 1-7). Use these LEDs to verify all nodes and hubs are properly connected (only the left LED on all CCMAB adapters is amber and both LEDs on all CCMLB linecards are amber). If no LEDs are lit, check the system for power. If only the right LED is amber, there is no connection to the remote system or hub. Verify power is on at the remote system, that all cables are properly inserted, and that the jumper settings on CCMAB adapters and CCMLB linecards are correct.

Figure 1-6 Checking CCMAB Status LEDs

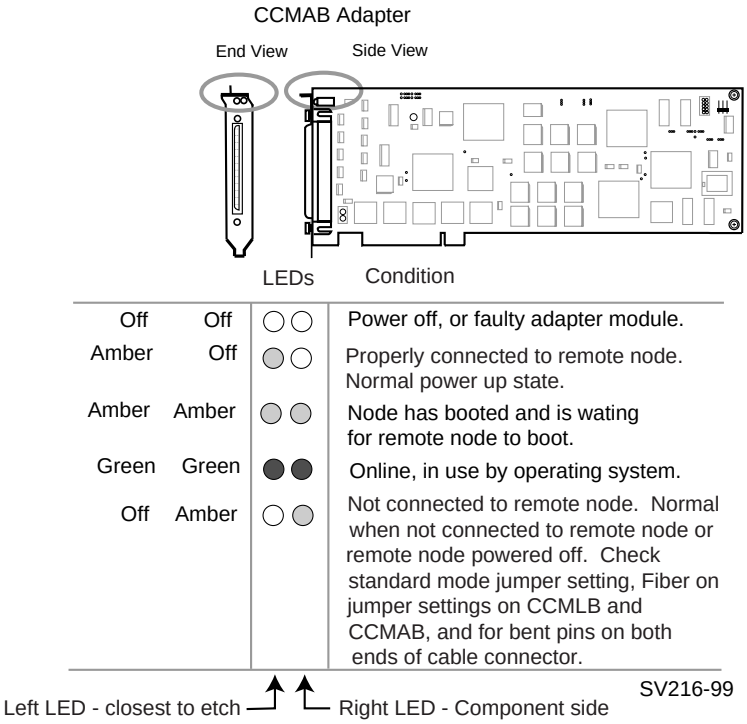
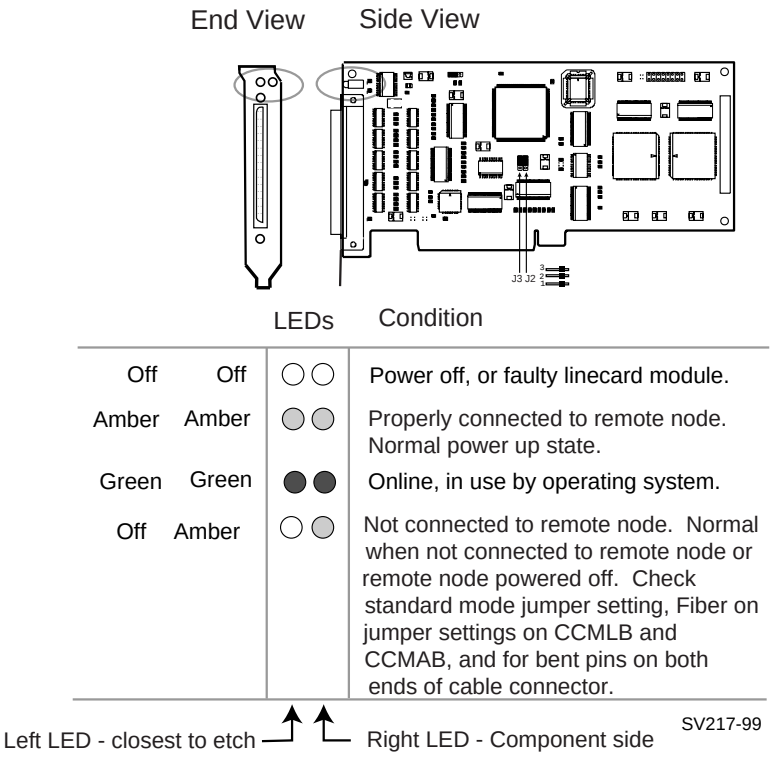


Figure 1-7 Checking CCMLB Status LEDs



1.4 Memory Channel Cables

The BN39B is a copper cable with two 100-pin connectors. It connects two CCMAB adapters when in virtual hub mode or connects the CCMAB adapter to the hub when in standard hub mode. For system separation greater than 10 meters (32.8 ft), the BN34R fiber optics cable is used.

Figure 1-8 Memory Channel Cables

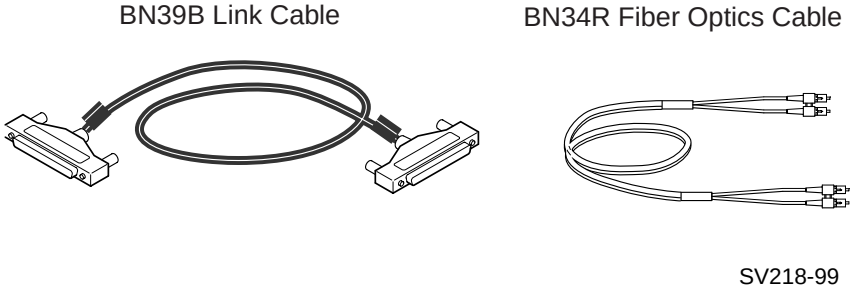


Table 1-4 BN39B Link Cable

Part Number	Option Number	Description
17-04563-01	BN39B-10	10-meter (32.8-ft) cable
17-04563-02	BN39B-04	4-meter (13.1-ft) cable
17-04563-03	BN39B-01	1-meter (3.3-ft) cable used with the CCMFB fiber optics module

Each connector, provided with embedded screws, has 100 pins (50 twisted pairs). Install the connectors carefully. Bent pins will cause errors. The cluster may run with bent pins initially, but errors from bent pins may show up later.

To check cable connection, or to install snugly, rock the connector gently from side to side, not up and down.

Removal

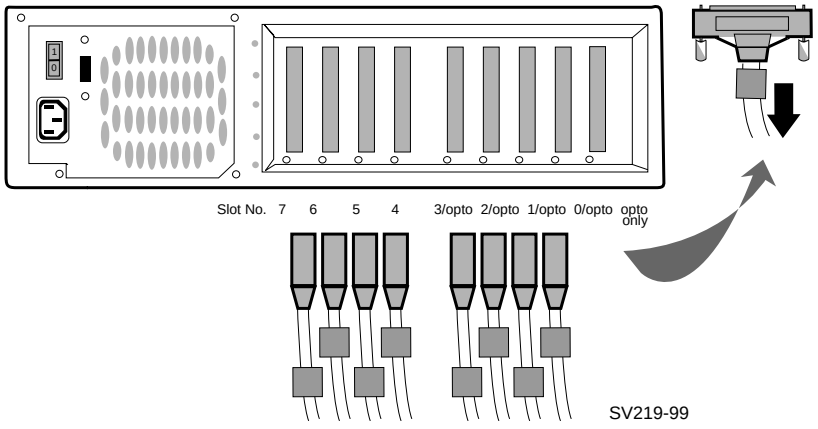
If you are installing a redundant configuration, label each end of the cables with the system and adapter they connect (for example, "Node 1/mca0" and "Node 1/mcb0"). This labeling will save you time with checking for crossed rails as well as any future maintenance of the cluster.

The cable has two identical 100-pin dual in-line keyed connectors.

One connector is always attached to a CCMAB adapter in a system. The second connector is attached to a CCMLB linecard in the hub (standard mode) or to another CCMAB adapter (virtual hub mode) in a second system. The ferrite sleeves of cables may interfere with each other. In this case, slide one or both sleeves slightly, keeping as close to the connectors as possible, until they fit (see Figure 1-9).

1. Loosen the embedded thumbscrews by turning counterclockwise.
2. Gently pull the cable connector from the receptacle on the back of the hub.

Figure 1-9 Cabling BN39B to the CCMHB Hub



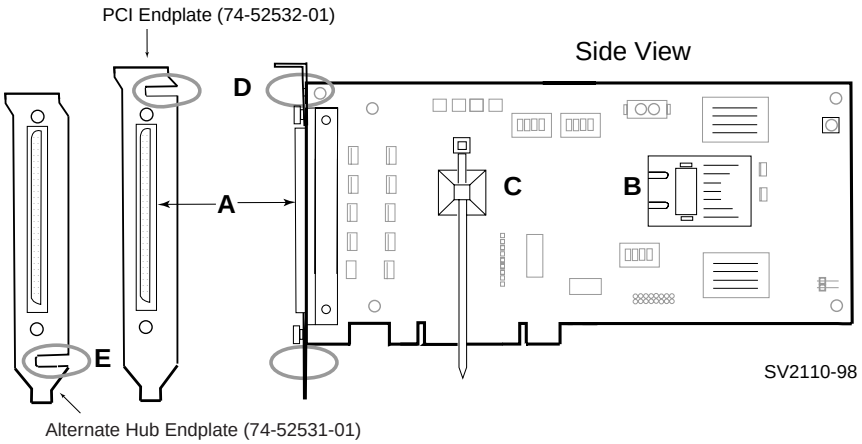
Replacement

To replace, reverse steps 1 and 2 above.

1.5 CCMFB Fiber Optics Module

To obtain a greater separation between Memory Channel systems than that provided by the BN39B cable, fiber optics are used. The CCMFB fiber optics module is used in conjunction with the BN39R fiber optics cable.

Figure 1-10 CCMFB Fiber Optics Module



The CCMFB fiber optics module occupies one slot in a system's PCI or in a system's CCMHB hub. Two CCMFB modules are required to connect two nodes. The CCMFB module has two connectors:

- a 100-pin connector (see A, Figure 1-10) on the end of the module, for the 1-meter black BN39B link cable
- a SC duplex connector on the front of the transceiver (see B) into which the BN34R fiber cable is plugged

Each CCMFB fiber optics module in a system's PCI is connected to the CCMAB adapter with the BN39B-01 cable. Each CCMFB fiber optics module in a CCMHB hub is connected to a CCMLB linecard with the BN39B-01 cable. The CCMFB converts the BN39B signal and transmits it over the BN34R fiber cable to the other system's CCMFB. There it is converted and transmitted over another BN39B-01 to the second system's CCMAB.

The CCMFB comes with two endplates. The one attached is used when the module is installed in a system's PCI. The alternate endplate (74-52531-01) is used when installing the CCMFB in a hub (see Figure 1-10).

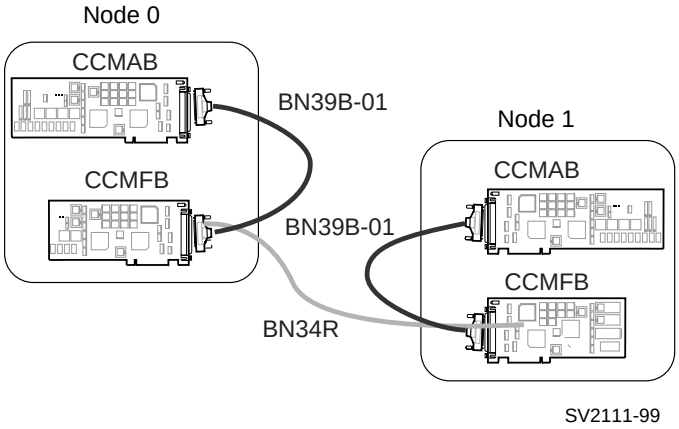
The BN34R fiber optics cable is available in two lengths: 10 meters (32.8 feet) and 31 meters (101.7 feet). Its Simplex connectors, which are clipped together, are inserted into the transceiver on the CCMFB (see B, Figure 1-10) and the cable is tie-wrapped (see C) to provide strain relief.

CAUTION: Handle fiber optics cables with care. Avoid sharp bends to avoid damage to the fiber. The minimum recommended bend radius for the BN34R cable is 5.08 cm (2 inches). Do not touch the unprotected plug ends. Any standard optical cleaning kit is acceptable to clean fiber cables.

1.5.1 Virtual Hub Mode with Fiber Optics

A virtual hub configuration using fiber optics requires two CCMAB adapters, two CCMFB fiber optics modules, two BN39B-01 link cables, and one BN34R fiber optics cable.

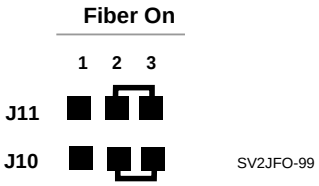
Figure 1-11 Virtual Hub with Fiber Optics Modules and Cable



NOTE: The CCMFB fiber module only gets power from the PCI slot. Software does not see the CCMFB in the slot, so there are no slot restrictions.

For a virtual hub configuration, install one CCMFB in each system's PCI card cage, as follows:

1. Perform an orderly shutdown of the systems.
2. Thread one end of the BN39R fiber optics cable through the PCI bulkhead slot.
3. Thread the optics cable through the slot near the top of the endplate (see D in Figure 1-10). Remove the cable tip protectors and insert the Simplex connectors into the transceiver housing until they click in place. Tie-wrap the cable to the module (see C).
4. Seat the CCMFB fiber optics module firmly into the PCI backplane and secure the module to the PCI card cage with the mounting screw.
5. Attach the 1-meter BN39B link cable from the CCMAB adapter to CCMFB connector A.
   NOTE: Make certain CCMAB jumpers J10 and J11 are set to Fiber On (jumper pins 2-3).



6. Repeat steps 1 through 5 at remote node, or second system.
7. Power up and verify the systems. Run **mc_cable** at the console prompt. A response from all nodes signifies a complete connection. A "no response" indicates the possibility of a bad cable or incorrect jumper settings.

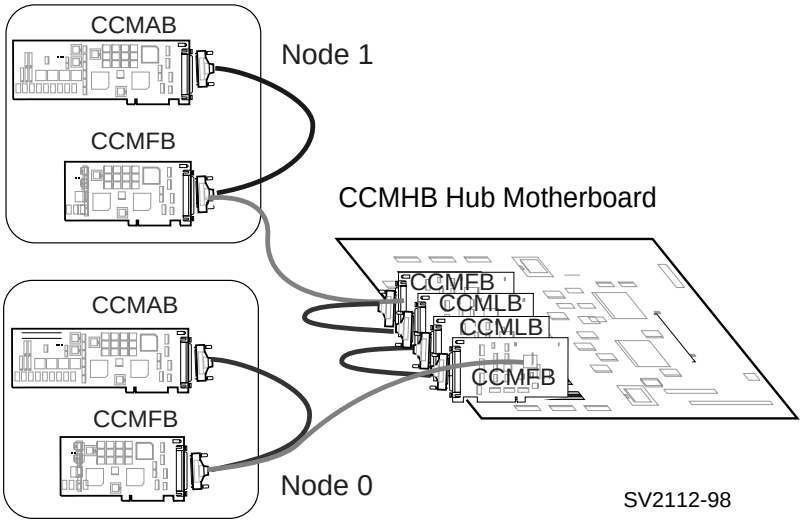
For more information:

MEMORY CHANNEL Installation Card

1.5.2 Standard Hub Mode with Fiber Optics

Each node in a standard hub configuration with fiber requires one CCMFB module, one BN39B-01 link cable, and one BN39R fiber optics cable. Each BN39R connects to a CCMFB in the CCMHB hub (Section 1.6), which in turn connects via a second BN39B-01 link cable to a CCMLB linecard (Section 1.8).

Figure 1-12 Standard Hub with Fiber Optics Modules and Cables



NOTE: CCMFB modules can only be installed in the first five hub slots: opto only, 0/opto, 1/opto, 2/opto, and 3/opto.

CCMFB Module Removal

1. Perform an orderly shutdown of the systems. Remove the hub's top panel (Section 1.7) or the PCI card cage cover.
2. Detach the BN39B-01 link cable connecting the CCMFB module to the CCMAB adapter or the CCMLB linecard.
3. Remove the mounting screw which secures the CCMFB module to the PCI card cage or hub. Lift the CCMFB module from the PCI backplane or hub.
4. Remove the tie-wrap (see C, Figure 1-10) holding the BN34R fiber optics cable to the module and gently unplug the Simplex connectors from the CCMFB transceiver housing (see B). Lift the fiber optics cable out of the module endplate slot (see D).
5. Pull the BN34R fiber optics cable out through the PCI bulkhead or hub slot and remove.

Replacement

1. Perform an orderly shutdown of the systems and remove the PCI card cage or hub cover. Thread one end of the BN39R fiber optics cable through the PCI bulkhead slot or hub slot.
2. Thread the optics cable through the slot near the top of the endplate when installing in a node (see D, Figure 1-10). When installing in a hub, replace the attached endplate with the alternate endplate, and thread the optics cable through the slot (see E, Figure 1-10) at the bottom of the endplate. Remove the cable tip protectors and insert the Simplex connectors into the transceiver housing (see B) until they click in place. Tie-wrap (see C) the cable to the module.
3. Seat the CCMFB fiber optics module firmly into the PCI backplane or the hub motherboard and secure the module with the mounting screw.
4. Attach the 1-meter BN39B link cable from the CCMFB connector A to the CCMAB adapter or CCMLB linecard.
   NOTE: Make certain CCMAB jumpers J10 and J11(see Section 1.3.1) and CCMLB jumpers J2 and J3 (see Section 1.8) are set to Fiber On.
5. Repeat steps 1 through 5 at remote node or second system.
6. Replace PCI card cage and hub covers and power up and verify the systems.
7. Run **mc_cable** to assure a response from each node.

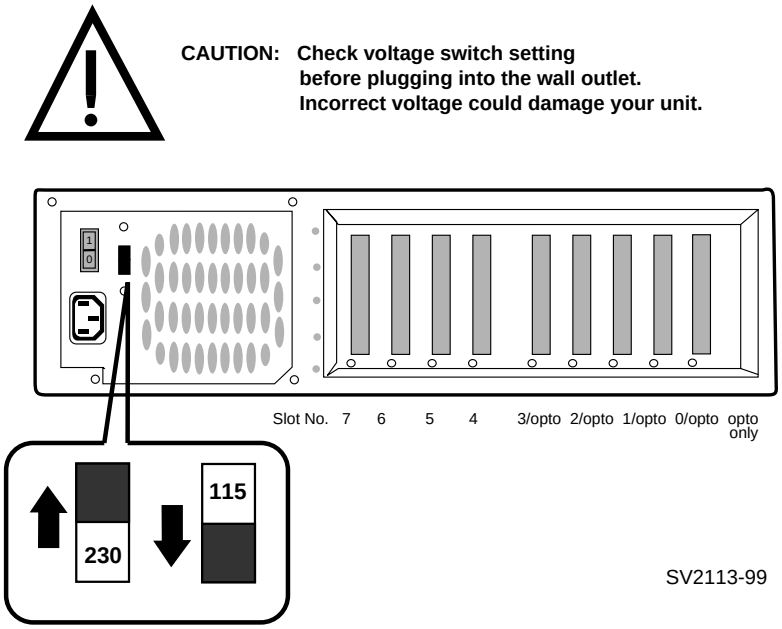
For more information:

Memory Channel Installation Card

1.6 CCMHB Hub

The CCMHB hub can hold up to eight linecards. The hub has three FRUs: linecard (Section 1.8), optics module (Section 1.5), and fan assembly (Section 1.9). The hub is also available with no linecards (CCMHB-BA).

Figure 1-13 Hub, Rear View



NOTE: You must set the voltage selection switch before powering up the hub.

Removal

1. Push in the power button to power down the hub. Unplug and remove the power cord.
2. Note the position of each cable, label, and disconnect. The cabled slot position determines node ID of cluster members. Returning cables and linecards to the same slots helps with troubleshooting, introducing fewer variables.

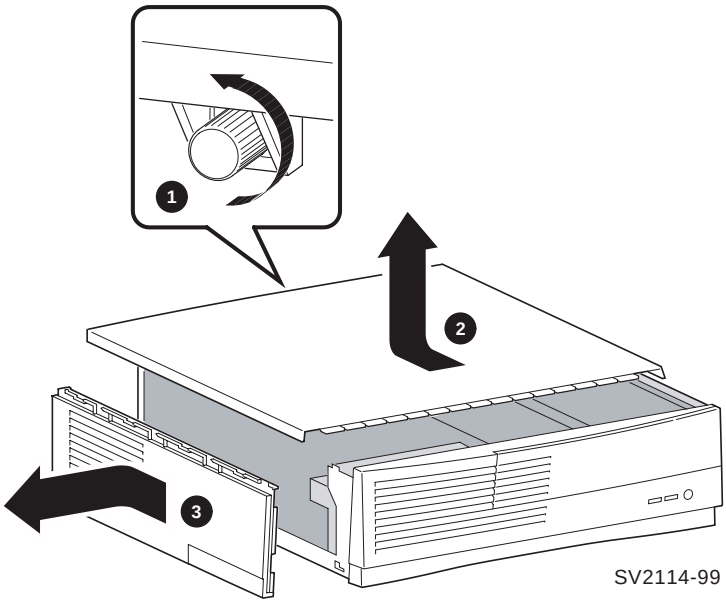
Replacement

1. Unpack and place the new hub.
2. Install CCMLB linecards and/or CCMFB fiber modules and connect cables to their previous position.
3. Check voltage selection switch and set to correct voltage.
4. Attach the power cord to the hub and plug it in.
5. Turn the hub on by pushing in the power button on the front of the hub control panel.

1.7 Hub Panel Removal

You may have to remove one or more panels to access the hub components.

Figure 1-14 Removing Hub Panels



Removal

1. Push in the power button to power down the hub. Unplug the power cord from the wall outlet.
2. Locate the thumbscrew ❶, at the rear of the hub, that fastens the top cover to the rear panel in the upper center of the back panel. Loosen the thumbscrew by turning it counterclockwise. You may need to use a flathead screwdriver.
3. Brace the back panel of the box with one hand while pulling the top cover toward you ❷ with the other. The lip of the cover is useful to gain a firm grip. It is a tight fit, so it may require a strong pull.
4. Lift cover off and set aside.
5. Remove the left side panel ❸ (when viewed from the front) to access the item you are servicing, by pressing the metal tab located near the front of the panel on the inside surface. While keeping the tab depressed, slide the panel towards the rear of the system unit and slightly outward, away from the enclosure.
6. Finally, the CD tray is removed by squeezing in the metal tabs at rear. Slide the CD tray to the rear and lift out.

Replacement

1. To replace the side panel, align the four guide pins with the four slots in the hub frame. Holding the unit steady, push the panel in and slide it forward until it clicks and locks in place.
2. To replace the top panel, seat the top panel on the hub with the edge 2 inches from the front. Holding the unit steady, push the back of the panel in with force until the clips catch and hold.
3. Secure the panel by tightening the thumbscrew.

1.8 CCMLB Linecard

Eight CCMLB linecards (P/N 54-24966-01) can be installed in the hub. Each linecard has two diagnostic LEDs visible from the rear of the hub. Jumpers J2 and J3 must be set for fiber when fiber optics are used. Linecards can be installed in any hub slot except the "opto only" slot.

Figure 1-15 CCMLB Linecard

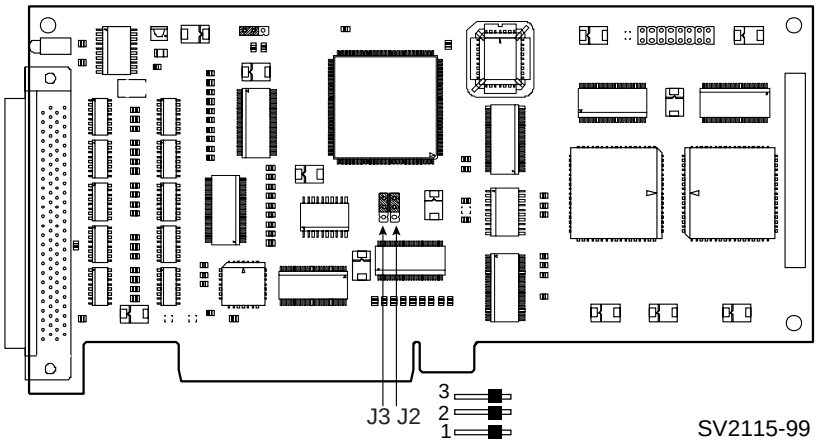
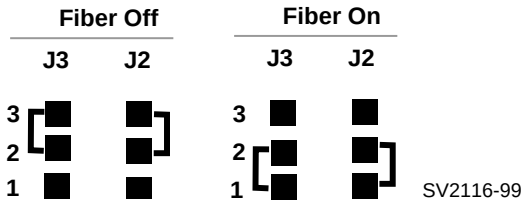


Figure 1-16 CCMLB Fiber Jumpers



Removal

1. Power down the hub and remove the hub's top panel (see Section 1.7).
2. Note the position and label the cable connected to the linecard and disconnect. Return the cable to the same slot; position determines node ID of cluster members.
3. Remove the mounting screw that secures the linecard to the card cage.
4. Remove the linecard by pulling it straight up and out of the slot connector.

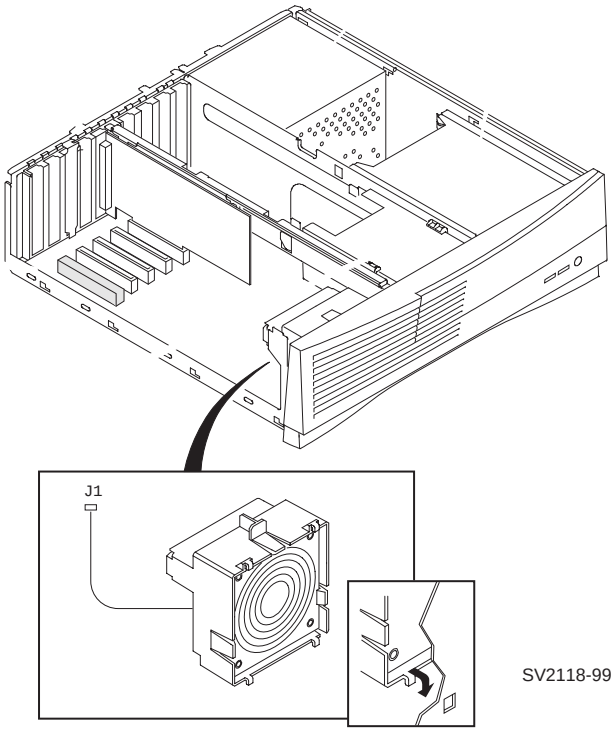
Replacement

1. Make certain linecard jumpers J2 and J3 are set properly. The default setting is fiber off.
2. Install the new linecard in the same slot. Seat it firmly in the connector on the motherboard, or it may not function correctly.
3. Secure the linecard to the card cage with the mounting screw.
4. Reconnect the cable and reinstall the top panel.
5. Power up and check the LEDs (see Figure 1-7).

1.9 Hub Fan Assembly

The fan (P/N 70-32978-01) is located behind the control panel and is secured to the system unit by tabs. The fan unit is 4 inches (10.2 cm) high, 4 inches (10.2 cm) wide, and 2-3/4 inches (7.0 cm) deep.

Figure 1-17 Hub Fan Assembly Replacement



The fan assembly may need replacement if:

- The fan fails to turn with the hub powered on.
- The linecards fail repeatedly; may be due to overheating, caused by a faulty fan unit.

NOTE: If the fan has been replaced and there are still problems, the power supply may be faulty.

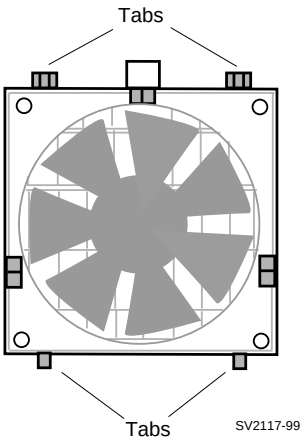
Removal

1. Power down the hub and remove the top panel (see Section 1.7).
2. Remove the side panel (see ❸, Figure 1-14) by pushing in the metal tab located on the inside near the front bezel. Slide the panel back, as shown in the directions located on the inside of the front panel.
3. Disconnect the power cord from the power supply.
4. Disconnect the power lead from the J1 connector on the motherboard.
5. If there is a tie-wrap holding the fan assembly, cut the tie-wrap and lift the fan assembly up approximately ¼ inch to release the four tabs that hold the fan in the frame and carefully pull it straight back away from the hub.

Replacement

1. Insert the four tabs of the fan assembly (see Figure 1-18) into the slots on the front frame and press the fan in until it is firm against the frame and down so all four tabs lock.
2. Connect the fan power lead to the J1 connector on the motherboard.
3. Replace any linecards you removed for access.
4. Replace the side panel by aligning the four guide pins with the four slots in the hub frame. Holding the hub steady, push the panel in and slide it forward until it clicks and locks in place.
5. Replace the top panel and power cord, and power up the hub.

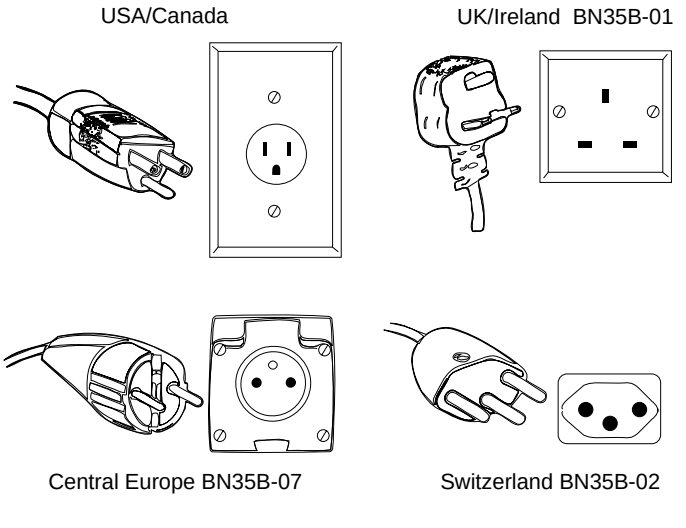
Figure 1-18 Hub Fan Assembly



1.10 Hub Power Cords

The hub ships with the power cord assigned to the country of destination. Figure 1-19 illustrates several hub power cords and their receptacles.

Figure 1-19 Hub Power Cords and Receptacles



All CCMHB-AA hubs ship with a BN35A-01 (North American) power cord, which will be redundant in areas that do not use this type of cord.

Table 1-5 lists the hub power cord for various countries.

Table 1-5 Hub Power Cords

Name	Part No.	Country	Alternates
BN35B-08	17-04364-08	Australia/ New Zealand	BN25P-2E/17-00198-12
BN35B-07	17-04364-07	Central Europe	BN03A-2E/17-00199-17
BN35B-06	17-04364-06	Denmark	
BN35B-03	17-04364-03	Egypt/India	BN22X-2E/17-00456-14
BN35B-05	17-04364-05	Israel	BN22M-2E/17-00457-14
BN35B-04	17-04364-04	Italy	BN19M-2E/17-00364-18
BN35T-02	17-04364-09	Japan	
BN35A-01	17-04357-01	North American	
BN35B-02	17-04364-02	Switzerland	BN04A-2E/17-00210-11
BN35B-01	17-04364-01	United Kingdom/ Ireland	BN19B-2E/BN26D-2E 17-00209-18, -19

Chapter 2

Configuration Requirements

This chapter describes Memory Channel system and software requirements. Sections include:

- System Configuration Requirements
- Operating System Requirements
- Console Error Messages

2.1 System Configuration Requirements

Console firmware for all systems must be at 5.0 Rev or higher. Also, some AlphaServer 2000/2100s require upgrades to support Memory Channel.

2.1.1 AlphaServer 800/1000/1000A Requirements

- Runs OpenVMS or DIGITAL UNIX operating systems.
- For the AlphaServer 1000A, CCMAB adapters must be in PCI slots 11, 12, and 13, the top three slots.

2.1.2 AlphaServer 2000/2100 Requirements

- Check your system for Memory Channel readiness as shown in Example 2-1.

Example 2-1 Checking the AlphaServer 2000/2100 for Readiness

```
P00>>> examine -b econfig:20008  ❶
econfig:             20008 04    ❷
```

❶ At the console prompt, enter **examine -b econfig:20008**.

❷ If a hexadecimal value of **04** or greater is returned, your I/O module supports Memory Channel.

If your system is not hardware-ready for Memory Channel and you install MC hardware and power up, console error message #1 will result (see Section 2.3). If a value of less than four is displayed, the system requires a hardware upgrade to support Memory Channel. The customer must order the required upgrade (see Table 2-1). Install the upgrade and proceed with installation.

Table 2-1 AlphaServer 2000/2100 Upgrades

AlphaServer	Order	to Upgrade	to Rev
2000	H3095-AA	B2111-AA backplane	H or higher
2100	H3096-AA	B2110-AA standard I/O module	L or higher

2.1.3 AlphaServer 2100A Requirements

- CCMAB adapter must be installed in one of the bottom four slots (see Figure 1-5). CCMAB adapters may not be installed in slots 0 through 3 or at power-up Memory Channel console error message #3 will result (see Section 2.3).

2.1.4 AlphaServer 4000/4100 Requirements

Under DIGITAL UNIX V4.0F with TruCluster Software V1.6

- For a single-channel configuration, the CCMAB adapter may be in any PCI slot.
- For a redundant configuration, the second CCMAB adapter must be on the same PCI bus as the first adapter, and in a higher slot number than the first adapter.

Under OpenVMS Version 7.1-1H2 or higher

- The CCMAB adapter(s) may be in any PCI slot.

2.1.5 AlphaServer 8200/8400 Requirements

- In a DWLPA, CCMAB adapters must be installed in PCI slots 0 through 7. No slot restrictions in the DWLPB.
- Under DIGITAL UNIX with multi-channel configurations, both CCMAB adapters must be in the same DWLPA/DWLPB card cage.
- Under OpenVMS with multi-channel configurations, only one CCMAB adapter may be in a DWLPA. You may have two CCMABs in a DWLPB, one in a DWLPA and one in a DWLPB, or one CCMAB in each of two DWLPAs.

2.1.6 Additional AlphaServer Requirements

For a current list of all supported systems, refer to the *DIGITAL Systems and Options Catalog.* Check your Memory Channel release notes for any additional requirements.

2.2 Operating System Requirements

Using console commands, check that MC diagnostic commands are supported in each system console. If they are not, update the console firmware.

2.2.1 DIGITAL UNIX Requirements

- Version 4.0F and TruCluster V1.6.
- When installing the DIGITAL UNIX TruCluster Software, each system must have a KZPSA SCSI adapter and shared SCSI devices.
- Unique SCSI ID, cable length limitations, and required slots are described in the TruCluster Software *Hardware Configuration* guide.

2.2.2 OpenVMS Requirements

- Version 7.1-1H2 or higher.
- Each system must have an adapter (CI, DSSI, SCSI) for booting a system disk. The expected configurations are a shared-SCSI bus, or a CI device with HSJ disk servers.

For more information:

Section 1.3, CCMAB Adapter
TruCluster Software *Hardware Configuration*
Guidelines for OpenVMS Cluster Configurations

2.3 Console Error Messages

At power-up, the console checks the hardware revision levels of the system required for MC clusters. If the system hardware does not support MC clusters, the console will report one of three error messages.

Example 2-2 Error Messages at Power-Up

```
①
*****************************************************
** Memory Channel hardware requirement ERROR  # 1    **
** See release notes, or Memory Channel User's Guide **
*****************************************************


②
*****************************************************
** Memory Channel hardware requirement ERROR  # 2    **
** See release notes, or Memory Channel User's Guide **
*****************************************************


③
*****************************************************
** Memory Channel hardware requirement ERROR  # 3    **
** See release notes, or Memory Channel User's Guide **
*****************************************************
```

Internal test of MC module logic is not done during power-up.

① **For AlphaServer 2000/2100:** An upgrade is needed; see Table 2-1.

② **For AlphaServer 8200/8400:** Check that the CCMAB is in DWLPA/DWLPB slots 0 through 7.
If the error message persists, an upgrade is needed.

③ **For AlphaServer 2100A:** Check your CCMAB modules.
They must be installed before the bridge, in the bottom four slots.

The **show configuration** console command can be used to confirm that the CCMAB modules are reporting to the system console. The **show version** command reports the installed console firmware revision level.

The MC diagnostics, **mc_cable** and **mc_diag**, check most of the logic of the MC hardware. These two diagnostics are invoked only at the system console and do not execute during power-up. See Section 4.2, Troubleshooting with mc_diag, and Section 4.3, Troubleshooting with mc_cable, in your *Memory Channel User's Guide.*

The diagnostics check the cables (see Section 4.4, Cable Troubleshooting, of your *Memory Channel User's Guide*.

Registers specific to MC can be read from console level, and these registers report errors in the system error log. Each operating system supporting Memory Channel has an error log. DECevent is designed for field service engineers to analyze the system error log. See Chapter 3, Troubleshooting, and Chapter 4, Memory Channel Subsystem Configurations and DECevent.

Chapter 3

Troubleshooting

This chapter describes basic Memory Channel troubleshooting procedures, using diagnostics and the system's error log. Topics covered include:

- Overview
- Error Logging
- MC Registers and Address Space Allocation
  – Link Control and Status Register (LCSR)
  – MC Error Register (MCERR)
  – MC Port Register (MCPORT)
  – Module Configuration Register (MODCFG)
  – Port Online State Register (POS)
  – CI Receive (from MC) Base Address Register (PRBAR)
  – Configuration Longword 10h –
    MC Transmit Base Address Register (CFG10H)
  – Configuration Longword 30h –
    Expansion ROM Base Address Register (CFG30H)

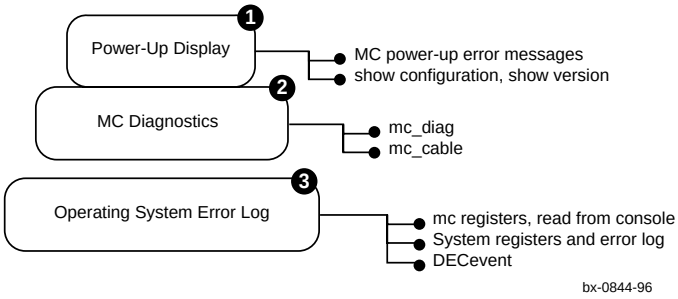
For more information:

Your AlphaServer system's *User's Guide*
Your AlphaServer system's *Service Information*

3.1 Overview

In addition to the physical installation of the hardware, you can check three main areas where troubleshooting information is collected.

Figure 3-1 Troubleshooting Overview



❶ At power-up, the console checks the hardware revision levels required for MC clusters. If the system hardware does not support MC clusters, the console will report one of three error messages (see Section 2.3, Console Error Messages). Internal test of MC module logic is not done during power-up.

The **show configuration** console command can be used to confirm that the CCMAB modules are reporting to the system console. The **show version** command reports the installed console firmware revision level.

❷ The **mc_cable** and **mc_diag** diagnostics, which check most of the logic of the MC hardware, are invoked only at the system console and do not execute during power-up. See Sections 4.2 and 4.3 for troubleshooting with mc_diag and mc_cable and Section 4.5, Cable Troubleshooting, of the *Memory Channel User's Guide.*

❸ Registers specific to MC can be read from console level, and these registers report errors in the system error log. Each operating system supporting Memory Channel has an error log. DECevent is designed for Compaq field service to analyze the system error log. See Section 4.7, Operating System Errors, of the *Memory Channel User's Guide*, and Section 3.3, Error Logging, Section 3.4, Reading Memory Channel Registers, and Section 3.5, MC Registers and Address Space Allocation of this manual for more information. After booting, run the System Verification Software, see Appendix B.

3.2 Error Logging

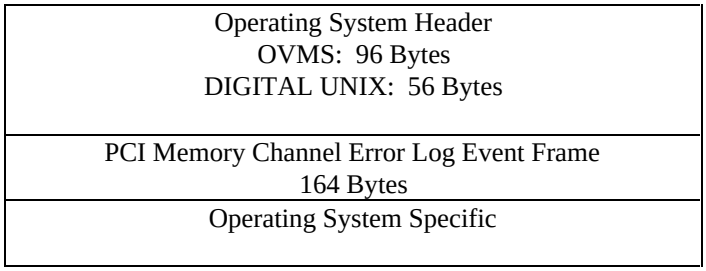
This section describes the format and content of the PCI Memory Channel adapter error event entry and an overview of the DECevent utility, which can be used to diagnose problems associated with Memory Channel hardware.

3.2.1 Error Log Overview

Using the general format described in this document, device drivers and operating system (platform-specific) code log errors detected and reported by PCI Memory Channel adapters. The complete event log entry comprises operating system event log header information followed by the PCI Memory Channel adapter specific information. The remaining event log entry contains operating system specific information, if required.

The event log entry contains information necessary to identify the source (node, PCI bus, adapter/FRU) of the fault. FRU replacement will depend on the engineer understanding the error log output and general knowledge of the system configuration.

Figure 3-2 General Event Log Entry Format



3.2.2 DECevent Overview

DECevent is a rules-based hardware fault management diagnostic tool that provides error event translation. During translation, the binary portion of an event log is transformed into readable text. This is known as Bit-to-Text translation (BTT). These events can then be displayed on the screen or printed.

Using DECevent allows Compaq and its customers to be proactive rather than reactive concerning maintenance issues. Customers can be notified of an upcoming problem and thereby schedule maintenance for minimal impact or downtime.

DECevent has the ability to update the knowledge libraries, as new products become available. Knowledge Library (KNL) updates are inclusive of all previous KNL information.

For more information on DECevent, including installation procedures and commands, use the WWW DECevent home page at http://www.service.digital.com/DECevent/

3.2.3 Memory Channel Adapter Event Report Generation Using DECevent

DIGITAL UNIX logs Memory Channel 1 adapter errors as "Adapter Type Errors" (entry type 105). For Memory Channel 2, adapter errors are logged as "Controller Type Errors" (entry type 104). To select MC adapter event log entries for DECevent translation report generation, enter the appropriate command:

On DIGITAL UNIX systems:

```
dia -i osf_entry=104  (MC2)
dia -i osf_entry=105  (MC1)
```

On OpenVMS systems:

```
$diagnose/translate/include=mca0
                           mcb0
```

If other types of adapter errors are in the event log, they are also included in the report. Example 3-1 is a sample DECevent report from a DIGITAL UNIX Memory Channel adapter error event entry. Example 3-2 is an OpenVMS example. The DECevent report is described in the sections that follow.

For more information:

DECevent Documentation
http://www.service.digital.com/DECevent/

3.2.4 DECevent Diagnosis Using the MC Error Event Entry

Information from the MC error event entry is displayed in the report in three places:

- The first section displays entry header information that identifies the system, event type, and timestamp.
- The second section (PCI Dev Config Data) displays PCI device configuration header information and displays the state of the PCI bus portion of the MC adapter. The contents of PCI bus control and status registers are displayed in this section of the report. These fields display the state of PCI bus-related error flags.
- The third section of the report (MC Adapter CSRs) displays the CCMAB adapter's control and status registers and displays the state of the Memory Channel portion of the adapter and any errors detected during Memory Channel interrupts. The significant Memory Channel error flags in the Link Control and Status Register (LCSR) and MC Error Register (MCERR) are displayed in this section of the report.

Asserted errors in PCI Control Register bits and PCI Status Register bits usually indicate a problem between the CCMAB adapter and the PCI bus. Check the event log for any error event entries logged by other PCI devices in the same time frame that might be related and assist in isolating the fault.

Asserted errors in the Link Control and Status Register and MC Error Register fields indicate a problem on the Memory Channel portion of the adapter. Depending on the specific error condition, the fault may be isolated to the reporting CCMAB adapter, the link cable, the associated hub linecard, or the hub. Check the system event logs of the other nodes in the cluster for any additional MC error event entries that may have been logged in the same time frame.

The DECevent report is divided into three sections:

❶ Section 1 displays entry header information, identifying the system, timestamp, and event type.

Example 3-1 DECevent Report Sample (DIGITAL UNIX)

```
*************************** ENTRY    7 ****************************
Logging OS                 ❶          2. Digital UNIX
System Architecture                   2. Alpha
Event sequence number                 7.
Timestamp of occurrence              15-AUG-1998 15:50:34
Host name                             sabl09

System type register      x00000018  AlphaServer 2000A or 2100A
Number of CPUs (mpnum)    x00000002
CPU logging event (mperr) x00000000

Event validity                        1. O/S claims event is valid
Event severity                        3. High Priority
Entry type                            104. Device Controller Type Errors

---- Device Profile ----
Unit                                   0
Product Name                          Memory Channel System
Vendor                                DIGITAL
  Subpacket Revision:         x0001
  PCI Frame Size:           x000000A4
```

❷ Section 2 displays PCI device configuration header information, displaying the state of the PCI bus portion of the MC adapter. The contents of the PCI bus control and status registers are displayed.

Example 3-1 DECevent Report Sample (DIGITAL UNIX) (Continued)

```
-- System/PCI Cfg Data - ❷
      Family ID                  24.
      Member ID                   0.
   Platform:              x00180000     --  Not Recognized
      Subpacket Revision:         1. Memory Channel II Frame
      Subpacket Length:   x000000A4

   PCI HOSE/Bus Number:           0.
   PCI Device ID Number:  x00000008  Physical Slot ID:  PCI 6

Vendor/Device ID Code     x00181011
        Vendor:               x1011  Digital Equipment Corp.
        Device:               x0018  PCI Memory Channel Adapter

Command Register      x0006  I/O Space Accesses Response:       DISABLED
                             Memory Space Accesses Response:    Enabled
                             PCI Bus Master Capability;         Enabled
                             Monitor for Special Cycle Ops:    DISABLED
                             Generate Mem Wrt/Invalidate Cmds: DISABLED
                             Parity Error Detection Response:  *IGNORE*
                             Wait Cycle Address/Data Stepping: DISABLED
                             SERR# Sys Err Driver Capability:  DISABLED
                             Fast Back-to-Back to Many Target: DISABLED
Status Register              x0400  Device is 33 Mhz Capable.
                                    Device Select Timing:  Slow.
Revision ID                    xA8  Memory Channel Adapter 2.0
  Reg Program Field            x00  Level Programming
  Sub Class Code               x80  Network Controller
  Base Class Code              x02  Network Controller
Sys Cache Line Size            x00
Latency Timer Value            xF8
Header Type                    x00  Single Function Device
Built-In Selftest              x00  No Built-In Selftest
  Window Control               x08  Valid PCI Address Space
  Base Address              xC00000  Transmit Base Address --- x000000
                                     PCITbar Field ----------- Not
Recognized
Expansion Rom Base Addr   x00000000
Interrupt Line Routing         x28
Interrupt Pin Being Used       x01
Min Bus Grant/Burst            x00
Max Bus Latency                x00
```

❸ Section 3 displays the state of the Memory Channel portion of the adapter and any errors detected during Memory Channel transactions. LCSR, MCERR, and MCPORT error flags are displayed.

Example 3-1 DECevent Report Sample (DIGITAL UNIX) (Continued)

```
MCLcs Reg   Bits  <15:00>  ❸   xC07E  MC Receive Path Error
                                     Configured as Virtual Hub
                                     MC Receive Error Interrupt Enabled
                                     MC Transmit Error Interrupt Enabled
                                     MC Interrupt Enabled
                                     Port Change Interrupt Enabled
                                     Alpha Mode
                                     MC Port State Change Interrupt
                                     Interrupt Summary Bit set
MCLcs Reg     Bits<31:16>     x0000
Rec Base Addr Bits<31:16>     x0800
Rev ID Test Value               xA8  Memory Channel Adapter 2.0
MCError Reg   Bits<15:00>   x0240  Link Control Packet Heartbeat Timeout
                                   Link RX Control Packet Error Summary
MCError Reg   Bits<31:16>     x0202  Heartbeat Timeout Enabled
                                   Link/Hub Receive Packet Summary Error
MCPort Reg    Bits<31:16>     x5201  Hub Linecard Slot 1 or VH1
                                     Port Status  - Timeout 0.75-1.5 sec
                                                  - Link Online Disable
                                                  - Adapter OK
                                                  - Link Broken
                                                  - Hub OK
Config Reg    Bits<15:00>     x001F  - Jumper Override
                                     - 8KB State
                                     - 128MB State
                                     - Sense 8KB
                                     - Sense 128MB
POS Reg       Bits<15:00>     x0000
```

❶ Section 1 displays entry header information, identifying the system, timestamp, and event type.

Example 3-2 DECevent Report Sample (OpenVMS)[1]

```
*************************** ENTRY    3 ********************************


Logging OS                ❶            1. OpenVMS
System Architecture                 2. Alpha
OS version                             H7.1-1H1
Event sequence number               6.
Timestamp of occurrence                03-SEP-1998 14:18:37
Time since reboot                      0 Day(s) 0:18:44
Host name                              SABL05

System Model                           AlphaServer 4000 5/400 4MB

Entry type                         98. Asynchronous Device Attention


---- Device Profile ----
Unit                                   SABL05$MCA0
Product Name                           Memory Channel Adapter
```

[1] DIAGNOSE/TRANSLATER/INCLUDE=MCA0

❷ Section 2 displays PCI device configuration header information, displaying the state of the PCI bus portion of the MC adapter. The contents of the PCI bus control and status registers are displayed.

Example 3-2 DECevent Report Sample (OpenVMS)[1] (Continued)

```
-- System/PCI Cfg Data -   ❷
      Family ID                  22.
      Member ID                   0.
   Platform:              x00160000     --  Not Recognized
      Subpacket Revision:         1. Memory Channel II Frame
      Subpacket Length:   x000000A4

   PCI HOSE/Bus Number:           0.
   PCI Device ID Number:  x00000004  PCI Physical Slot:  PCI 4


Vendor/Device ID Code     x00181011
        Vendor:               x1011  Digital Equipment Corp.
        Device:               x0018  PCI Memory Channel Adapter

Command Register       x0146  I/O Space Accesses Response:      DISABLED
                              Memory Space Accesses Response:    Enabled
                              PCI Bus Master Capability;         Enabled
                              Monitor for Special Cycle Ops:    DISABLED
                              Generate Mem Wrt/Invalidate Cmds: DISABLED
                              Parity Error Detection Response:    Normal
                              Wait Cycle Address/Data Stepping: DISABLED
                              SERR# Sys Err Driver Capability:   Enabled
                              Fast Back-to-Back to Many Target: DISABLED
Status Register               x0400  Device is 33 Mhz Capable.
                                     Device Select Timing:  Slow.
Revision ID                     xA8  Memory Channel Adapter 2.0
  Reg Program Field             x00  Level Programming
  Sub Class Code                x80  Network Controller
  Base Class Code               x02  Network Controller
Sys Cache Line Size             x00
Latency Timer Value             x10
Header Type                     x00  Single Function Device
Built-In Selftest               x00  No Built-In Selftest
  Window Control                x08  Valid PCI Address Space
  Base Address              x400000  Transmit Base Address ----- x000000
                                     PCITbar Field ------ Not Recognized
Expansion Rom Base Addr   x00000000
Interrupt Line Routing          x10
Interrupt Pin Being Used        x01
Min Bus Grant/Burst             x00
Max Bus Latency                 x00
```

[1] DIAGNOSE/TRANS/INCLUDE=ATTEN ERRLOG.OLD;-2

❸ Section 3 displays the state of the Memory Channel portion of the adapter and any errors detected during Memory Channel transactions. LCSR and MCERR error flags are displayed.

Example 3-2 DECevent Report Sample (OpenVMS) (Continued)

```
MCLcs Reg   Bits  <15:00>     x007C  Configured as Virtual Hub
                                     MC Receive Error Interrupt Enabled
              ❸                      MC Transmit Error Interrupt Enabled
                                     MC Interrupt Enabled
                                     Port Change Interrupt Enabled
                                     Alpha Mode
MCLcs Reg     Bits<31:16>     x0000
Rec Base Addr Bits<31:16>     xF800
MCError Reg   Bits<15:00>     x0010  Link Phase Lock Loop Error
MCError Reg   Bits<31:16>     x0200  Heartbeat Timeout Disabled
                                     Link/Hub Receive Packet Summary
Error
MCPort Reg    Bits<31:16>     xC200  Hub Linecard Slot  0 or VH0
                                     Port Status  - Timeout 7.4-8.0 sec
                                                  - Link Online Disable
                                                  - Adapter Broken
                                                  - Link Broken
                                                  - Link Hub OK
Config Reg    Bits<15:00>     x0006
POS Reg       Bits<15:00>     x0000

----- Software Info -----
UCB$x_ERRCNT                     1. Errors This Unit
UCB$L_DEVCHAR1            x00400000  Error Logging
example cont]
```

3.2.5 Fault Isolation

The error event reports, produced by the DECevent utility, will assist in isolating faults within the Memory Channel subsystem to a field-replaceable unit. In most cases, the event log of all nodes in the cluster should be examined using DECevent to determine the suspect FRU and the appropriate repair action. The log should also be checked for other potentially related PCI device entries to determine whether the problem is associated with the MC adapter, other PCI devices, bus bridges, or the PCI interconnect.

3.2.6 PCI Status and Control Register (CFG04H)

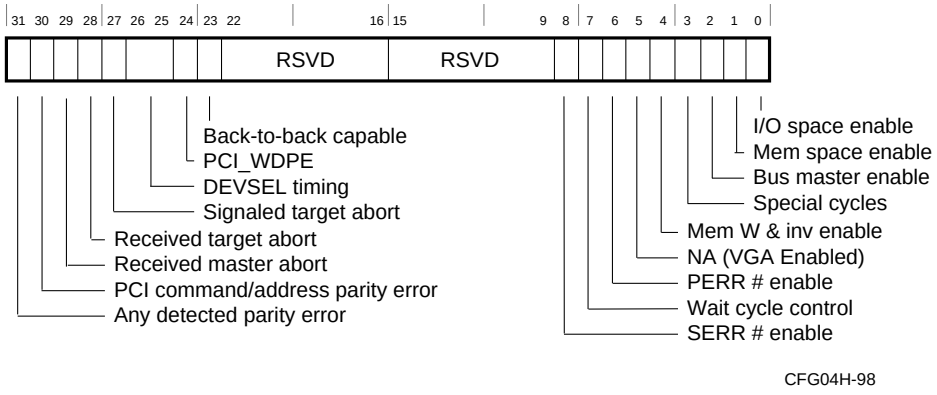


Table 3-1 PCI Status and Control Register (CFG04H) Bits

Name	Bit(s)	Type	Description
Any Detected Parity Error	<31>	W1C, 0	Set whenever the adapter detects any PCI parity error, even if parity error handling is disabled (as controlled by bit <6>). Two types of PCI parity errors are detected: write data parity error as a slave and address parity errors when the adapter is not the master ("potential" slave).
PCI Command/ Address Parity Error	<30>	W1C, 0	Set whenever the adapter asserts SERR PCI signal. The adapter asserts SERR# whenever it detects an address parity error and the adapter is not the master and SERR# Enable is set (bit <8>). This error indicates a parity error on a PCI write that potentially was an MC write, so the adapter asserts the Transmit Path Error bit (TPE, LCSR<00>).
Rcvd Master Abort	<29>	W1C, 0	Set whenever the adapter's master transaction on the PCI bus is terminated with a master abort sequence.
Rcvd Target Abort	<28>	W1C, 0	Set whenever the adapter's master transaction on the PCI bus is terminated with a target abort sequence.
Signaled Target Abort	<27>	R, 0	The adapter will never issue a target abort.
DEVSEL Timing	<26:25>	R, 10b	These bits, encoded as 10b, indicate the slowest time the adapter asserts DEVSEL for any bus command except Configuration Read/Write.

Table 3-1 PCI Status and Control Register (CFG04H) Bits (Continued)

Name	Bit(s)	Type	Description
PCI Write Data Parity Error while Master	<24>	W1C, 0	Set whenever the adapter detects an assertion of PERR# by the slave while it is the PCI bus master and the parity error response bit <6> is set. PERR# is asserted by the slave on a write to indicate a data parity error. This error indicates a parity error occurred on an MC write, so the adapter asserts the Receive Path Error bit (RPE, LCSR<1>).
Back-To-Back Capable	<23>	R, 0	Returns zero indicating the adapter is NOT capable of accepting back-to-back transactions when the transactions are not to the same agent.
RSVD	<22:9>	R, 0	Reserved.
SERR # Enable	<8>	R/W, 0	When enabled and on the detection of a PCI address parity error on a transaction for which it is not the master, the adapter drives the PCI SERR line and sets the TPE bit (LCSR<0>).
Wait Cycle Control	<7>	R, 0	Hardwired to zero, indicating the adapter does not support address/data stepping.
PERR # enable	<6>	R/W, 0	Controls the adapter's response to data parity errors. When set, the adapter asserts PERR# when it detects a write data parity error while it is the slave. When clear, the adapter ignores all data parity errors and completes the transaction as though parity were correct.
NA (VGA Control)	<5>	R, 0	Hardwired to zero.
Mem Write and Invalidate Enable	<4>	R, 0	This is the enable bit for using the Memory Write and Invalidate command. Hardwired to zero since the adapter never generates Memory Write and Invalidate commands.
Special Cycles	<3>	R, 0	Controls an adapter's action on "special cycle" operations. Hardwired to zero since the adapter does not support special cycle operations.
Bus Master Enable	<2>	R/W, 0	When set, allows the adapter to act as PCI bus master. When clear, the adapter cannot generate PCI accesses.
Memory Space Enable	<1>	R/W, 0	When set, the adapter can respond to PCI memory space accesses. When clear, the adapter cannot respond.
I/O Space Enable	<0>	R, 0	Controls adapter response to I/O space accesses. Hardwired to zero since the adapter does not support I/O space operations.

3.2.7 PCI Specific Problems

Detected Address Parity Error (PCI Bus Status Bits 31 & 30)

The adapter detected a PCI address parity error while not the master. The source of the bad address may be the source device (PCI bridge or another adapter), bus backplane, or the CCMAB bus adapter that detected and reported the error.

Fault Isolation Hints:

For three or more functioning devices on the bus (including the CCMAB and bus bridge):

At least one other device will also have detected and reported this error if the fault is associated with the source device or bus backplane. If there are multiple occurrences of the error reported by the same devices with the exception of one, then the one device that has not reported this error is the source of the bad address and should be replaced.

If the CCMAB is the only device reporting this error (multiple occurrences), then replace the CCMAB module. If the event log indicates that all devices on the bus have reported this error at least once, then the bus backplane is suspect and should be replaced if this pattern of errors continues.

For two functioning devices (CCMAB and bus bridge):

If the event log indicates that CCMAB module is the only device reporting this error, then either the CCMAB module or the bus bridge is defective.

If the event log indicates that both the bus bridge and CCMAB have reported this error at least once, then the bus backplane is suspect and should be replaced if this pattern of errors continues.

PCI Detected Write Data Parity Error (PCI Bus Status Bit 31 and Bit 30=0)

The adapter detected a PCI write data parity error while a slave. The source of the bad data may be the source device (PCI bus bridge or another adapter) PCI bus backplane, or the CCMAB bus adapter that detected and reported the error.

Fault Isolation Hints:

Check for a PCI error entry in the same time frame from another device on the same bus indicating a "PCI Write Data Parity Error While Master." Such an entry identifies the initiator (master) device and source of the data.

For three or more functioning devices on the bus (including the CCMAB and bus bridge):

If other devices on the bus report the same error condition along with associated entries from the same initiator device indicating a "Data Parity Error While Master," then replace that device.

If the CCMAB is the only device reporting this error (multiple occurrences), then replace the CCMAB module.

If the event log indicates that all devices on the bus have reported this error at least once, then the bus backplane is suspect and should be replaced if this pattern of errors continues.

For two functioning devices (CCMAB and bus bridge):

If the event log indicates that CCMAB module is the only device reporting this error, then either the CCMAB module or the bus bridge is defective.

If the event log indicates that both the bus bridge and CCMAB have reported this error at least once, then the bus backplane is suspect and should be replaced if this pattern of errors continues.

Received Master Abort (PCI Bus Status Bit 29)

The CCMAB adapter terminated the PCI bus transaction with a master abort sequence indicating that no target device claimed the transaction.

Fault Isolation Hints:

Check for a pattern of other devices on this bus reporting the same error with the exception of one. The software could be sending a nonexistent address.

Received Target Abort (PCI Bus Status Bit 28)

The CCMAB adapter terminated the PCI bus transaction due to a signaled target abort, indicating the target either detected a fatal error or will never be able to respond to the transaction.

Fault Isolation Hints:

Check for other devices on this bus reporting an error in the same time frame.

PCI Write Data Parity Error While Master (PCI Bus Status Bit 24)

The CCMAB adapter detected the assertion of PERR# by the target (slave) device while it was PCI bus master. This indicates that the target device detected a data parity error on a write from the CCMAB adapter (MC write receive). This would typically indicate a problem on the PCI side of the CCMAB.

Fault Isolation Hints:

There should be an associated error log entry from the target device indicating a "Write Data Parity Error."

For three or more functioning devices on the bus (including the CCMAB and bus bridge):

If other devices on the bus report the same error condition along with associated entries from the same target device indicating a "Write Data Parity Error," then replace that device.

If the CCMAB is the only device reporting this error (multiple occurrences and multiple target devices), then replace the CCMAB module.

If the event log indicates that all devices on the bus have reported this error at least once, then the bus backplane is suspect and should be replaced if this pattern of errors continues.

For two functioning devices (CCMAB and bus bridge):

If the event log indicates that the CCMAB module is the only device reporting this error, then either the CCMAB module or the bus bridge is defective.

If the event log indicates that both the bus bridge and CCMAB have reported this error at least once, then the bus backplane is suspect and should be replaced if this pattern of errors continues.

3.3 MC Registers and Address Space Allocation

Conventions used in register descriptions and in references to bits and fields are as follows:

- Registers are referred to by their mnemonics, such as **MCERR** register for the **Memory Channel Error Register**.
- Bits and fields are enclosed in angle brackets (for example, bit **<31>** and bits **<31:16>)**. Bits are usually specified by their numbers or names enclosed in angle brackets adjacent to the register mnemonic, such as **CFG10<31:27>** or **CFG10<PTBAR>,** which are equivalent designations.
- The **Type** column entry of a register description table may include the initialization value of the bits. For example, entry "R/W, 0" indicates a read/write bit that is initialized to 0.

The following abbreviations are used to indicate the access type of the bit(s):

Acronym	Access Type
R	Read only; writes ignored.
R/W	Read/write.
W1C	Read/write one to clear; unaltered by a write of zero.

Nine registers are useful in diagnosing Memory Channel problems. Six of these (LCSR, MCERR, MCPORT, PRBAR, CONFIG, and POS) reside in the PCI Transmit Window (see Table 3-2) and three (CFG04H, CFG10H, and CFG30H) in PCI Configuration Space.

Table 3-2 PCI Transmit Window Address Allocation

PTBAR+00000	PCT R/W Access
PTBAR+3FFFF	(256 KB)
PTBAR+40000	CSR Registers
PTBAR+41FFF	(8 KB)
PTBAR+42000	MC Transmit Space
PTBAR+7FFFFF	128 MB

3.3.1 Link Control and Status Register (LCSR)

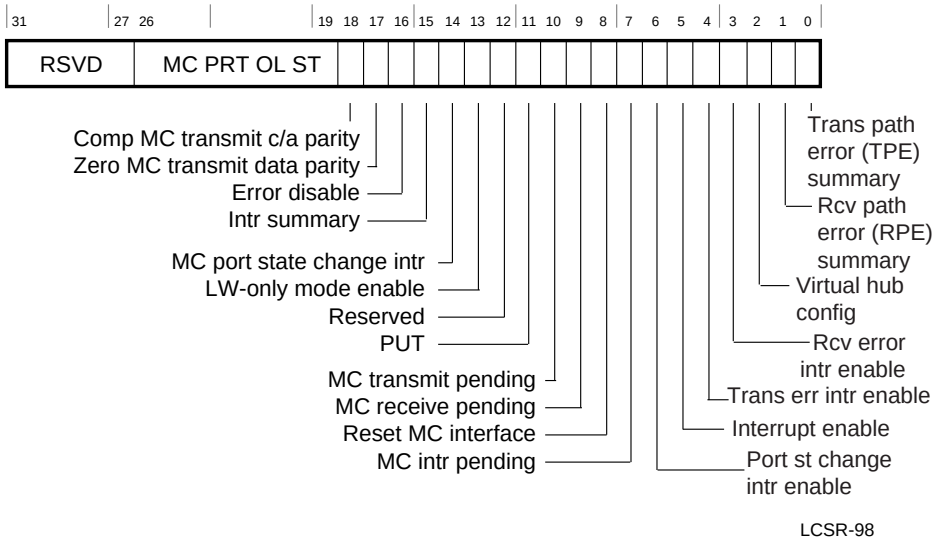


Table 3-3 LCSR Register (PTBAR + 40000) Bits

Name	Bit	Type	Description
RSVD	<31:27>	R, 0	Read as zeros.
MC Port Online State - Nodes [7:0]	<26:19>	R, 0	This field is a shadowed subset of the POS register. In hub-based systems, this field reflects the state of the MC port online state of all nodes in the cluster. A '1' indicates the port at the corresponding node ID is in the "Link Online" state; a '0' indicates it is not in the "Link Online" state. In virtual hub systems this field is undefined.
RSVD	<18:16>	R/W, 0	Reserved.
Interrupt Summary	<15>	R, 0	This bit represents the logical OR of all interrupting conditions from this adapter. TPE interrupt; RPE interrupt; MC interrupt and MC port state change interrupt.

Table 3-3 LCSR Register (PTBAR + 40000) Bits (Continued)

Name	Bit	Type	Description
MC Port State Change Interrupt	<14>	W1C, 0	This bit is set whenever the adapter has generated an interrupt request based on a change in the MC port state (local online, link online, etc.). LCSR<6> must be set to enable the generation of MC port state change interrupts.
RSVD	<13>	R/W, 0	Reserved.
Scatter/Gather Enable (SGA)	<12>	R/W, 0	When set, the scatter/gather table is used instead of PRBAR for mapping the receive MC virtual address to the local PCI address. May only be set when the adapter is configured with a 128MB window.
PUT	<11>	R/W, 1	When set, this adapter's Link OK signal remains deasserted and the adapter is limited to local online operation, the power-up testing (PUT) state.
MC Transmit Pending	<10>	R, 0	This bit is set when there is at least one packet in the MC-Transmit FIFO.
MC Receive Pending	<9>	R, 0	This bit is set when there is at least one packet in the MC-Receive FIFO.
Reset MC Interface	<8>	R/W, 0	Writing a 1 to this bit resets all the MC control logic and state. The PCI control logic and state are unaffected.
MC Interrupt Pending	<7>	W1C, 0	This bit is set when an MC-write to a page with INTR (from page control table)=1.
MC Port State Cng Intr Enbl	<6>	R/W, 0	When set, enables the generation of a PCI interrupt on any MC port state change.
MC Interrupt Enable	<5>	R/W, 0	When set, enables the generation of a PCI interrupt on receipt of an MC write to a page with INTR=1.
MC Trans Err Intr Enable	<4>	R/W, 0	When set, enables the generation of a PCI interrupt on the occurrence of an MC transmit path error (TPE).
MC Rcv Error Intr Enable	<3>	R/W, 0	When set, enables the generation of a PCI interrupt on the occurrence of an MC receive path error (RPE).
Virtual Hub Configuration	<2>	R, 0	This bit is set if the adapter is configured in a virtual hub cluster (either as the VH0 or VH1 node); it is 0 if the adapter is connected to a hub.
MC Rcv Path Error Summary	<1>	W1C, 0	This bit is set when any MC receive path error (RPE) occurs.
MC Trans Path Error Summary	<0>	W1C, 0	This bit is set when any MC transmit path error (TPE) occurs.

3.3.2 MC Error Register (MCERR)

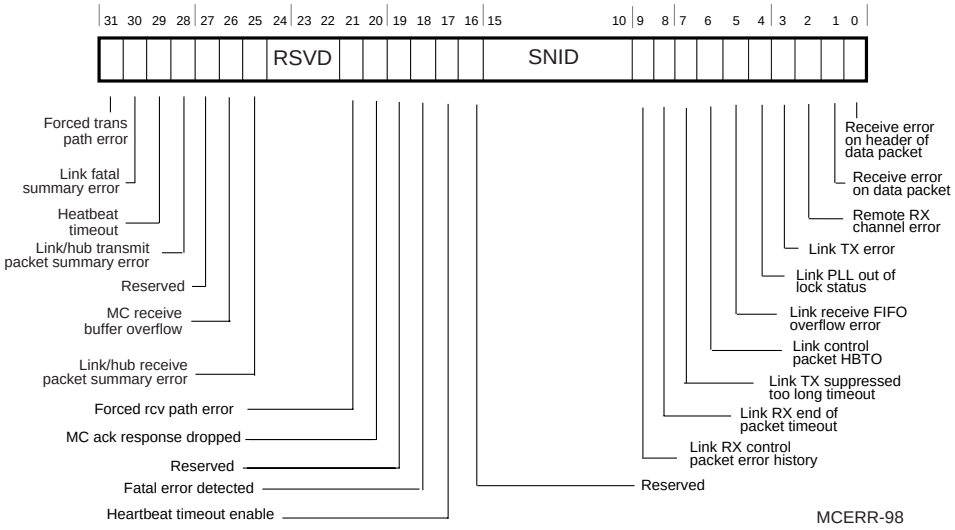


Table 3-4 MCERR Register (PTBAR + 41000) Bits

Name	Bit(s)	Type	Description
RSVD	<31>	W1C, 0	Reserved.
Link Fatal Summary Error (Fatal)	<30>	W1C, 0	Set when the link generates either receive (RPE) or transmit (TPE) path fatal error. To determine the cause of this error, check MCERR bits <15:0>.
Heartbeat Timeout (HBTO)	<29>	W1C, 0	Set if the adapter detects a heartbeat timeout. Adapter sets this bit, TPE and RPE, goes to the Fatal Link Error State. The adapter's Link OK signal is deasserted and Link Online is then deasserted.
Link/Hub Trans Packet Summary Err	<28>	W1C, 0	Set when the link or hub detects a packet error on an MC Transmit Write. To determine the cause of this error, check MCERR bits <15:0>.
Reserved	<27>	R, 0	Reserved.
MC Receive Buffer Overflow	<26>	W1C, 0	Set if the adapter attempts to load the receive FIFO when the FIFO is full. Adapter sets this bit, TPE and RPE, goes to the fatal link error state, deasserts its Link OK signal; then deasserts Link Online.

Table 3-4 MCERR Register (PTBAR + 41000) Bits (Continued)

Name	Bit(s)	Type	Description
Link/Hub Receive Packet Summary Error	<25>	W1C, 0	Set whenever the link or hub detects a receive path error (RPE) on an MC receive packet. To determine the cause of this error, check MCERR bits <15:0>. Response: The bit is set, RPE (LCSR<01>) is set, the packet is marked bad and flushed.
Reserved	<24:21>		Reserved. Bit<24> = R, 0. Bit<23>=W1C, 0. Bit<22>=R/W, 0. Bit<21>=W1C, 0.
MC ACK Response Dropped	<20>	W1C, 0	Status. A dropped MC ACK response is a permitted event. This bit is implemented to allow the OS to retry.
Reserved	<19>	W1C, 0	Reserved.
Fatal Error	<18>	R, 0	Set whenever the adapter or the LIC-Link chip detects a fatal error. Following a fatal error, the adapter is taken off-line and must be reset before resuming normal operation. If no other error bits are set, then the fatal error occurred due to a power supply transient.
Heartbeat Timeout Enable	<17>	R/W, 0	When set, the adapter logic enforces an HBTO which will force the MC port offline if at least one MC transmit transaction is not generated by the node within the HBTO period. The HBTO period is selected by MCPORT<26>.
RSVD	<16>	R/W, 0	Reserved.
SNID*	<15:10>	R, 0	Source Node Identification (SNID) decode field

15	14	13	12	11	10	SNID
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	0	1	0	0	4
0	0	0	1	0	1	5
0	0	0	1	1	0	6
0	0	0	1	1	1	7

**NOTE: SNID field only valid when a receiving adapter detects a Receive Path Error (RPE).*

Table 3-4 MCERR Register (PTBAR + 41000) Bits (Continued)

Name	Bit(s)	Type	Description
Link RX Control Packet Error History	<9>	R, 0	Indicates an error in the reception of a control packet. Does not, by itself, cause any other error bits to be set. It merely indicates an internal error that has resolved itself without generating an MC error. Cleared by a reset.
Link RX End of Packet Timeout	<8>	R, 0	Indicates that the link received a packet, which is too long, and now out of sync. Filters the bad packet, sets LCSR<1,0> (RPE/TPE), MCERR bits <30> and <18> (fatal error), and takes the node offline.
Link TX Suppressed Too Long Timeout	<7>	R, 0	When set, indicates a failure in the link's remote FIFO flow control mechanism. Sets LCSR<1,0> (RPE/TPE), MCERR bits <30> and <18> (fatal error), and takes the node offline.
Link Control Packet HBTO	<6>	R, 0	When set, indicates the link's internal control packet communication facility has failed. Sets LCSR<1,0> (RPE/TPE), MCERR bits <30> and <18> (fatal error), and takes the node offline.
Link Receive FIFO Ovrflw Error	<5>	R, 0	When set, indicates a fatal error in the link's local RX FIFO flow control mechanism. Sets LCSR<1,0> (RPE/TPE) and bits <30>and <8>(fatal error).
Link PLL Out of Lock Status	<4>	R, 0	Indicates, dynamically, the current lock status of the link's Phase Lock Loop. When set ("out of lock"), LCSR<1,0>(RPE/TPE) is set, MCERR bits <30> and <18> (fatal error), and the node is taken offline.
Link TX Error	<3>	R, 0	Detects two types of errors: (1) the TX FIFO going full, (2) a malformed packet from a packet read from the TX FIFO. If due to the TX FIFO going full, sets LCSR<1,0> (RPE/TPE) and bits <30> and <18> (fatal error). If due to a general packet error, sets the link TPE <28> and LCSR<0>. Does not transmit the packet over the cable in either case.
Remote RX Channel Error	<2>	R, 0	Indicates special cases of an RX error in the remote node that needed to be reflected back in the sender node as a TPE error. Occurs in a virtual hub system when a loopback request arrives at a remote node with an error. The sender must be notified with a TPE error, otherwise the result would be a missing loopback packet and no error bits would be indicated on the sender node. Sets LCSR<0> and TPE<28>.
Recv Err on Data Packet	<1>	R, 0	Sets LCSR<1> (RPE) and MCERR Register bit<25>.
Recv Err on Header of Data packet	<0>	R, 0	Sets LCSR<1> (RPE) and MCERR Register bit<25>.

3.3.3 MC Port Register (MCPORT)

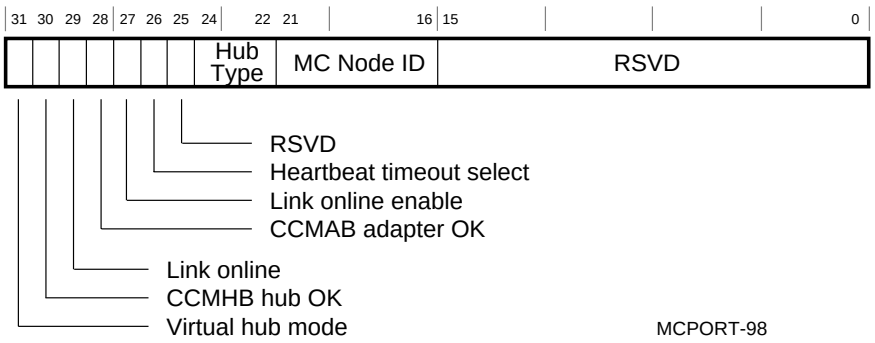


Table 3-5 MCPORT Register (PTBAR + 41004) Bits

Name	Bit(s)	Type	Function
Virtual Hub Mode	<31>	R, n	This bit reflects the state of the J1 hub mode jumper on the adapter. When set, indicates adapter is configured as part of a virtual hub cluster and that this adapter is node 0 and will provide the link arbitration. If clear, indicates that this node is part of a cluster using the MC hub, or node 1 in a hubless configuration.
CCMHB Hub OK	<30>	R, 0	When set, indicates the Link Hub OK signal is asserted.
Link Online	<29>	R, 0	When set, indicates the Link Online signal is asserted.
CCMAB Adapter OK	<28>	R, 0	When set, indicates the Link Adapter OK signal is asserted.
Link Online Enable (OLEN)	<27>	R/W, 0	When set, enables adapter to enter Link Online state. Adapter hardware automatically clears OLEN in the transition to the Link Online state. This clearing assures that the adapter will not exit and reenter the Link Online state for a cable removal and replacement; instead the adapter will remain in the Local Online-Wait OK/OLEN.
Heartbeat Timeout Select	<26>	R/W, 0	This bit selects the value of the Heartbeat Timeout (HBTO). When set, 1.7≤HBTO≤2 seconds; when clear, 7.4≤HBTO≤8 seconds.

Table 3-5 MCPORT Register (PTBAR + 41004) Bits (Continued)

Name	Bit(s)	Type	Function
RSVD	<25>	R, 1	Reserved.
Hub Type	<24:22>	R, 1	This field powers up to a 00 hex and remains 00 hex in a virtual hub configuration (no loading of this field occurs in a virtual hub system).
MC Node ID	<21:16>	R, n	This field contains the MC node ID used by the MC protocol for transaction routing. The hub assures that each node is assigned a unique node ID based on the physical slot in the hub to which the cable is attached. The 8-node hub assigns node IDs 0 - 7. For a node connected to a hub, this field is loaded from the hub linecard as part of the adapter initialization sequence. In a virtual hub configuration, the virtual hub node VH0 is always assigned node ID 0 and the other node (VH1) is assigned node ID 1. 21 20 19 18 17 16 = 0, Hub linecard 0 or VH0 21 20 19 18 17 16 = 1, Hub linecard 1 or VH1 21 20 19 18 17 16 = 2, Hub linecard 2 21 20 19 18 17 16 = 3, Hub linecard 3 21 20 19 18 17 16 = 4, Hub linecard 4 21 20 19 18 17 16 = 5, Hub linecard 5 21 20 19 18 17 16 = 6, Hub linecard 6 21 20 19 18 17 16 = 7, Hub linecard 7
RSVD	<15:0>	R, 0	Reserved.

3.3.4 Module Configuration Register (MODCFG)

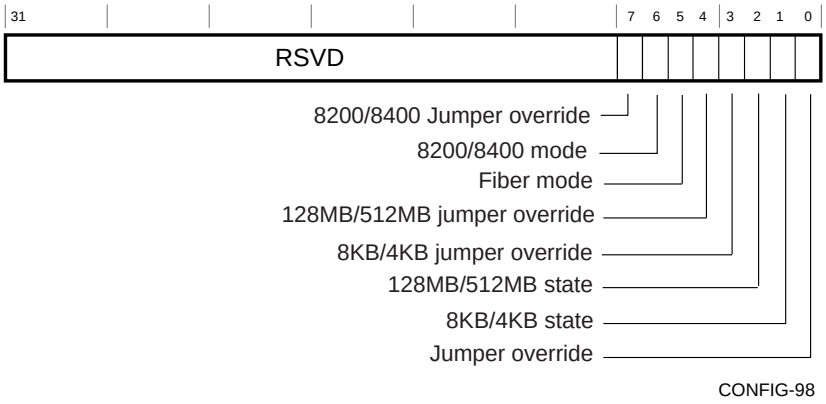
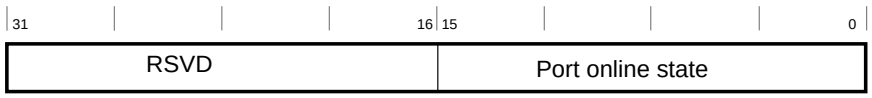


Table 3-6 Module Configuration Register (MODCFG) Bits

Name	Bits	Type	Description
RSVD	<31:8>	n, 0	Reserved.
8200/8400 Jumper Override	<7>	R/W, 0	When set, and the Jumper Override bit<0> is set, the adapter will be forced to 8200/8400 mode.
8200/8400 Mode	<6>	R, 0	When set, the adapter is in 8200/8400 mode, increasing 8200/8400 bandwidth up to 20MB/s.
Fiber Mode	<5>	R, 0	When set, the fiber mode jumper is installed and the module is in fiber mode.
128MB/ 512MB Jumper Override	<4>	R, 0	When set, and the Jumper Override bit<0> is set, the adapter window size will be 128MB. When set, and the Jumper Override bit<0> is cleared, the adapter window size will match the jumper.
8KB/ 4KB Jumper Override	<3>	R/W, 0	When set, and the Jumper Override bit<0> is set, the adapter page size will be 8KB. When set, and the Jumper Override bit<0> is cleared, the adapter page size will match the jumper.
128MB/ 512MB State	<2>	R, n	When set, the adapter will be mapped to a 128MB window. When cleared, the window is set to 512MB.
8KB/4KB State	<1>	R, n	When set, the adapter is set to 8KB page mode. When cleared, the mode is set to 4KB page.
Jumper Override	<0>	R/W, 0	When set, the hardware jumpers are disabled and the override configuration bits are enabled. When cleared, the hardware jumpers are enabled.

3.3.5 Port Online State Register (POS)

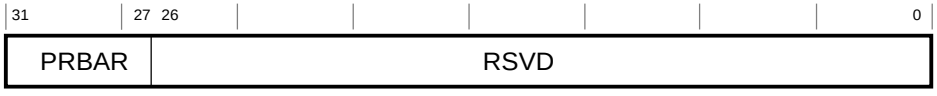


POS-98

Table 3-7 Port Online State Register (POS) Bits

Name	Bits	Type	Description
RSVD	<31:16>	n, 0	Reserved.
Port Online State	<15:0>	R, 0	In hub based systems, this field reflects the state of the MC PORT Online state at all nodes in the cluster. A '1' indicates the port at the corresponding node ID is in the "Link Online" state. In virtual hub systems this field is not used. Bits <7:0> are a shadow of LCSR<26:19>.

3.3.6 PCI Receive (from MC) Base Address Register (PRBAR)



PRBAR-98

Table 3-8 PCI Receive (from MC) Base Address Register (PRBAR) Bits

Name	Bit(s)	Type	Description
PCI Receive Base Address (PRBAR)	<31:27>	R/W, 0	Defines the window in PCI memory space that the MC adapter writes to. Used to map Memory Channel DMA writes to host scatter/gather space.
RSVD	<26:0>		Reserved.

3.3.7 Configuration Longword 10h - MC Transmit Base Address Register (CFG10H)

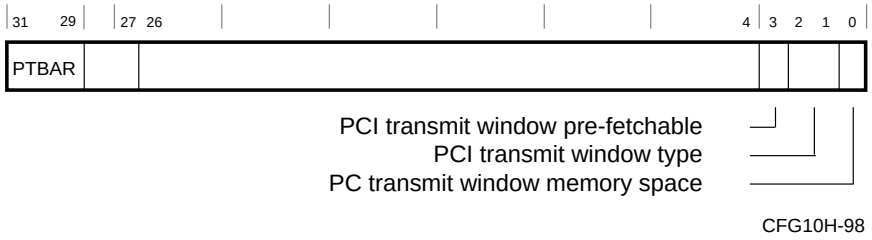


Table 3-9 Configuration Longword 10h - MC Transmit Base Address Register (CFG10H) Bits

Name	Bit(s)	Type	Description
PTBAR: 512MB 128MB	 <31:29> <31:27>	R/W, 0	Defines the window in PCI memory space that will select this adapter for MC transmits. Used to map PCI write transactions to the MC.
For 512MB	<28:4>	R, 0	All these bits are read as zero.
For 128MB	<26:4>	R, 0	All these bits are read as zero.
PCI Transmit Window Prefetchable	<3>	R, 1	Returns a one, normally indicating the adapter window is prefetchable. The one assures the PCI MC Adapter Transmit Window is in PCI dense space.
PCI Transmit Window Type	<2:1>	R, 0	Returns 00b, indicating that this window can be placed anywhere within a 32b PCI address space as long as it is naturally aligned based on the window size.
PCI Transmit Window Memory Space	<0>	R, 0	Read as zero, indicating that this window is in PCI memory space.

3.3.8 Configuration Longword 30h - Expansion ROM Base Address Register (CFG30H)

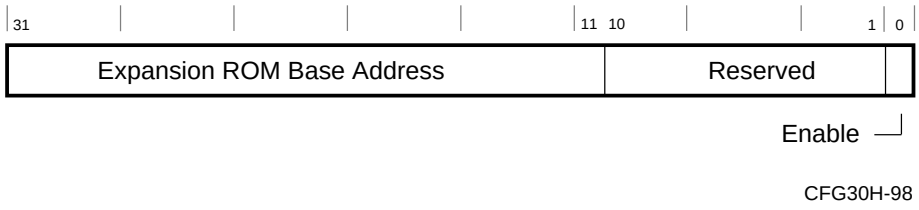


Table 3-10 Configuration Longword 30h - Expansion ROM Base Address Register (CFG30H) Bits

Name	Bit(s)	Type	Description
Expansion ROM Base Address	<31:22>	R/W, 0	Defines the window in PCI memory space that will read/write this adapter's expansion ROM.
	<21:1>	R, 0	All these bits are read as zero.
Enable	<0>	R/W, 0	Enables accesses to the device's expansion ROM. When set, allows reads or writes to the expansion ROM address space. When cleared, access to the expansion ROM is disabled.

Chapter 4

Memory Channel Subsystem Configurations and DECevent

This chapter provides an overview of the Memory Channel (MC) port state and port state signals. It gives examples of MC subsystem configurations, MC subsystem troubleshooting using DECevent, FRU callouts based on failure examples, and explains how to use Source Node Identification (SNID) as a troubleshooting aid. Examples of the MC Configuration FRU Table Entry are also included. Sections include:

- MC Port State Overview and Signals
- MC Subsystem Configurations
  - Definitions
  - Source Node Identification
  - Troubleshooting Cluster Examples
- MC Configuration FRU Table Entry
  - System Resource Subpacket
  - Vital Product Data Subpacket

4.1. MC Port State Overview and Signals

There are three primary MC port states: *Local Online, Link Online,* and *Fatal Error.* Three bits in the MC Port Register (see Table 4-1) are useful in determining the state of communication between an adapter and hub in a standard hub system or between two adapters (VH0 and VH1) in a virtual hub configuration.

A node powers up in the *Local Online* state. In this state, local Memory Channel operations; that is, "loopbacks" can be performed. Any power-up testing a node performs is done while in this state.

When a node is ready to join a cluster, the CCMAB adapter asserts the link cable signal, *Link Adapter OK*. This informs the CCMHB hub, connected to the other end of the link cable, that the adapter is prepared to join the MC hub. Independently, the hub asserts a corresponding signal, *Link Hub OK*, when the hub is ready to establish a connection with the adapter. When both OK signals are asserted, the hub and adapter hardware perform a simple synchronization operation to form a low-level connection over the link cable. The hub asserts the link signal, *Link Online,* after this connection is established. Once the hardware connection is established, software can use the MC subsystem to communicate to other nodes in the cluster.

The MC port *Fatal Error* state is entered if the adapter detects an error condition that requires the adapter to be reset in order to recover from the failure. When the adapter enters the *Fatal Error* state, it deasserts *Link Adapter OK*. When the hub detects the deassertion of *Link Adapter OK*, it deasserts *Link Online*. The detection and recovery from transient errors (such as data parity errors) do not cause any change in the primary MC port state.

The above description describes a configuration using the CCMHB hub. In a virtual hub (hubless) system, VH0 takes the responsibilities of the hub and will drive/receive the MC Port State normally driven/received by the hub. VH0, for example, drives the *Link Hub OK* signal and monitors *Link Adapter OK*.

Figure 4-1 MC PORT Register

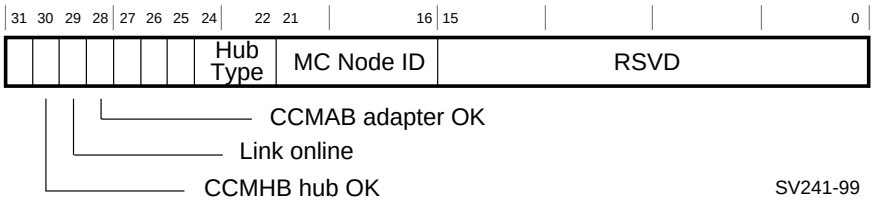


Table 4-1 MC PORT Register Signal Bits

Name	Bit	Type	Function
CCMHB Hub OK	<30>	R, 0	When set, indicates the Link Hub OK signal is asserted. When the hub is ready to establish a connection with the adapter, it asserts the Link Hub OK signal. The state of this signal is indicated by an LED on the CCMAB adapter and the CCMLB hub linecard (see Figure 1-6). In a virtual hub configuration, this signal is driven by VH0 (see Section 1.3, CCMAB Adapter).
Link Online	<29>	R, 0	When set, indicates the Link Online signal is asserted. This signal is asserted after the adapter and hub have established a connection over the link cable. In a virtual hub configuration, this signal is driven by VH0 (see Section 1.3, CCMAB Adapter).
CCMAB Adapter OK	<28>	R, 0	When set, indicates the Link Adapter OK signal is asserted. When the adapter is ready to establish a connection with the hub, it asserts the Link Adapter OK signal. The state of the Link Adapter OK signal is indicated by an LED on the adapter and the hub linecard (see Figure 1-6). In a virtual configuration, this signal is driven by VH1 (see Section 1.3, CCMAB Adapter).

4.2. MC Subsystem Configurations

The section provides sample Memory Channel configurations and troubleshooting examples of subsystem failures. It provides guidelines and documented theory of how a failure in the Memory Channel subsystem will be depicted in DECevent and how errors will be displayed across platforms. For sample DECevent reports, see Section 3.2, Error Logging.

In analyzing failures it is important that service engineers review all error logs, console logs, and operating system messages across all platforms before replacing a FRU.

NOTE: Check all cable connections and connector pins before replacing any FRU.

Memory Channel design, along with operating system retry algorithms, permits extended usage of the subsystem without catastrophic failures. Layered products utilize the subsystem much like a network with packet retries. Actual FRU replacement should be minimal.

4.2.1. Definitions

- Transmitting adapters – generate error "check" bytes (parity generation).
- Linecards associated with transmitting adapters – check parity (parity detection)
- Linecards associated with the receiving adapters – pass data (no error checking)
- Receiving adapters – check parity (parity detection)
- MC hub – pass data (no error checking)
- RPE – Receive Path Error
- TPE – Transmit Path Error

4.2.2. Source Node Identification (SNID)

As a troubleshooting aid, MCERR Register bits <15:10> provide the Source Node Identification (SNID). When a receiving adapter detects an RPE, the SNID field will be collected in the adapter's register file and posted in the binary error log along with the already collected status and control registers. This data can then be utilized as additional information in problem diagnoses.

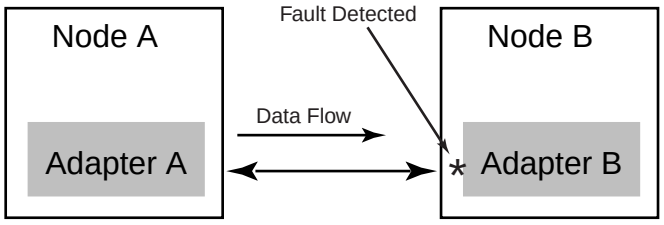
There are cases where the SNID value collected by the microcode may be in error; for example, the SNID field in the data packet had bad parity and caused the RPE. Therefore, analyzing the various error logs from all platforms, understanding the hardware configurations, and looking closely at timestamps within DECevent will assist in problem diagnoses.

Examples 4-5 and 4-6 show how to use the SNID register when troubleshooting the Memory Channel subsystem.

4.2.3. Troubleshooting Cluster Examples

This section illustrates a two-node virtual hub cluster, a two-node standard hub cluster, and a four-node standard hub cluster. For each example, it describes the error condition and what the DECevent error log will show and suggests repair strategy.

Figure 4-2 Two-Node Virtual Hub Cluster



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Example 4-1 Link Detected "Receive Error on Data Packet" on Node B

Data Transfer: Node A transmits to Node B (see Figure 4-2)

1. Adapter B detects an error – Receive Error on Data Packet (MCERR 01).
2. Adapter B sets RPE and Link Receive Packet Summary Error (MCERR 25).
3. Adapter B raises the Interrupt Signal to host processor.
4. Adapter B sends error control packet to adapter A reflecting Link Receive Packet Summary Error.
5. Adapter A sets TPE and Link Transmit Packet Summary Error (MCERR 28).
6. Adapter A raises the Interrupt Signal to host processor.

The link chip in adapter B detected an error in its Receive Path. In a virtual hub configuration, the receiving adapter notifies the transmitting adapter of the error.

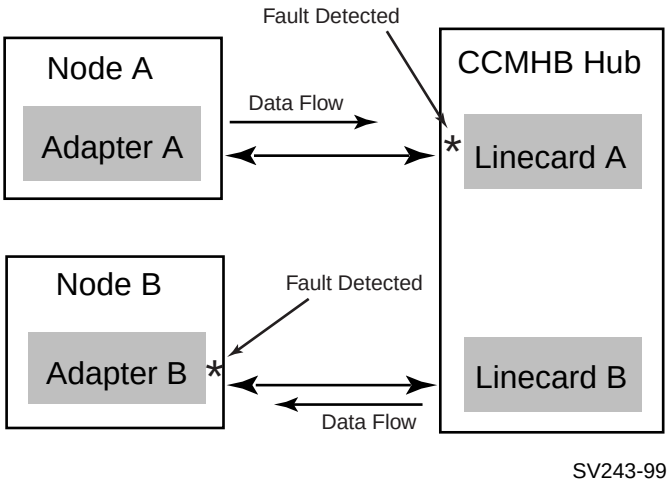
The DECevent error log will reflect:

- TPE on node A
- Link Transmit Packet Summary Error on node A
- RPE on node B
- Link Receive Packet Summary Error on node B
- Receive Error on Data Packet on node B

Check/replace in suggested order:

- Cable/cable connections
- Adapter A
- Adapter B

Figure 4-3 Two-Node Standard Hub Cluster - Case 1



Example 4-2 Link Detected "Receive Error on Data Packet" by Linecard A

Data Transfer: Node A transmits to Node B (see Figure 4-3)

1. Linecard A detects an error – Receive Error on Data Packet (MCERR 01).
2. Linecard A sends an error control signal to adapter A, reflecting a linecard detected error.
3. Adapter A sets TPE and Link Transmit Packet Summary Error (MCERR 28).
4. Adapter A raises the Interrupt Signal to the host processor.
   Linecard A detected an error. However, because data parity is checked at the end of the packet, the faulty data transfer is committed to the MC hub. The linecard cannot buffer the entire data packet and then perform the parity check, therefore the data packet is passed to the hub. Remember that the hub does not check the data, it just passes the data to the destination node. Therefore, the target node, in this case, node B, will detect the data error and set RPE and Link Receive Packet Summary Error (MCERR 25).
5. Target Adapter B sets RPE and Link Receive Packet Summary Error.
6. Target Adapter B raises the Interrupt Signal to host processor.

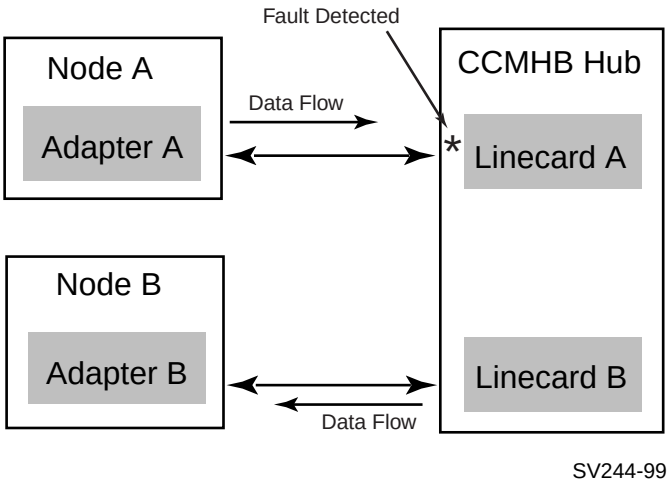
The DECevent error log entry will show:

- TPE on node A
- Link Transmit Packet Summary Error on node A
- RPE on node B
- Link Receive Packet Summary Error on node B
- Receive Error on Data Packet on node B
- Look at the error log(s) on all platforms, and compare event times and analysis the failure. The problem is on the transmit side (node A) of the hub.

Check/replace in suggested order:

- Cable/cable connections between linecard A and adapter A
- Adapter A
- Linecard A

Figure 4-4 Two-Node Standard Hub Cluster - Case 2



Example 4-3 Link Detected "Receive Error on Header of Data Packet" by Linecard A

Data Transfer: Node A transmits to Node B (see Figure 4-4)

1. Linecard A detects an error – Receive Error on Header of Data Packet (MCERR 00).
2. Linecard A sends an error control signal to adapter A reflecting a linecard detected error.
3. Adapter A sets TPE and Link Transmit Packet Summary Error (MCERR 28).
4. Adapter A raises the Interrupt Signal to host processor.

Linecard A detected an error in the header of the incoming packet. In this case, the header contains the parity error, which is checked at the beginning of the packet. The Linecard detects the header error, and the transfer is aborted. The data, in this case is not passed to the MC hub.

The DECevent error log entry will show:

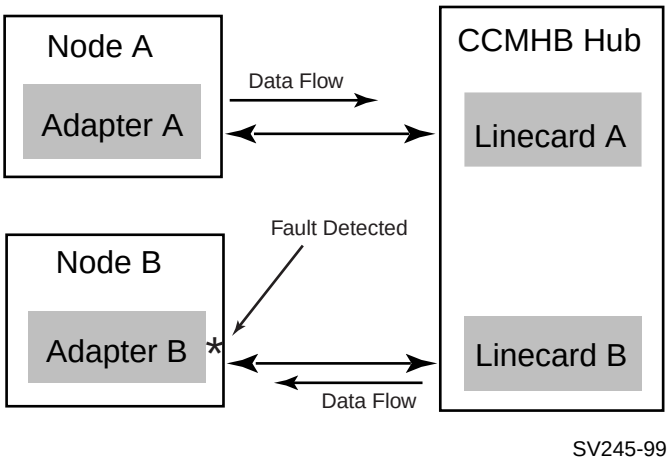
- TPE on node A
- Link Transmit Packet Summary Error on node A

The problem here is on the transmit side (node A) of the hub.

Check/replace in suggested order:

- Cable/cable connections between linecard A and adapter A
- Adapter A
- Linecard A

Figure 4-5 Two-Node Standard Hub Cluster - Case 3



Example 4-4 Link Detected "Receive Error on Data Packet" on Node B

Data Transfer: Node A transmits to Node B (see Figure 4-5)

1. Adapter B detects error - Receive Error on Data Packet (MCERR 01)
2. Adapter B sets RPE and Link Receive Packet Summary Error (MCERR 25).
3. Adapter B raises the Interrupt Signal to host processor.

This example could be a broadcast command to all nodes, or a data command to only one adapter. In this case, ONLY adapter B detected an error in its Receive Path and sets RPE.

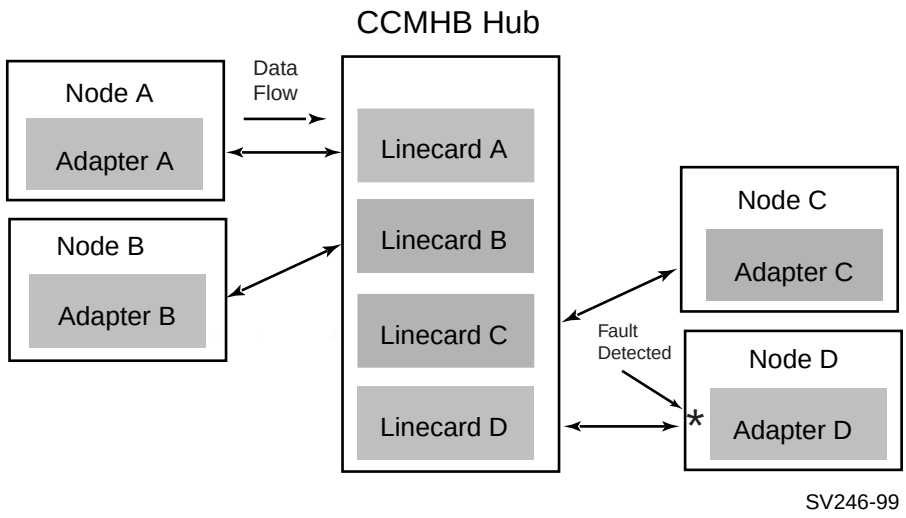
The DECevent error log entry will show:

- RPE on node B
- Link Receive Packet Summary Error on node B
- Receive Error on Data Packet on node B

Check/replace in suggested order:

- Cable/cable connections between linecard B and adapter A
- Adapter B
- Linecard B
- Linecard A
- Hub

Figure 4-6 Four-Node Standard Hub Cluster - Case 1



Example 4-5 Link Detected "Receive Error on Data Packet" by Node D

Data Transfer: Node A transmits to *ALL* or *ANY* Node (see Figure 4-6)

1. Adapter D detects error - Receive Error on Data Packet (MCERR 01)
2. Adapter D sets RPE and Link Receive Packet Summary Error (MCERR 25).
3. Adapter D raises the Interrupt Signal to host processor.

This example could be a broadcast command to all nodes, or a point-to-point command to only one adapter. In this case, ONLY adapter D detected an error in its Receive Path and sets RPE.

This is a case where the SNID register may have added value. When adapter D sets RPE, it also captures the SNID. The source of the data is node A. This expands the DECevent callout to include linecard A.

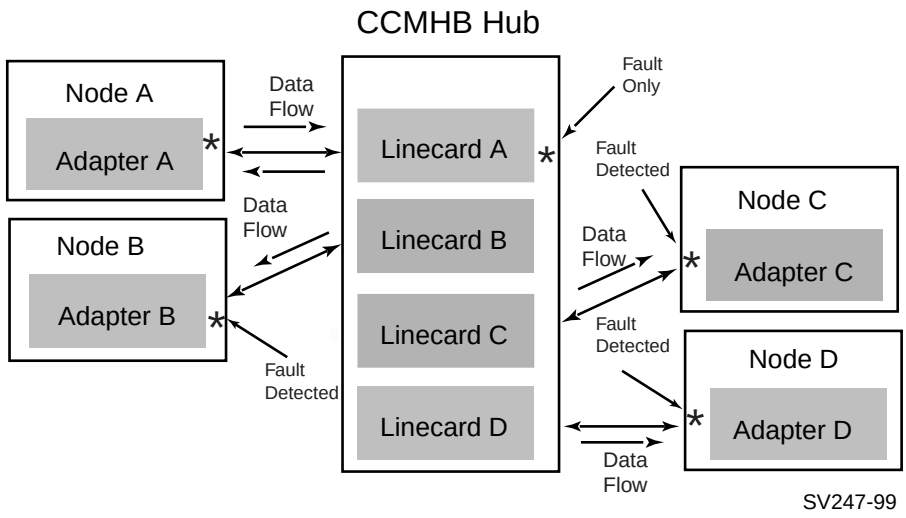
The DECevent error log entry will show:

- RPE on node D
- Link Receive Packet Summary Error on node D
- Receive Error on Data Packet on node D

Check/replace in suggested order:

- Cable/cable connections between linecard D and adapter D
- Adapter D
- Linecard D
- Linecard A - The SNID may have added value. Change linecard A before replacing the hub.
- Hub

Figure 4-7 Four-Node Standard Hub Cluster - Case 2



Example 4-6 Multiple Links Detected "Receive Error on Data Packet"

Data Transfer: Node X transmits to *ALL* Nodes (Broadcast Command) (see Figure 4-7)

1. Adapter detects error - Receive Error on Data Packet (MCERR 01)
2. Adapter sets RPE and Link Receive Packet Summary Error (bit 25).
3. Adapter raises the Interrupt Signal to host processor.

This example is a broadcast command to all nodes. The transmitting adapter and its associated linecard did not detect an error when the transmit occurred. However, all receiving adapters detected an error (in a broadcast command, the transmitter also becomes a receiver). The error occurred on the transmitting linecard (after the error checking logic) or in the hub. Since TPE was never set, the transmitting adapter/ linecard cannot be identified.

This is another case where the SNID register may add value to the problem. Check all nodes via the error log and analyze the problem. All receiving adapters will have RPE set. Check the SNID filed in the error log across all adapters; the transmitting adapter's linecard is likely faulty.

The DECevent error log entry will show:

- RPE on all nodes
- Link Receive Packet Summary Error on all nodes
- Receive Error on Data Packet all nodes

Check/replace in suggested order:

- Linecard from SNID
- Hub

4.3. MC Configuration FRU Table Entry

At system start-up or boot time, the console identifies all known devices and deposits a binary bitmap entry, known as a System Resource Subpacket. When DECevent executes, the following report is generated and is visible to the user. These FRU Configuration Table Entries are excellent resources for the user as configuration management and asset management tools. Example 4-7 illustrates a Memory Channel Configuration FRU Table Entry.

4.3.1. System Resource Subpacket

Example 4-7 System Resource Subpacket

```
      ================ System Resource Subpacket  ===============
          Length              x0058
          Class 1.            System Resource Subpacket
          Type 5.             PCI
          Revision            1.

PCI Device Registers ----
PCI Configuration Address     x000000F9C0040018
                                          PCI: 0
                                          Bus: 0
                                          Device Number: 4

Vendor/Device ID Code  x00181011
        Vendor:                      x1011 Digital Equipment Corp.
        Device:                      x0018 PCI Memory Channel Adapter

Command Register    x0146  I/O Space Accesses Response:      DISABLED
              Memory Space Accesses Response:                Enabled
              PCI Bus Master Capability;                     Enabled
              Monitor for Special Cycle Ops:                 DISABLED
              Generate Mem Write/Invalidate Cmds:            DISABLED
              Parity Error Detection Response:               Normal
              Wait Cycle Address/Data Stepping:              DISABLED
              SERR# Sys Err Driver Capability:               Enabled
              Fast Back-to-Back to Many Targets:             DISABLED
```

Example 4-7 System Resource Subpacket (Continued)

```
Status Register            x0400  Device is 33 MHz Capable.
                           No Support for User Definable Features.
                           Fast Back-to-Back to Different Targets,
                           Is Not Supported in Target Device.
                           Device Select Timing:     Slow.
Device Revision:                    xA8
Device Class Code:                  x028000
Sys Cache Line Size:                x00
Latency Timer Value:                x10
Header Type:                        x00  Single Function Device
Built-in Self Test CSR:             x00
Base Address Register 1             x40000008
Base Address Register 2             x00000000
Base Address Register 3             x00000000
Base Address Register 4             x00000000
Base Address Register 5             x00000000
Base Address Register 6             x00000000
Expansion Rom Base Addr:            x00000000
Interrupt Line Routing:             x10
Interrupt Pin Being Used:           x01
Min Bus Grant/Burst:                x00
Max Bus Latency:                    x00
```

4.3.2. Vital Product Data Subpacket

The MC Configuration FRU Table Entry has been enhanced with the addition of the Vital Product Data (VPD) Subpacket (see Example 4-8) which includes the following data items:

1. Part number (example, 54-12345-01)
2. FRU part number (example, CCMAB-AA)
3. Engineering revision of assembly (example, B01)
4. Manufacturing ID (example, NIO)
5. Serial number of specific assembly (example, NI72400097)
6. ROM code revision (example, 45)
7. Minimum ROM code revision (example, 42)

The VPD elements are coded according to an Industry Standard PCI Specification.

Example 4-8 Vital Product Data Subpacket

```
    --------------------- FRU Subpacket  ----------------------

          Length       x0053
          Class 2.     FRU Subpacket
          Type 3.      PCI FRU
          Rev  2.

Console Slot ID:       x0000000D Number 13
   FRU Self Test Status       x00000001 Self-Test Status NOT Available

     Assembly Number (PN)     54-12345-01
     FRU Number      (FN)             CCMAB-AA
     Engineering Rev (EC)             B01
     Mfg. ID Number   (MN)    NIO
     Serial Number   (SN)             NI72400099
     ROM Code Rev    (RM)     171
     Loadable Level  (LL)             34
```

Appendix A

Updating Firmware

Use the Loadable Firmware Update (LFU) Utility to update system firmware. LFU runs without any operating system and can update the firmware on any system module. You are not required to specify any hardware path information, and the update process is highly automated.

Both the LFU program and the firmware microcode images it writes are supplied on a CD-ROM. You start LFU by booting the CD. A typical update procedure is:

1. Boot the LFU CD-ROM.
2. Use the LFU **list** command if you want to check the current firmware versions.
3. Use the LFU **update** command to write the new firmware.
4. Exit

Example A-1 LFU Booting

```
P00>>> b dka600                  [boot the CD]
.
.
.
jumping to bootstrap code

VMS PALcode V5.56-7, OSF PALcode V1.45-12
       .
       .
       .
       .

------------------------------------------------------------
     ++++++++++++++++++++++++++++++++++++++++++++  Jan. 4, 1999
     +    AlphaServer 2000/2100/2100A Firmware  +
     +              README-First !!!            +
     ++++++++++++++++++++++++++++++++++++++++++++
       .
       .
       .
Hit <RETURN> to scroll text, or <CTRL/C> to skip text.
       .
       .
       .
The default bootfile for this platform is

        [ALPHA2100]OCT24_SBUPDATE.EXE

Hit <RETURN> at the prompt to use the default bootfile.

Bootfile:                 [Hit<RETURN>]


VMS PALcode V5.56-7, OSF PALcode V1.45-12

starting console on CPU 0
initialized idle PCB
       .
       .
```

```
      .
      .
***** Loadable Firmware Update Utility *****
--------------------------------------------------------------
 Function    Description
--------------------------------------------------------------

Display     Displays the system's configuration table.
Exit        Done exit LFU (reset).
List        Lists the device, revision, firmware name, and
                update revision.
Readme      Lists important release information.
Update      Replaces current firmware with loadable data image.
Verify      Compares loadable and hardware images.
? or Help   Scrolls this function table.
--------------------------------------------------------------


UPD> list           [display the current firmware versions]

Device      Current Revision    Filename        Update Revision

arcflash    4.54-0               arcrom         4.55-0
mca0        171                  ccmab_fw       171
mcb0        171                  ccmab_fw       171
srmflash    4.10-6146            srmrom         5.1-1470
                    cipca_fw              A315
                    dfeaa_fw              1.3
                    dfeab_fw              3.10
                    dfxaa_fw              3.10
                    kzpsa_fw              A11

UPD> update mca0          [update the firmware]

Confirm update on:
mca0
[Y/(N)]y
WARNING: updates may take several minutes to complete for each
device.

                          DO NOT ABORT!

mca0            Updating to 171...  Verifying 171...  PASSED.

UPD> exit                 [type exit]

Do you want to do a manual update? [y/(n)]   [return]


Please reset the system...[do a manual reset at this point]
```

Appendix B

Running the MC Exerciser

The MC Exerciser is one of a number of generic exercisers contained in the System Verification Software (formerly known as DEC VET). The Verification Software is an installation (and repair) verification procedure, test controller, and system exerciser. It provides users with both a Windows and a command interface and allows the user to exercise the hardware and software in the same way for every node, regardless of the operating system under which the software is running.

The Verification Software comes with a standard set of exercisers, which test and verify system hardware and software and the base operating system. The Verification Software supports various exerciser configurations, ranging from a single device exerciser to simultaneous exercising of multiple devices.

NOTE: Refer to the System Verification Software documentation for details on invoking the Verification Software exercisers.

For more information:

Digital System Verification Software Release Notes and Installation Guide
Digital System Verification Software Getting Started Guide for your operating system

Table B-1 lists typical Verification Software exercisers. The specific names and exercisers displayed may vary with the operating system.

Table B-1 Verification Software Exercisers

Exerciser	Description
CPU	Tests processor functions including binary operations, integer computations, floating-point computations, and data conversion.
Memory	Tests dynamic allocation and deallocation of virtual memory and verifies test patterns written.
Disk	Tests logical and physical disk I/O by performing read and write operations and verifies test patterns written.
Memory Channel	Tests reading and writing between master and client.
File	Tests reading and writing to disk files and verifies test patterns written.
Tape	Tests reading and writing to tape device files (including file mark detection, spacing, rewind, end-of-tape detection) and verifies test patterns written.
Network	Tests underlying protocol (including caches, buffers, and queues), physical network adapters, local and remote networks, destination adapters, and network services.
Printer	Tests printers by sending ASCII, PostScript, or a user specified file to a selected print queue. A PostScript file is provided with the exerciser.
Video	Tests text, graphic, and palette capabilities of video monitors. Graphic tests check various video distortions possible in a CRT monitor.

Sizing Memory Channel

The Memory Channel exerciser provides on-line verification of the Memory Channel hardware. When the Verification Software is invoked, all nodes in a Memory Channel cluster that are visible to the operating system are automatically sized (see Figure A-1). The hub is not sized. All Memory Channel nodes will be displayed by the sizer according to device name (mc0, mc1, etc.) and will be identified as a Memory Channel device type. This information is listed by using the **show devices all** command.

Figure B-1 Sized Device Screen

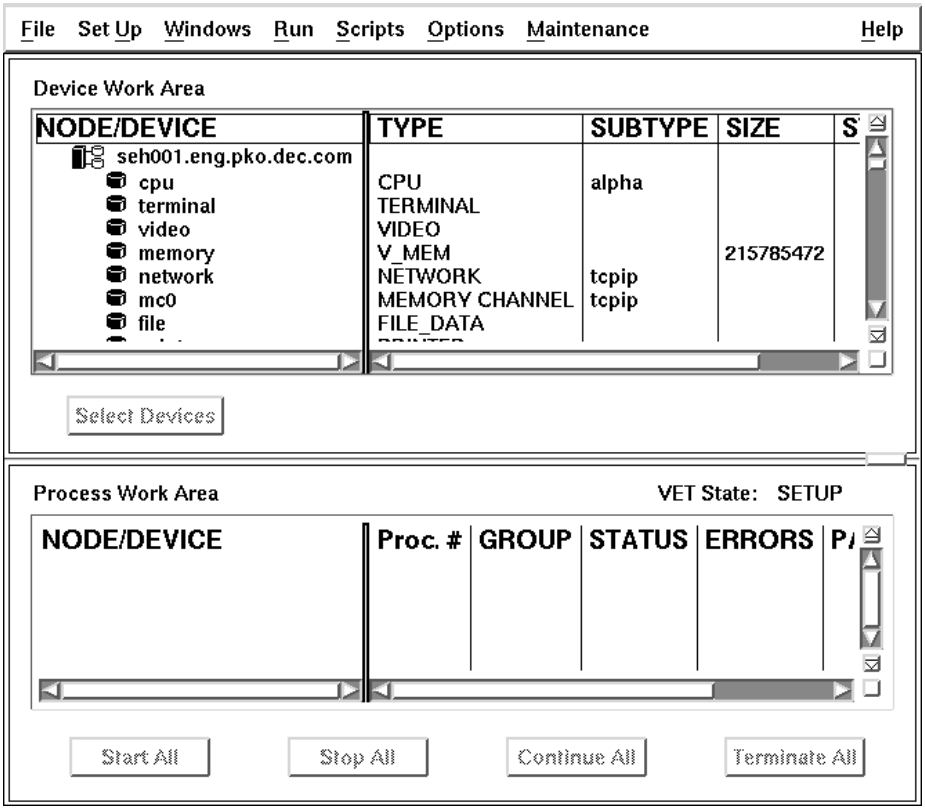
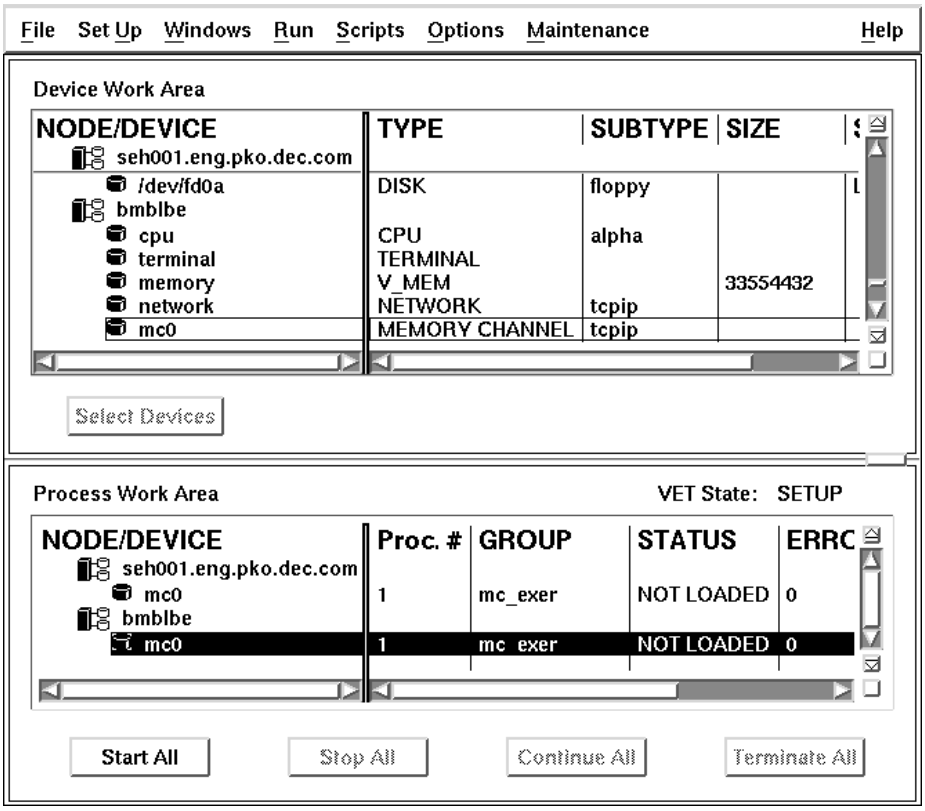


Figure B-2 Selecting MC Exerciser Screen



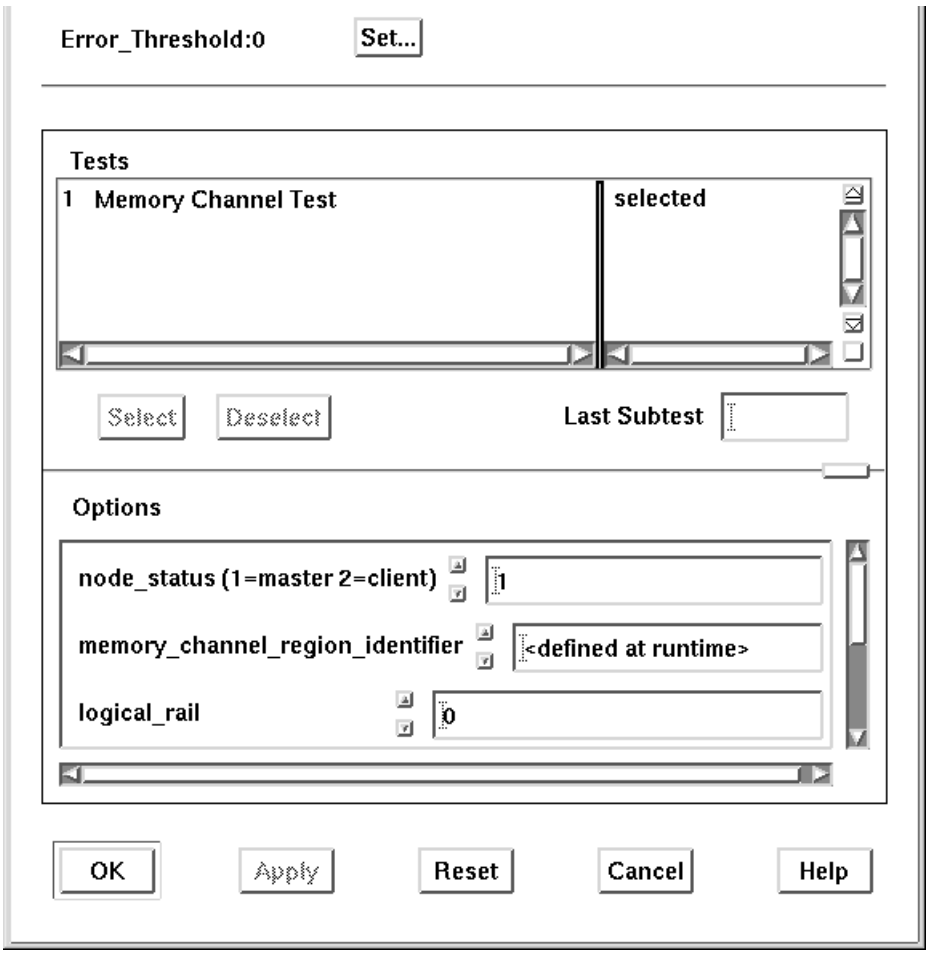
Testing Memory Channel

The master node allocates a Memory Channel address space region of 8KB and fills the address space with the test pattern. The client in the test reads the test pattern from the allocated region. This cycle is repeated for each of four test patterns: all ones (1111), all zeros (0000), alternating ones and zeros (1010), and alternating zeros and ones (0101). This process is repeated with each node in the cluster alternating as master. A mismatch between read data and expected data (the test pattern) will be reported as an error.

Selecting Nodes for Test and Test Options

The user must select a minimum of two nodes for testing. The memory_channel_region_identifier (see Figure B-3) must be identical at the master and client. The user can select the run time, pass count, cpu affinity, and data pattern for test. There will be only one test in the test group.

Figure B-3 Parameters Screen



Error Reports

Errors reported by the Memory Channel Exerciser include, but are limited to:

- A mismatch between expected and received data
- A failed call to the Memory Channel Application Programming Library Interface

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