1

Addendum to KA680 CPU Module Technical Manual

Print date: August 1993

Part Number: EK-KA680-UP. C01

LPN S2336

Preface

This document is an addendum to the KA680 CPU Module Technical (Part number EK-KA680-TM.001). Included are changes and additions pertaining to the KA675, KA681 KA690, KA691, and KA692 CPU modules.

The table below outlines the key differences between the six CPU modules:

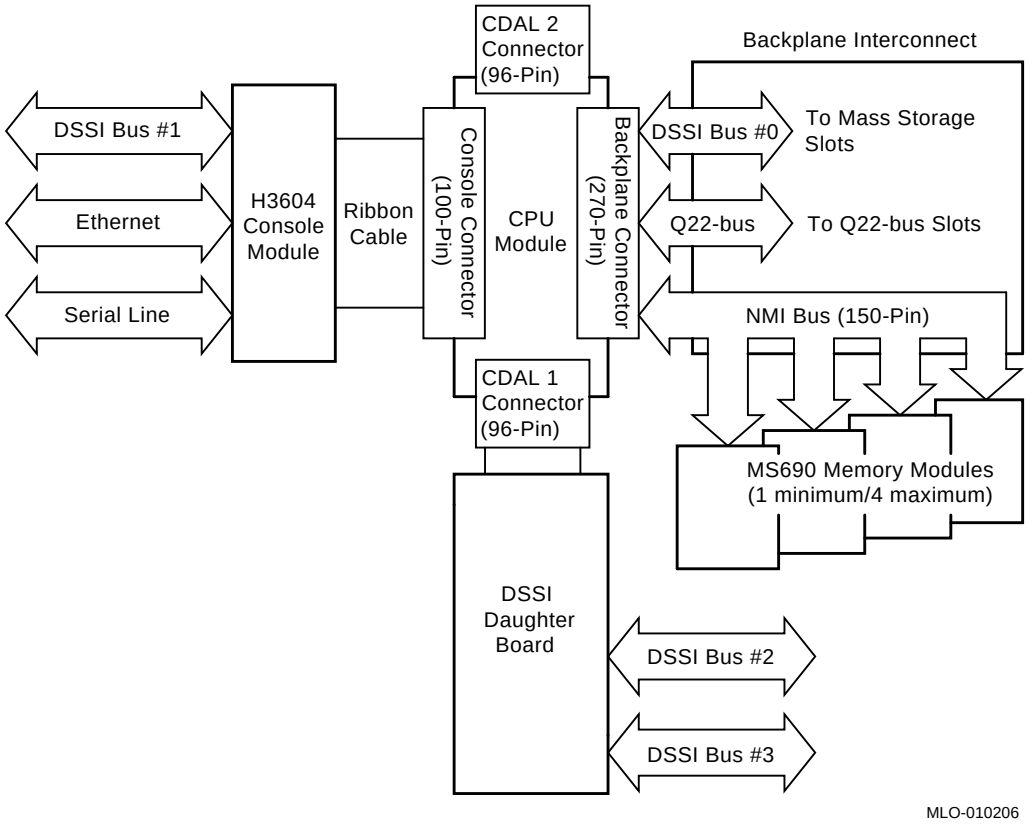
Module	Clock Speed	Cache Size	VIC?	I/O Expansion?
KA675	16ns	128 KByte	No	No
KA680	14ns	128 KByte	Yes	No
KA690	12ns	512 KByte	Yes	No
KA681	14ns	128 KByte	Yes	Yes
KA691	12ns	512 KByte	Yes	Yes
KA692	10ns	2 MByte	Yes	Yes

Changes to the technical manual itself are listed on the following pages. The changes are bulleted, listed by page number, followed by a description of the change. Unless otherwise noted in this document, all references to the KA680 CPU module in the KA680 CPU Module Technical Manual can be taken to include the KA675, KA681, KA690, KA691, and KA692 CPU modules.

Changes, additions to the KA680 CPU Module Technical Manual to include the KA675, KA681, KA690, KA691, and KA692 CPUs:

Page 1-1:

- Figure 1-1, rename to KA675/KA680/KA690 Module in a System
- Add figure: KA681/KA691/KA692 Module in a System

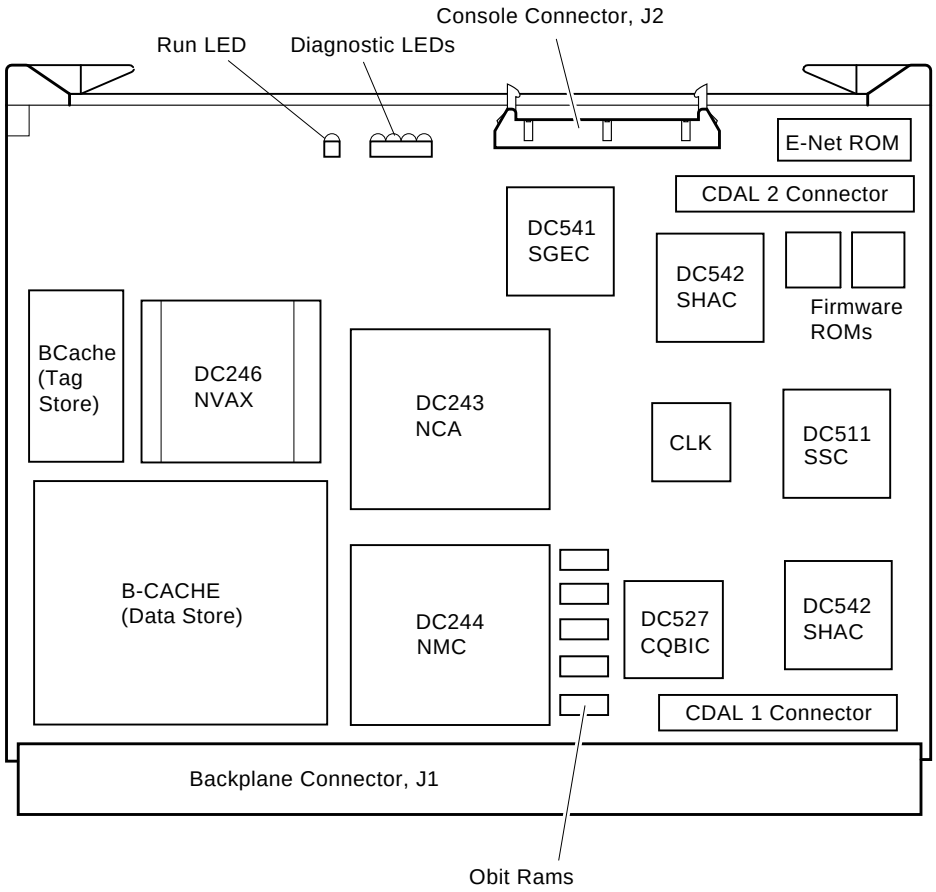


Page 1-3:

Major hardware components description changes:

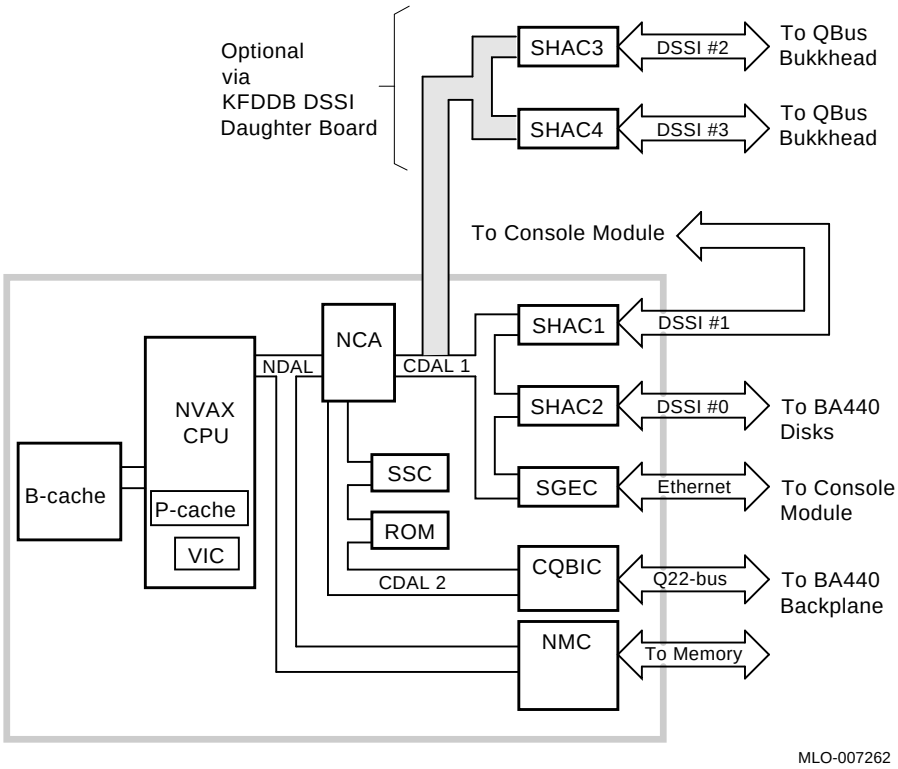
- Cache RAMs — 128 KB backup cache (KA675, KA680, KA681) / 512 KB backup cache (KA690, KA691)/ 2MB backup cache (KA692)
- Firmware ROMs (4) — 512KB; each 128KB by 8 FLASH programmable (KA675,KA680,KA690)
- Firmware ROMs (2) — 512KB; each 256KB by 8 FLASH programmable (KA681, KA691, KA692)
- CDAL Bus connectors — 96-pin connectors for daughter card option (e.g., KFDDB) (KA681, KA691, KA692)

- Figure 1-3, rename to KA675/KA680/KA690 Module Component Side
- Add figure: KA681/KA691/KA692 Module Component Side



Page 1-4:

- Figure 1-4, rename to KA675/KA680/KA690 CPU Module Block Diagram
- Add figure: KA681/KA691/KA692 CPU Module Block Diagram



Page 1-5:

- Section 1.2.1.2 The Cache Memory, first paragraph. Change to:

The *processor modules* use a 3-level cache architecture to maximize performance. The first level of cache, referred to as the *virtual instruction cache* (VIC), is 2 kilobytes (KB), and is located in the CPU chip. This cache handles instructions only (no data references), and deals only with virtual addresses. In this way, the CPU can obtain instruction information without the need for virtual to physical address translation, thereby decreasing the latency and improving performance. *The KA675 processor module does not implement this first level of cache.*

- Section 1.2.1.2 The Cache Memory, third paragraph. Change to:

The third level of cache, referred to as the *backup cache* (Bcache), stores instructions and data. *The KA675, KA680, and KA681 Bcache is 128 KBytes, the KA690 and KA691 Bcache is 512 KBytes, and the KA692 Bcache is 2 MBytes.* The Bcache is controlled by the Bcache controller located in the CPU chip. The data and tag store memory for this cache is located in SRAM chips on the *CPU* module. The Bcache uses physical addresses.

Page 1-8:

- Section 1.3 MS690 Memory Module, add to end of second paragraph:

Note that the 32 MB memory module is not supported for use with the KA692 CPU processor module.

Page 2-7:

- Section 2.4 DSSI Cabling, Device Identity, and Bus Termination

Add after second paragraph:

The KA681, KA691, and KA692 CPU modules have connectors to the CP buses. The KFDDB dual-DSSI daughter card connects to the CP1 bus connector. This option allows for 2 more DSSI buses in the BA440 enclosure. Cables from the daughter card connect to two QBus bulkhead handles. Each handle has two 50-pin connectors, providing an in-out connection to each of the extra DSSI buses. These connectors require terminators if the bus is unused.

Page 3-43:

- Table 3-11 (Cont.) The System Control Block Format

Add entries to table:

SCB Offset	Interrupt/Exception Name	Type	# Params	Notes
10C	Mass Storage Interface Three (DSSI PORT 3)	Interrupt	0	IPL is 14
110	Mass Storage Interface Four (DSSI PORT 4)	Interrupt	0	IPL is 14

Page 3-46:

- Table 3-13 System Identification Extension Register Bits

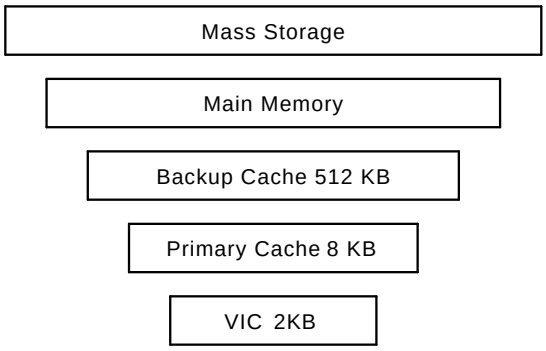
Add entries to table:

Field	Name	RW	Description
15:8	SYS_SUB_ TYPE	ro	This field identifies the particular system subtype. *07 : KA690* *0C: KA675* *0E: KA681* *0F: KA691* *10: KA692*

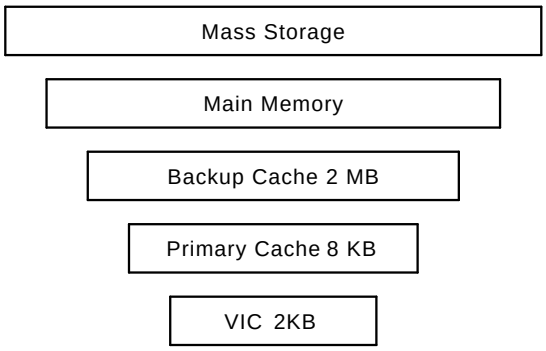
Page 4-1:

- Figure 4-1, rename to KA680,KA681 Cache/Memory Hierarchy

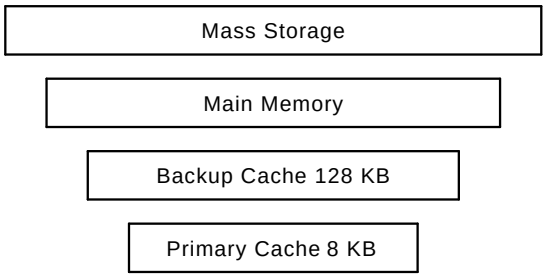
- Add figure: KA690,KA691 Cache/Memory Hierarchy



- Add figure: KA692 Cache/Memory Hierarcy



- Add figure: KA675 Cache/Memory Hierarchy



- Second paragraph, change to:

For I-stream references, the memory hierarchy starts with the VIC *for the KA680*, KA681, KA690, KA691 and KA692 CPU modules, whereas for D-stream references, the memory hierarchy starts with the Pcache. *The memory hierarchy for the KA675 for both I-stream and D-stream references starts with the Pcache.*

Page 4-2:

- Section 4.2 Virtual Instruction Cache, add the following;

Note: The KA675 does not implement the virtual instruction cache. This section pertains to the KA680, KA681, KA690, KA691 and KA692 only.

Page 4-7:

- Table 4-5 ICSR Register

Description of ENABLE bit should read:

Enable bit. When set, allows cache access to the VIC. Initializes to 0 on system reset. *Note that setting this bit on the KA675 is not supported.*

Page 4-21:

- Table 4-11 Backup Cache Size and RAMs Used

Replace table:

Cache Size	Tag Bits Used	Index Bits Used
128 kilobytes	Tag<28:17>	Index<16:5>
512 kilobytes	Tag<28:19>	Index<18:5>
2 Megabytes	Tag<28:21>	Index<20:5>

- Table 4-12 Tag and Index Interpretation Based on Cache Size

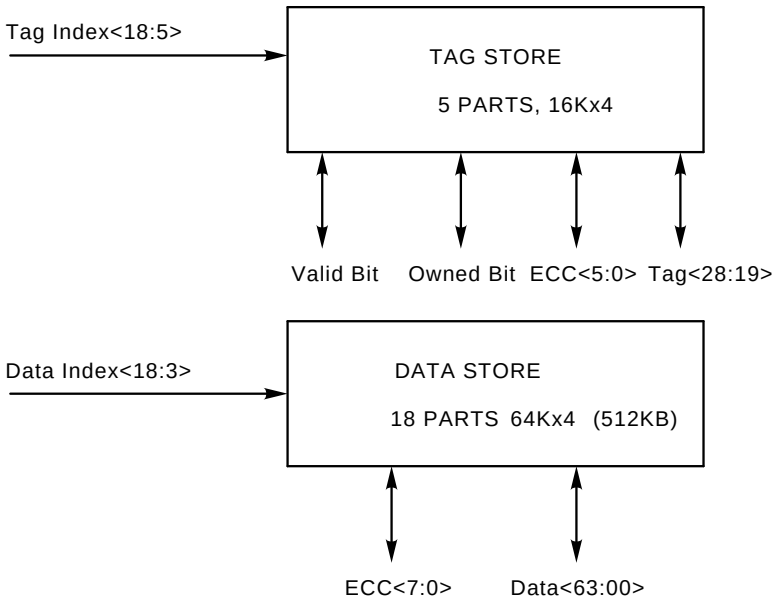
Replace table:

Cache Size	Tag RAM Size	Data RAM Size	Number of Tags	Valid Bits Per Tag
128 kilobytes	4K x 4	16K x 4	4K	1
512 kilobytes	16K x 4	64K x 4	16K	1
2 Megabytes	64K x 4	256K x 4	64K	1

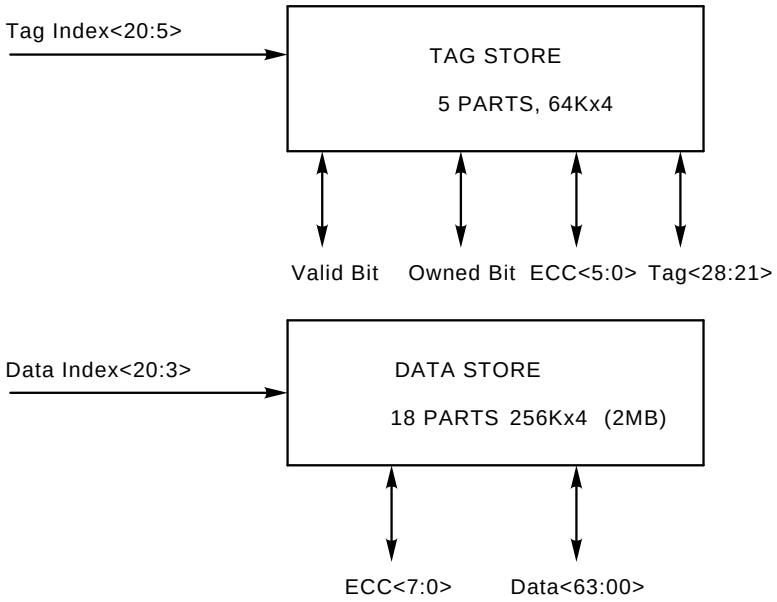
Page 4-22:

- Section 4.4.5 Backup Cache Block Diagrams

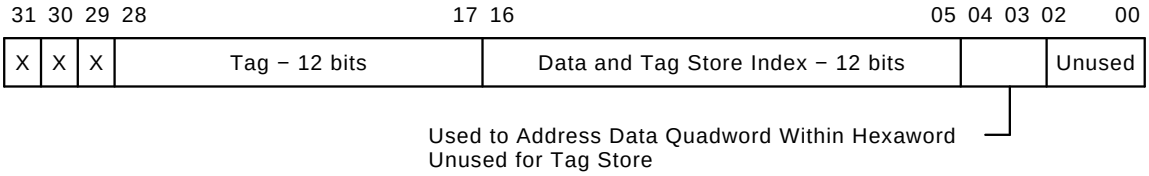
Add figure: Tags and Data for 512-Kilobyte Cache



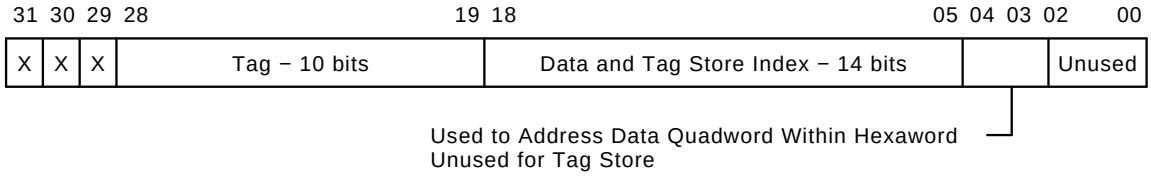
Add figure: Tags and Data for 2-Megabyte Cache



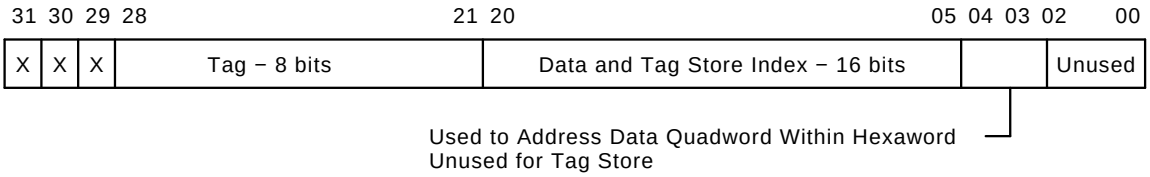
Replace Figure 4-16: Address Used for 128-Kilobyte Cache



Add figure: Address Used for 512-Kilobyte Cache



Add figure: Address Used for 2-Megabyte Cache



Page 4-25:

- Replace Table 4-13 IPR Addresss Space Decoding

IPR Group	Mnemonic[1]	IPR Address Range (hex)	Contents
Normal	---	00000000..000000FF	256 individual IPRs
Bcache Tag	BCTAG	01000000..0101FFE0[2]	4K Bcache tag IPRs (KA675,KA680, KA681), each separated by 20(hex) from the previous one
	BCTAG	01000000..0103FFE0[2]	16K Bcache tag IPRs (KA690,KA691), each separated by 20(hex) from the previous one
	BCTAG	01000000..0105FFE0[2]	64K Bcache tag IPRs (KA692), each separated by 20(hex) from the previous one
Bcache Deallocate	BCFLUSH	01400000..0141FFE0[2]	4K Bcache tag deallocate IPRs (KA675, KA680, KA681), each separated by 20(hex) from the previous one
	BCFLUSH	01400000..0143FFE0[2]	16K Bcache tag deallocate IPRs (KA690,KA691), each separated by 20 (hex) from the previous one
	BCFLUSH	01400000..0145FFE0[2]	64K Bcache tag deallocate IPRs (KA692), each separated by 20(hex) from the previous one

[1] The mnemonic is for the first IPR in the block.

[2] Unused fields in theIPR addresses for these groups should be zero. Neither hardware nor microcode detects and faults on an address in which these bits are non-zero, and they are ignored with respect to the tag or data location that is accessed.

Page 4-27:

- Table 4-15 Bcache/NDAL Processor Registers

Add entries to table:

Register Name	Mnemonic	Number (Dec)	Number (Hex)	Type	Impl	Cat
BCache Tag-KA675/KA680/KA681 (01000000 - 0101FFE0(hex))	BCTAG	--	--	RW	NVAX	2-5
BCache Deallocate-KA675/KA680/KA681 (01400000 - 0141FFE0(hex))	BCFLUSH	--	--	W	NVAX	2-5
BCache Tag-KA690/KA691 (01000000 - 0103FFE0(hex))	BCTAG	--	--	RW	NVAX	2-5
BCache Deallocate-KA690/KA691 (01400000 - 0143FFE0(hex))	BCFLUSH	--	--	W	NVAX	2-5
BCache Tag-KA692 (01000000 - 0105FFE0(hex))	BCTAG	--	--	RW	NVAX	2-5
BCache Deallocate-KA692 (01400000 - 0145FFE0(hex))	BCFLUSH	--	--	W	NVAX	2-5

Page 4-29:

- **TAG_SPEED** description: Note should be changed to read:

Note

Improper setting of this bit can prevent the NVAX CPU from functioning properly. This bit should be set to 0 (3 cycle read, 3 cycle write) for the KA690, KA691 and KA692, or 1 (4 cycle read, 4 cycle write) for the KA675, KA680 and KA681.

Page 4-30:

- **DATA_SPEED** description: Note should be changed to read:

Note

Improper setting of these bits can prevent the NVAX CPU from functioning properly. These bits should be set to 00 (binary) (2 cycle read, 3 cycle write) for the KA690 and KA691, 01 (binary) (3 cycle read, 4 cycle write) for theKA680, KA681 and KA692, or 10 (binary) (4 cycle read, 5 cycle write) for the KA675.

- **SIZE** section: Replace text with:

SIZE
These two bits are used to select the size of the Bcache as differentiated between the CPU modules. Three backup cache sizes are selectable by using the SIZE bits, as shown in Table 4-19, with the 128-kilobyte size corresponding to the KA675/KA680/KA681, the 512-kilobyte size corresponding to the KA690/KA691, and 2-Megabyte size corresponding to the KA692. These bits are cleared on reset; the 128-kilobyte cache is selected by default.

Note

The console code configures these bits at power up. Modifying them can prevent proper operation.

Page 4-31:

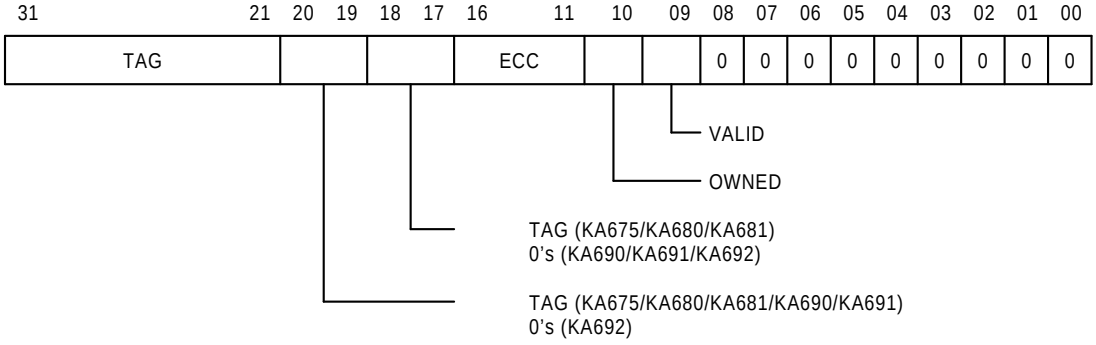
- Table 4-19 SIZE

Replace table:

SIZE<1:0>	Backup Cache Size
00	128 kilobytes
10	512 kilobytes
11	2 Megabytes

Page 4-36:

- Replace Figure 4-22 IPR Format of BCETAG



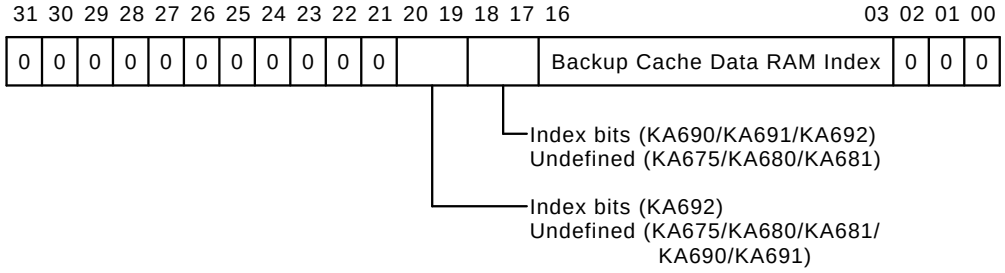
Page 4-37:

- Replace Table 4-23 TAG Interpretation

Cache Size	Tag Bits Used	Unused Tag Bits
128KB (KA675/KA680/KA681)	TAG<28:17>	TAG<31:29>
512KB (KA690/KA691)	TAG<28:19>	TAG<31:29>,<18:17>
2MB (KA692)	TAG<28:21>	TAG<31:29>,<20:17>

Page 4-40:

- Replace Figure 4-25 BCEDIDX



- Replace Table 4-26 BCEDIDX Interpretation

Cache Size	Index Bits Used	Undefined Index Bits
128 KB (KA675/KA680/KA681)	BCEDIDX<16:3>	BCEDIDX<20:17>
512 KB (KA690/KA691)	BCEDIDX<18:3>	BCEDIDX<20:19>
2 MB (KA692)	BCEDIDX<20:3>	none

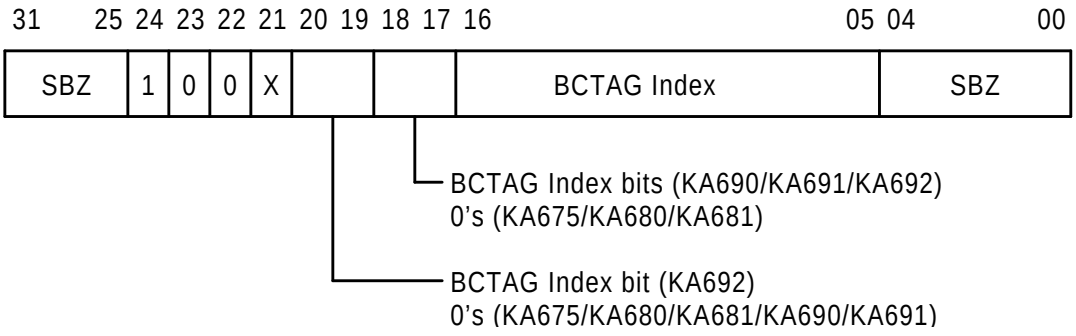
Page 4-51:

- Section 4.4.11 Backup Cache Tag Store Access Through IPR Reads and Writes (BCTAG)

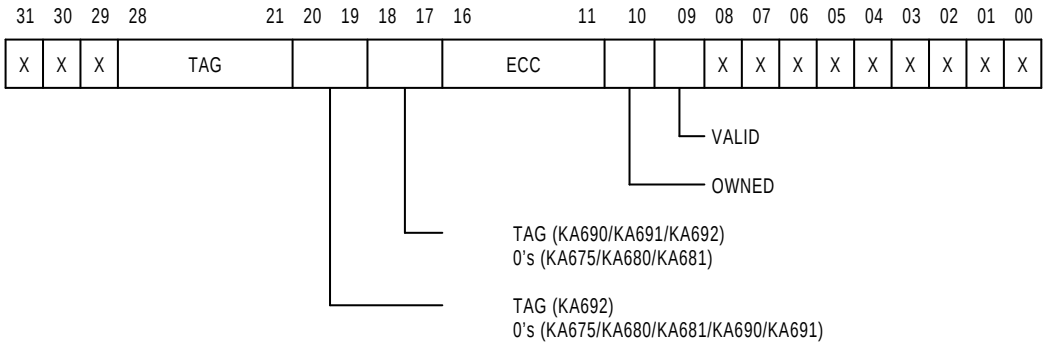
Third paragraph should read:

When the backup cache tag store is being accessed through IPR reads and writes, address bits <24:22> = 100 (BINARY). Address bits <20:5> (KA692), *<18:5> (KA690*/KA691*)* or *<16:5>* (KA675/*KA680*/KA681) are used as the index into the tag store RAMs; these indicate which backup cache location is to be written or read.

- Replace Figure 4-36 Backup Cache Tag Store IPR Addressing Format



- Replace Figure 4-37 IPR Format of the Backup Cache Tag Store



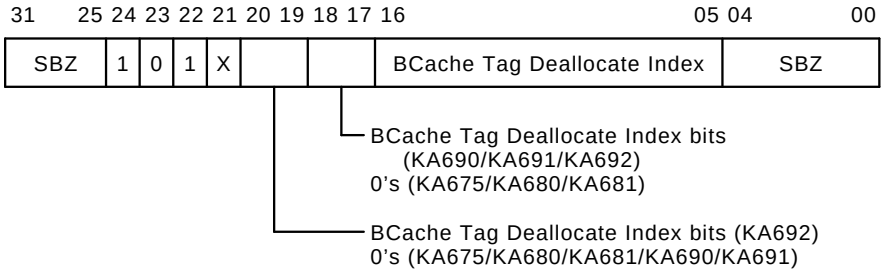
Page 4-52:

- Table 4-31 Tag and Index Interpretation for BCTAG IPR

Add entries to table:

Cache Size	Tag bits Used	Index Bits Used
128 KB (KA675/KA680/KA681)	TAG<28:17>	Index<16:5>
512 KB (KA690/KA691)	TAG<28:19>	Index<18:5>
2 MB (KA692)	TAG<28:21>	Index<20:5>

- Replace Figure 4-38 Backup Cache Deallocate IPR Addressing Format



Page 5-24:

- Table 5-8 (Cont.) Mode Control and Diagnostic Status Register, MMCDSR

Description of REF_INT_SEL should read:

When this bit is 1, the NMC uses an alternate refresh interval for use in conjunction with NDAL cycle times longer (slower) than 42 ns. The KA680 and *KA681* CPU modules operate at 42ns; *KA690 and KA691 CPU modules operate at 36ns; the KA692 CPU module operates at 30ns; therefore, for these CPU modules* this bit should not be set by software because it will cause excessive memory refresh cycles and subsequently reduce system performance. *The KA675, however, requires that this bit to be set to 1, since the cycle time is 48 ns.*

Page 6-6:

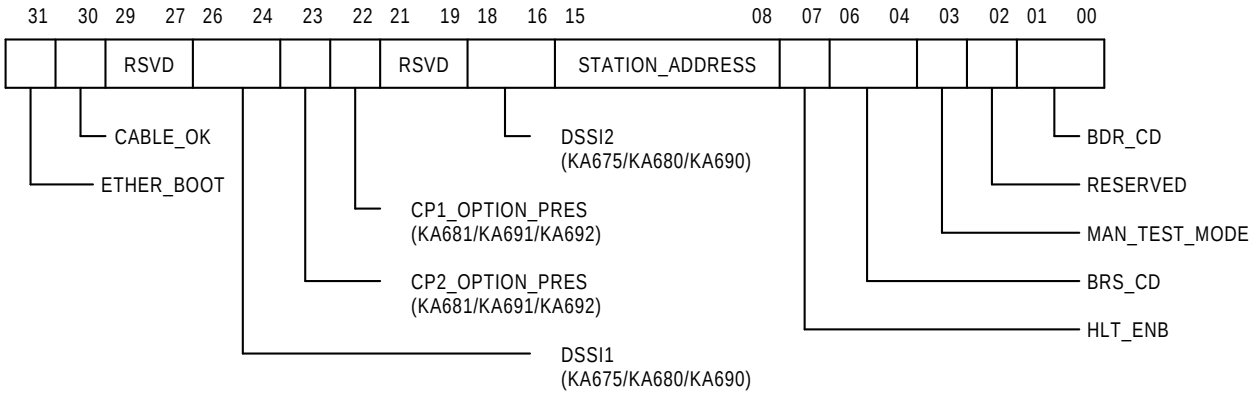
- Section 6.3.3 CP1 and CP2 Interface

Add the following text:

Note that on the KA680, KA681, KA690, KA691 and KA692 CPU modules, the CP bus cycle time is 70 ns. The KA675 CP bus cycle time is 80 ns.

Page 8-1:

- Replace Figure 8-1 Boot and Diagnostic Register (BDR)



Page 8-2:

- Table 8-1 Boot and Diagnostic Register Bit Description

Replace the following bit descriptions:

Data Bit	Name	Description
<26:24>	DSSI1	This field contains the DSSI node number for the external DSSI bus (Bus 1, accessed through the console module) *for the KA675/KA680/KA690 CPU modules only. This information is in SSC RAM location 201407F9(hex) for the KA681/KA691/KA692.*
<23>	CP2_OPT_PRES	When 0, indicates that an option module is present on the CP2 connector (KA681/KA691/KA692 only). These bits are RESERVED on the KA675/KA680/KA690.
<22>	CP1_OPT_PRES	When 0, indicates that an option module is present on the CP1 connector (KA681/KA691/KA692 only). These bits are RESERVED on the KA675/KA680/KA690.
<21:19>	Reserved	Reserved.
<18:16>	DSSI2	This field contains the DSSI node number for the internal DSSI bus (Bus 0, connected to the BA440 disks via the backplane connector, and accessed through the DSSI connector to the left of QBus slot 12) *for the KA675/KA680/KA690 CPU modules only. This information is in SSC RAM location 201407F9(hex) for the KA681/KA691/KA692.*

Page 11-5:

- Section 11.3 SHAC Registers

Replace first paragraph:

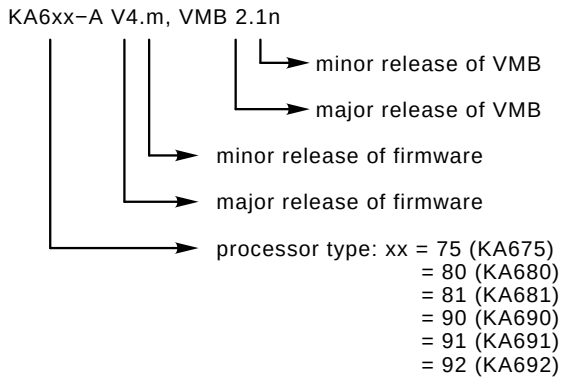
The CPU communicates directly with the *4 SHAC chips* through a set of device registers in each SHAC. These registers occupy a 1-page (512-byte) region in I/O address space, aligned on a page boundary. *The register descriptions show the addresses for SHAC1 I/O addresses.* The offsets for the other 3 SHACs are the same, the base addresses are as shown below:

SHAC1 20004000
SHAC2 20004200
SHAC3 20004400 (on KFDDB dual DSSI card option, if present)
SHAC4 20004600 (on KFDDB dual DSSI card option, if present)

Note that only the KA681, KA691 and KA692 CPU modules can support the KFDDB option. On these three modules, the two native SHAC DSSI IDs established by the node ID plugs may be overriden by the SET DSSI_ID console command. The optional SHAC3 and SHAC4 DSSI IDs default to the SHAC1 and SHAC2 ID plug values, respectively, and may also be overridden by the SET DSSI_ID console command. Note also that reading SHAC3 or SHAC4 registers with no option card present will cause an exception. Check the CPn_OPT_PRES in the Boot and Diagnostic register before accessing these registers.

Page 12-8:

- Replace Figure 12-2 Console Banner:



Page 12-27:

- Table 12-6 Command, Parameter, and Qualifier Keywords

Add entries to table:

SET & SHOW Parameter Keywords		
CONTROLP	DSSI_ID	PSE
PSWD	SAVED_STATE	

Page 12-50:

- Section 12.2.9 Console Commands (cont.) (This section begins on page 12-34)

Add LOGIN command:

LOGIN

Format

LOGIN

Qualifiers

None.

Arguments

None.

Description

Exit from the secure console by entering the password at the prompt. The LOGIN command may only be executed while in secure console mode.

Examples

```
>>>sho pse    ! in secure console mode
?63 ILLEGAL COMMAND    ! this command is illegal in this mode
>>>login
Password:  ! enter password to enter privileged mode
>>>sho pse
Enabled
>>>set pse 0  ! now set secure console switch off
>>>
```

Page 12-58:

- **SET** console command description

Add to **Parameters** list:

DSSI_ID
Sets the DSSI node ID for each adapter. Ther first parameter is the bus number. The second parameter is the ID, or "F" to revert to the bus ID plug.

Page 12-60:

- **SET** console command description (continued from page 12-58)

Add to **Parameters** list :

PSE
Once a password has been set, the state of the secure console enable bit, PSE, will determine whether the secure console mode will be entered when certain console commands are executed. If PSE = 0 (disabled), the console will remain in privileged mode even if a password has been set. If PSE = 1 (enabled), the console will enter into secure mode when the following commands are executed:

BOOT (with any supplied parameters)
CONTINUE
HALT
START

Once in secure mode, the only commands which may be executed are BOOT (with no qualifiers) and LOGIN (in order to enter the password and exit into privileged mode). Since the BOOT command will take no qualifiers in secure console mode, it is advisable to SET BOOT and SET BFLG prior to exiting privileged mode.

PSWD
Set password to be entered in order to exit from secure console to privileged console. A 16-character password must be typed at the "PSWD1:" prompt. The password must be typed again for verification at the "PSWD2:" prompt.

Page 12-61:

- **SET** console command description (cont.)

Add to **Examples**:

```
>>>sho dssi_id
DSSI Bus 0/A = ID 6  determined by Bus 0 ID PLUG
DSSI Bus 1/B = ID 7  determined by Bus 1 ID PLUG
DSSI Bus 2/C = ID 6  determined by Bus 0 ID PLUG
DSSI Bus 3/D = ID 7  determined by Bus 1 ID PLUG
>>>set DSSI_ID 0 5          ! change Bus 0 ID

            WARNING !
   Bus 0 ID may not match ID PLUG
   SET DSSI_ID 0 F, restores use of ID PLUG

>>>sho dssi_id
DSSI Bus 0/A = ID 5  determined by SET DSSI_ID command, Bus 0 ID PLUG ignored
DSSI Bus 1/B = ID 7  determined by Bus 1 ID PLUG
DSSI Bus 2/C = ID 6  determined by Bus 0 ID PLUG
DSSI Bus 3/D = ID 7  determined by Bus 1 ID PLUG
>>>set dssi_id C 4          ! change Bus 2/C ID.  Can specify either 2 or C.
>>>sho dssi_id
DSSI Bus 0/A = ID 5  determined by SET DSSI_ID command, Bus 0 ID PLUG ignored
DSSI Bus 1/B = ID 7  determined by Bus 1 ID PLUG
DSSI Bus 2/C = ID 4  determined by SET DSSI_ID command
DSSI Bus 3/D = ID 7  determined by Bus 1 ID PLUG
>>>set dssi_id A F          ! revert back to Bus 0/A ID plug
>>>sho dssi_id
DSSI Bus 0/A = ID 6  determined by Bus 0 ID PLUG
DSSI Bus 1/B = ID 7  determined by Bus 1 ID PLUG
DSSI Bus 2/C = ID 4  determined by SET DSSI_ID command
DSSI Bus 3/D = ID 7  determined by Bus 1 ID PLUG
>>>
```

Page 12-62:

- **SHOW** console command description:

Add to **Parameters** list:

DSSI_ID
Lists the DSSI node ID for each adapter.

Page 12-63:

- **SHOW** console command description (cont.)

Add to **Parameters** list:

SAVED_STATE
Lists all the non-volatile console parameter values stored in FEPROM. These values include DSSI_ID, SCSI_ID, BOOT device, BFLG, HALT action, LANGUAGE.

Page A-3

- Section A.1.5 USER Area

Add the following:

For the KA681/KA691/KA692, the DSSI node IDs are read from a fixed word location in SSC RAM at physical address 201407F9(hex). There are 16 bits total; 4 PRESENT bits and 12 (4x3) ID bits.

Add the following chart:

Bits	Name	Function
0	DSSI_B0_pres	If 1, DSSI Bus 0 (SHAC2)* present.
1	DSSI_B1_pres	If 1, DSSI Bus 1 (SHAC1)* present.
2	DSSI_B2_pres	If 1, DSSI Bus 2 (SHAC3) present.
3	DSSI_B3_pres	If 1, DSSI Bus 3 (SHAC4) present.
4:6	DSSI_ID_B0	3 bit DSSI ID Bus 0 SHAC2* node number
7:9	DSSI_ID_B1	3 bit DSSI ID Bus 1 SHAC1* node number
10:12	DSSI_ID_B2	3 bit DSSI ID Bus 2 SHAC3 node number
13:15	DSSI_ID_B3	3 bit DSSI ID Bus 3 SHAC4 node number

* Note that SHAC2 sits on DSSI Bus 0, SHAC1 sits on DSSI bus 1.

Page G-12:

- Section G.3 DC Power Consumption

Replace power requirements table with the following:

Module	Current (Amps)				Power (Watts) (total)	QBus loads	
	+5 Vdc	+3.3 Vdc	+12 Vdc	−12 Vdc		ac	dc
MS690−BA	5.3 A	0.0 A	0.0 A	0.0 A	26.5 W	0	0
MS690−CA	4.2 A	0.0 A	0.0 A	0.0 A	21.0 W	0	0
MS690−DA	6.4 A	0.0 A	0.0 A	0.0 A	32.0 W	0	0
KA675−AA(3)	3.6 A	2.8 A	1.6 A	0.0 A	46.4 W	4	1
KA680−AA(3)	4.8 A	3.2 A	1.6 A	0.0 A	53.8 W	4	1
KA681−AA(3)	7.6 A	(5)	1.6 A	0.0 A	57.2 W	4	1
KA690−AA(3)	5.8 A	3.5 A	1.6 A	0.0 A	59.8 W	4	1
KA691−AA(3)	9.1 A	(5)	1.6 A	0.0 A	64.7 W	4	1
KA692−AA(3)	9.2 A	(5)	1.6 A	0.0 A	65.2 W	4	1

NOTES:
1) MS690 current and power values are unique depending on option.
2) Memory modules are in dedicated slots 4 through 1.
3) Power data includes CPU module, H3604 & Backplane power.
4) H3604 & Backplane power: 2.0 A @ +5 Vdc, 1.6 A @ +12 Vdc.
5) Total output power from +3.3 Vdc and +5 Vdc must not exceed 330 watts.
6) +3.3 Vdc generated from on−board regulator for KA681−AA, KA691−AA, KA692−AA.

Page I-3:

- Add to KA680 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

```
 SHAC3 address space (CP1_OPT_PRES=0 in BDR<22>)

    Reserved Local Register I/O Space    2000 4400 - 2000 442F
    SHAC3 SSWCR                          2000 4430
    Reserved Local Register I/O Space    2000 4434 - 2000 4443
    SHAC3 SSHMA                          2000 4444
    SHAC3 PQBBR                          2000 4448
    SHAC3 PSR                            2000 444C
    SHAC3 PESR                           2000 4450
    SHAC3 PFAR                           2000 4454
    SHAC3 PPR                            2000 4458
    SHAC3 PMCSR                          2000 445C
    Reserved Local Register I/O Space    2000 4460 - 2000 447F
    SHAC3 PCQ0CR                         2000 4480
    SHAC3 PCQ1CR                         2000 4484
    SHAC3 PCQ2CR                         2000 4488
    SHAC3 PCQ3CR                         2000 448C
    SHAC3 PDFQCR                         2000 4490
    SHAC3 PMFQCR                         2000 4494
    SHAC3 PSRCR                          2000 4498
    SHAC3 PECR                           2000 449C
    SHAC3 PDCR                           2000 44A0
    SHAC3 PICR                           2000 44A4
    SHAC3 PMTCR                          2000 44A8
    SHAC3 PMTECR                         2000 44AC

 SHAC4 address space (CP1_OPT_PRES=0 in BDR<22>)

    Reserved Local Register I/O Space    2000 4600 - 2000 462F
    SHAC4 SSWCR                          2000 4630
    Reserved Local Register I/O Space    2000 4634 - 2000 4643
    SHAC4 SSHMA                          2000 4644
    SHAC4 PQBBR                          2000 4648
    SHAC4 PSR                            2000 464C
    SHAC4 PESR                           2000 4650
    SHAC4 PFAR                           2000 4654
    SHAC4 PPR                            2000 4658
    SHAC4 PMCSR                          2000 465C
    Reserved Local Register I/O Space    2000 4660 - 2000 467F
    SHAC4 PCQ0CR                         2000 4680
    SHAC4 PCQ1CR                         2000 4684
    SHAC4 PCQ2CR                         2000 4688
    SHAC4 PCQ3CR                         2000 468C
    SHAC4 PDFQCR                         2000 4690
    SHAC4 PMFQCR                         2000 4694
    SHAC4 PSRCR                          2000 4698
    SHAC4 PECR                           2000 469C
    SHAC4 PDCR                           2000 46A0
    SHAC4 PICR                           2000 46A4
    SHAC4 PMTCR                          2000 46A8
    SHAC4 PMTECR                         2000 46AC
Reserved Local Register I/O Space    2000 46B0 - 2000 7FFF
```

Pages J-1 through J-8:

- Replace Appendix J Configurable Machine State with updated version on the following pages:

Configurable Machine State

The KA675, KA680, KA681, KA690, KA691 and KA692 CPU modules have many control registers that need to be configured for proper operation of the modules. The following list shows the normal state of all configurable bits in the CPU modules as they are left after the successful completion of power-up ROM diagnostics.

KA675, KA680, KA681, KA690, KA691, KA692 Configuration registers and writable bits: (* = indicates the default state of bit at power-up, before any console code is executed)

All address values are hexidecimal.

NCA:

CMCDSR: Mode Control and Diagnostic Status Register (2102 0004)

15:14: CP2 MT Timer Prescaler
11 = 144000 cycles* - needed for CQBIC 10ms No Grant timeout

13:12: CP1 MT Timer Prescaler
00 = 144 cycles - minimum for passive releases, no cycle should take longer than this

11:10: NDAL Timeout Prescaler
00 = 3200 cycles* - this is longer than both NCA and NMC transactions timeouts, preserves timeout order

9: QBUS_TRANS enable (formerly CQBIC_PRESENT)
0 = QBUS_TRANS signal disabled* - this is to avoid QBUS_TRANS deadlock

8: IO2 ID enable
1 = enabled

7: Force wrong CP2 bus parity
0 = off* - diagnostic use only

6: Force wrong CP1 bus parity
0 = off* - diagnostic use only

5: Force wrong NDAL master parity
0 = off* - diagnostic use only

4: Force wrong NDAL slave parity
0 = off* - diagnostic use only

3: Enable prefetch
1 = enable CP bus prefetch on DMA reads

2: Force write buffer hit
0 = off* - diagnostic use only

1: Force CP2 bus owner
0 = disabled - diagnostic use only

0: Force CP1 bus owner
0 = disabled - diagnostic use only

ICCS: Interval Clock Control and Status Register (2100 0060)
NOTE: VMS sets ICCS, NICR to proper values

6: Interrupt enable
0 = disabled*

5: Single step
0 = off*

4: Transfer
0 = disabled*

0: Run - increment every 1µs
0 = do not increment*

NICR: Next Interval Count Register (2100 0064)
31:0 Initial count value for ICR (FFFFD8F0* (10ms))

NMC:

MEMCON_0-7: Memory Configuration Registers (2101 8000 thru 2101 801C)
NOTE: Diagnostics set these registers based on available memory

31: Base Address Valid
0 = not valid*
1 = valid

28:24: Base Address (0 on reset)
1MB RAM - all address bits used
4MB RAM - only <28:26> used

2:1 RAM size
00 = 1MB RAM*
01 = 1MB RAM
10 = 4MB RAM
11 = non-existent bank

0: Mode
1 = 64-bit mode

MMCDSR: Mode Control and Diagnostic Status Register (2101 8048)

31: Fast Diagnostic Mode (FDM)
0 = disabled* - diagnostic use only

30: FDM Second pass
0 = disabled* - diagnostic use only

29: Diagnostic Checkbit mode
0 = disabled* - diagnostic use only

28: QBus on I01
0 = QBus on IO2*

27: Enable soft error log (NDAL & memory related)
0 = disabled* - VMS enables this

26: Flush BCache
0 = don't flush*

24:17: Memory diagnostic check bits
0 - meaningful only in diagnostic check mode* (may or may not be read as 0)

8:7: NDAL Timeout Scaler
00 = 2600 cycles* - maximum, to preserve timeout order

6: Disable memory error
0 = memory errors detected and corrected*

5: Refresh interval timer select
0 = 328 cycles* (KA680,KA681.KA690,KA691,KA692)
1 = 244 cycles (KA675)

4:2: Force wrong parity on NDAL transactions
0 = off* - diagnostic use only

1: Disable memory refresh
0 = memory refreshed*

0: Force refresh
0 = normal refresh*

MOAMR: O-bit Address and Mode Register (2101 804C)

16: Ignore O-bit mode
0 = O-bits checked*

15: Disable O-bit error
0 = O-bit errors detected*

14:6: O-bit segment address (0*) - meaningful only during O-bit data register access

5:3: O-bit mask (0*) - meaningful only during O-bit data register access

2:0: O-bit operation mode
000 = reconstruction mode* - meaningful only during O-bit data register access

MODR: O-bit Data Registers (2101 0000 thru 2101 7FFF)

23:12: O-bit field 1 (0*) - used only during Fast Memory test

11:0: O-bit field 0 (0*) - used only during Fast O-bit test mode

NVAX:

CPUID: CPU ID Register (IPR E)

7:0: CPU identifcation = 0 (for single processor config.)

SID: System Identification Register (IPR 3E)

NOTE: this register may only be written by microcode

31:24: CPU type - 13(hex) (NVAX code)

13:8: Patch revision

7:0: Microcode revision

ICSR: IBox Control and Status Register (IPR D3)

0: VIC enable
0* = disabled (KA675)
1 = enabled (KA680, KA681, KA690, KA691, KA692)

ECR: EBox Control Register (IPR 7D)

13: FBox test enable
0 = disabled* - diagnostic use only

7: Interval time mode
1 = full CPU implemented interval timer

5: S3 stall timeout
0 = counts cycles w/ timeout_enable asserted* (~3 sec)

3: FBox stage 4 bypass
1 = enabled - result from stage 3 passed directly to FBox output interface (improves FBox latency)

2: S3 external time base timeout
0 = disabled* - use internal time base

1: FBox enable
1 = enabled

0: Vector present
0 = no* - no vector option available at this time

MMAPEN: Memory Map Enable Register (IPR E6)

0: Memory map enable
0 = disabled* - VMS enables this

PAMODE: Physical Address Mode Register (IPR E7)

0: Physical address mode
0 = 30-bit physical address space*

PCCTL: PCache Control Register (IPR F8)

8: PCache Electrical disable
0 = PCache enabled*

7:5 MBox performance monitor mode
0 - diagnostic use only*

4: PCache error enable
1 = enables PCache error detection

3: Bank select during force hit mode
0 = left bank selected if force hit mode enabled*
- diagnostic use only

2: Force hit
0 = disabled* - diagnostic use only

1: I_enable
1 = enable PCache for IREAD, INVAL, I_CF commands

0: D_enable
1 = enable PCache for INVAL, D-stream read/write/fill commands

CCTL: CBox Control Register (IPR A0)

30: Software ETM
0 = disabled* - diagnostic use only

16: Force NDAL parity error
0 = off* - diagnostic use only

15:11: Performance monitoring BCache access and hit type
0 = configures BCache for performance monitoring*
meaningful only during performance monitoring

10: Disable CBox write packer
0 = write packer enabled* - improves write latency

9: Read timeout counter test
0 = test disabled* - use external time base for read timeout counter

8: Software ECC
0 = use correct ECC*

7: Disable BCache errors
0 = BCache errors detected*

6: Force Hit
0 = disabled* - diagnostic use only

5:4: BCache size
00 = 128 KB* (KA675,KA680,KA681)
10 = 512 KB (KA690,KA691)
11 = 2 MB (KA692)

3:2: Data store speed
00 = 2 cycle read, 3 cycle write* (KA690,KA691)
01 = 3 cycle read, 4 cycle write (KA680,KA681,KA692)
10 = 4 cycle read, 5 cycle write (KA675)

1: Tag store speed
0 = 3 cycle read, 3 cycle write* (KA690,KA691,KA692)
1 = 4 cycle read, 4 cycle write (KA675,KA680,KA681)

0: Enable BCache
1 = enabled

CQBIC:

SCR: System Configuration Register (2008 0000)

14: Halt enable
1 = BHALT to CQBIC HALTIN pin to cause halts

12: Page prefetch disable
1 = map prefetch disabled - historical latency reasons

7: Restart enable
0 = QBus restart causes ARB power-up reset*

3:1: ICR offset address select bits
0 = no effect (AUX mode not supported)*

ICR: Interprocessor Communication Register (2000 1F40)

8: AUX Halt
0 = no halt (AUX mode not supported)

6: ICR interrupt enable
0 = interprocessor interrupts disabled - only uniprocessor config. allowed

5: Local memory external access enable
0 = external access disabled* - VMS will configure map

QBMBR: Q-Bus Map Base Address Register (2008 0010)

28:15: address where 8K QBus mapping registers are located (VMS reconfigures map)

SHAC:

NOTE: all SHAC registers are subsequently configured by VMS driver. SHAC1 addresses shown. Base address for SHAC2 = 2000 4200, SHAC3 = 2000 4400, SHAC4 = 2000 4600.

PQBBR: Port Queue Block Base Register (2000 4048)

20:0: upper bits of physical address of base of Port Queue block. Contains HW version, FW version, shared host memory version and CI port maintenance ID at power-up.

PPR: Port Parameter Register (2000 4058)

31:29: Cluster size. For SHAC value = 0.

28:16: Internal buffer length = 0* (For SHAC value = 1010(hex))

7:0: Port number. Same as SHAC's DSSI ID.

PMCSR: Port Maintenance Control and Status Register (2000 405C)

2: Interrupt enable
0 = disabled*

1: Maintenance timer disable
0 = enabled*

SGEC:

NOTE: all SGEC registers are susequently configured by VMS driver

NICSR0: Vector Address, IPL, Synch/Asynch Register (2000 8000)

31:30: Interrupt priority
00 = 14*

29: Synch/Asynch bus master operating mode
0 = asynchronous*

15:0: Interrupt vector = 0003(hex)*

NICSR6: Command and Mode Register (2000 8018)

30: Interrupt enable
0 = disabled*

28:25: Burst limit mode
maximum number of longwords transferred in a single DMA burst. 1*,2,4,8 when NICSR6<19> is 0 (1*,4 when NICSR6<19> is 1).

20: Boot message enable mode
0 = disabled*

19: Single cycle enable mode
0 = disabled*

11: Start/Stop transmission command
0 = SGEC transmission process in stopped state*

10: Start/Stop reception command
0 = SGEC reception process in stopped state*

9:8: Operating mode
00 = normal mode*

7: Disable data chaining mode
0 = frames too long for current receive buffer will be transferred to the next buffer(s) in receive list*

6: Force collision mode (internal loopback mode only)
0 = no collision*

3: Pass bad frames mode
0 = bad frames discarded*

2:1: Address filtering mode
00 = normal mode*

NICSR7: System Base Register (2000 801C)

29:0: System base address - physical starting address of the VAX system page table (unpredictable after reset)

NICSR9: Watchdog Timers Register (2000 8024)

31:16: Receive watchdog timeout
0 = never timeout*
default = 1250 = 2 ms
range = 72 µs (45) to 100 ms

15:0: Transmit watchdog timeout
0 = never timeout*
default = 1250 = 2 ms
range = 72 µs (45) to 100 ms

SSC:

SSCBAR: SSC Base Address Register (2014 0000)

29:0 20140000(hex) = Base address*

SSCCR: SSC Configuration Register (2014 0010)

27: Interrupt vector disable
0 = interrupt vector enabled*

25:24: IPL Level
00 = 14*

23: ROM access time
0 = 350 ns*

22:20: ROM size
101 = 256KB

18:16: Halt protected space
101 = 20040000 - 2007FFFF(hex) (historical)

15: Control P enable
0 = 20 spaces recognized as break*, not control-p (historical)

14:12: Terminal UART baud rate
101 = 9600 (historical)

6: Programmable address strobe 1 ready enable (for BDR)
1 = ready asserted after address strobe

5:4: Programmable address strobe 1 enable (for BDR)
11 = read enabled, write enabled

2: Programmable address strobe 0 ready enable
0 = no ready after address strobe* - not used

1:0: Programmable address strobe 0 enable
00 = read disabled, write disabled* - not used

RXCS: Console Receiver Control and Status Register (2014 0080)

6: Interrupt enable
0 = disabled* - polled in console mode

TXCS: Console Transmitter Control and Status Register (2014 0088)

6: Interrupt enable
0 = disabled*

2: Loopback enable
0 = disabled* - diagnostic use only

0: Break transmit
0 = terminate SPACE condition*

CBTCR: SSC Bus Time Out Register (2014 0020)

23:0: Bus timeout interval = 4000(hex) (16.384 ms)
range = 1 to FFFFFF(hex) (1 µs to 16.77 sec)

ADS0MTR: Programmable Address Strobe 0 Match Register (2014 0130)

29:2: Match address
0 = disabled* (this strobe is used during EEPROM reprogramming only)

ADS0MKR: Programmable Address Strobe 0 Mask Register (2014 0134)

9:2: Mask address bits (used during EEPROM reprogramming)

BDMTR: Programmable Address Strobe 1 Match Register (2014 0140)

29:2: Match address = 20084000(hex) (for BDR)

BDMKR: Programmable Address Strobe 1 Mask Register (2014 0144)

29:2: Mask address bits = 7C(hex) (for BDR)

TCR0: Programmable Timer 0 Control Register (2014 0100)

6: Interrupt enable
0 = disabled*

2: STP
0 = run after overflow*

0: RUN
0 = counter not running* (historical)

TCR1: Programmable Timer 1 Control Register (2014 0110)

6: Interrupt enable
0 = disabled*

2: STP
0 = run after overflow*

0: RUN
1 = counter incrementing every microsecond (historical)

TNIR0: Programmable Timer 0 Next Interval Register (2014 0108)

31:0: 0* = Timer next interval count (use 2's complement)
range = 0* to 1.2 hours

TNIR1: Programmable Timer 1 Next Interval Register (2014 0118)

31:0: F = Timer next interval count (use 2's complement)
range = 0* to 1.2 hours

TIVR0: Programmable Timer 0 Interrupt Vector Register (2014 010C)

9:2: Timer interrupt vector = 78(hex)

TIVR1: Programmable Timer 1 Interrupt Vector Registers (2014 011C)

9:2: Timer interrupt vector = 7C(hex)

TODR: Time of Year Register (2014 006C)

1:0: Number of 10 ms intervals since last written

DLEDR: Diagnostic LED Register (2014 0030)

3:0: Display bits
0 = LEDs on* (historical)