DIGITAL Server 7300/7300R Series

Service Manual

Part Number: EK-K9FWW-SG. A01

This manual is for anyone who services a DIGITAL Server 7300/7300R Series system. It covers installation, power-up, initial troubleshooting, and component installation.

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Preface

Document Audience

This manual is written for the customer service engineer.

Document Structure

This manual uses a structured documentation design. Topics are organized into small sections for efficient online and printed reference. Each topic begins with an abstract, followed by an illustration or example, and ends with descriptive text.

This manual has nine chapters, as follows:

- **Chapter 1, System Overview,** introduces the DIGITAL Server 7300/7300R series pedestal and cabinet systems and gives an overview of the system bus modules.
- **Chapter 2, Power-Up**, provides information on how to interpret the power-up display on the operator control panel, the console screen, and system LEDs. It also describes how hardware diagnostics execute when the system is initialized.
- **Chapter 3, Troubleshooting,** describes troubleshooting during power-up and booting, as well as the **test** command.
- **Chapter 4, Power System**, describes the DIGITAL Server 7300/7300R power system
- **Chapter 5, Error Detection with Error Registers,** describes the error registers used to hold error information.
- **Chapter 6, Removal and Replacement,** describes removal and replacement procedures for field-replaceable units (FRUs).
- **Chapter 7, Running Utilities**, explains how to run utilities such as the EISA Configuration Utility and RAID Standalone Configuration Utility.

- **Chapter 8, SRM Console Commands and Environment Variables,** summarizes the commands used to examine and alter the system configuration.
- **Chapter 9, Operating the System Remotely**, describes how to use the remote console monitor (RCM) to monitor and control the system remotely.

Documentation Titles

The following table lists titles related to DIGITAL Server 7300/7300R series systems.

DIGITAL Server 7300/7300R Series Documentation

Title	Order Number
DIGITAL 7300/7300R Series User and Configuration Documentation Kit	QC-06DAC-H8
System Drawer User's Guide	ER-K9FWW-UA
Configuration and Installation Guide	ER-K9FWW-IA
Illustrated Parts Breakdown	ER-K9FWW-IP
CPU Installation Card	ER-PD02U-IN
Memory Installation Card	ER-ACSMA–IN
Power Supply Installation Card	ER–H7291–IN
ServerWORKS Manager Administrator User's Guide	ER–4QXAA–UA

Information on the Internet

Using a Web browser, you can access information about DIGITAL Servers at:

`http://www.windowsnt.digital.com/products`

Access the latest system firmware either with a Web browser as follows:

`http://www.windowsnt.digital.com/support`

1
System Overview

This chapter introduces the DIGITAL Server 7300/7300R series systems. These systems are available in cabinets or pedestals.

The pedestal system has one system drawer and up to three StorageWorks shelves. The cabinet system can have a combination of system drawers and StorageWorks shelves that occupy the five sections of the cabinet. There is one system drawer, the BA30A, used with the DIGITAL Server 7300/7300R series.

Topics in this chapter include the following:

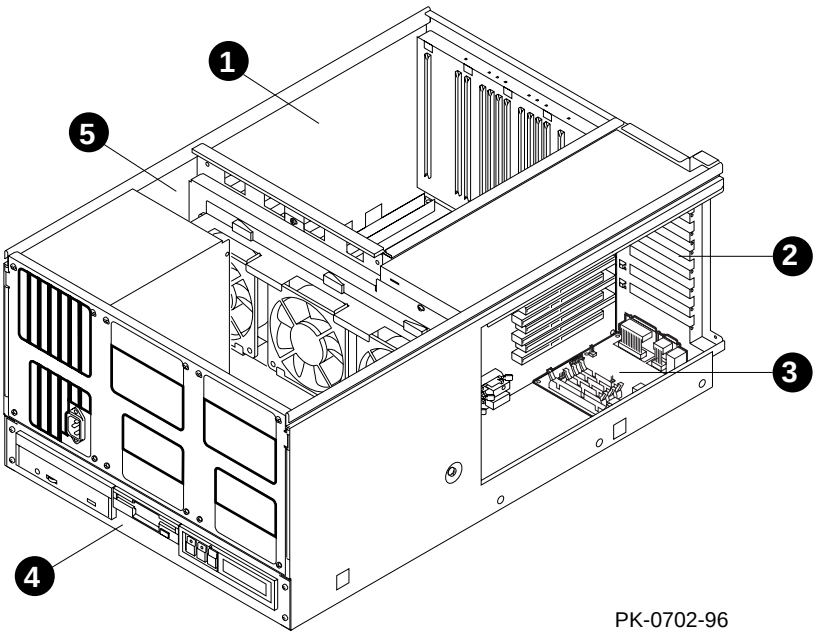
- DIGITAL Server 7300/7300R System Drawer (BA30A)
- Cabinet System
- Pedestal System
- Control Panel and Drives
- System Consoles
- System Architecture
- System Motherboard
- CPU Types

- Memory Modules
- System Bus
- System Bus to PCI Bus Bridge Module
- PCI I/O Subsystem
- Server Control Module
- Power Control Module
- Power Supply

DIGITAL Server 7300/7300R System Drawer (BA30A)

Components in the BA30A system drawer are located in the system bus card cage, the PCI card cage, the control panel assembly, and the power and cooling section. The drawer measures 30 cm x 45 cm (11.8 in. x 17.7 in.) and fully configured weighs approximately 45.5 kg (~100 lbs).

Figure 1-1 Components of the BA30A System Drawer



When the system drawer is in a pedestal, the control panel assembly is mounted in a tray at the top of the drawer.

The numbered callouts in Figure 1-1 refer to components of the system drawer.

❶ System card cage, which holds the system motherboard and the CPU, memory, bridge, and power control modules.

❷ PCI/EISA card cage, which holds the PCI motherboard, option cards, and server control module.

❸ Server control module, which holds the I/O connectors and remote console monitor.

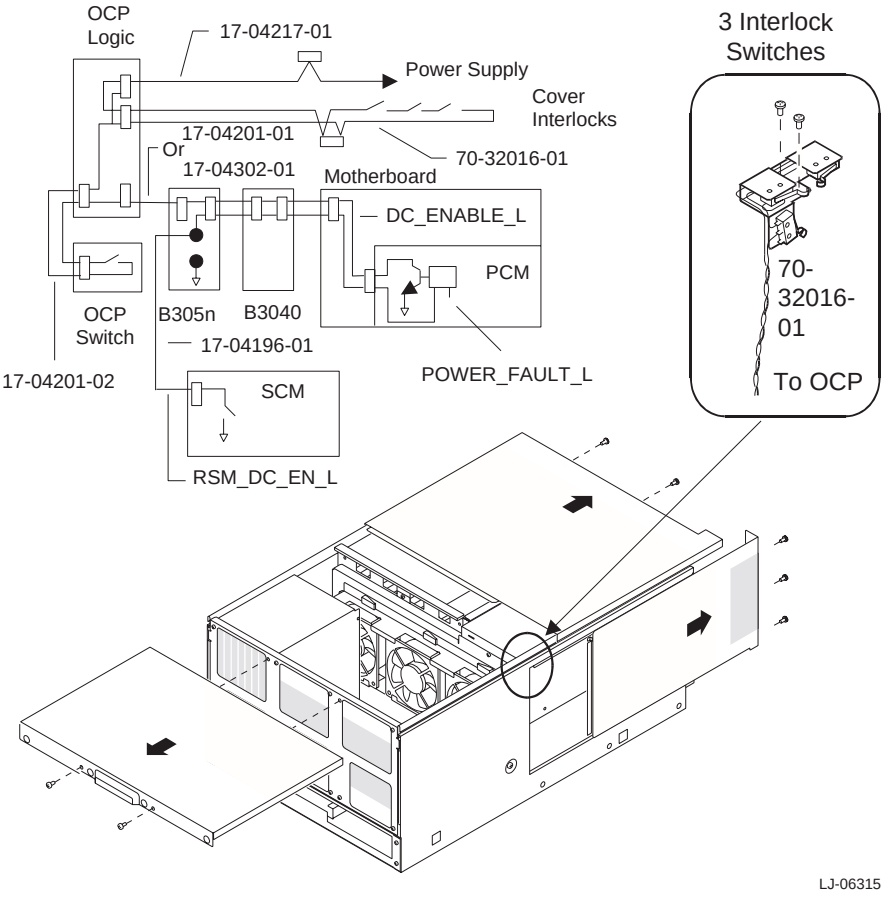
❹ Control panel assembly, which includes the control panel, a floppy drive, and a CD-ROM drive.

❺ Power and cooling section, which contains one to three power supplies and fans.

Cover Interlocks

The system drawer has three cover interlocks: one for the system bus card cage, one for the PCI card cage, and one for the power and system fan area. Figure 1-2 shows the cover interlock circuit. Note that “B305n” in Figure 1-2 stands for either the B3050-AA or B3052-AA PCI Motherboard.

Figure 1-2 Cover Interlock Circuit

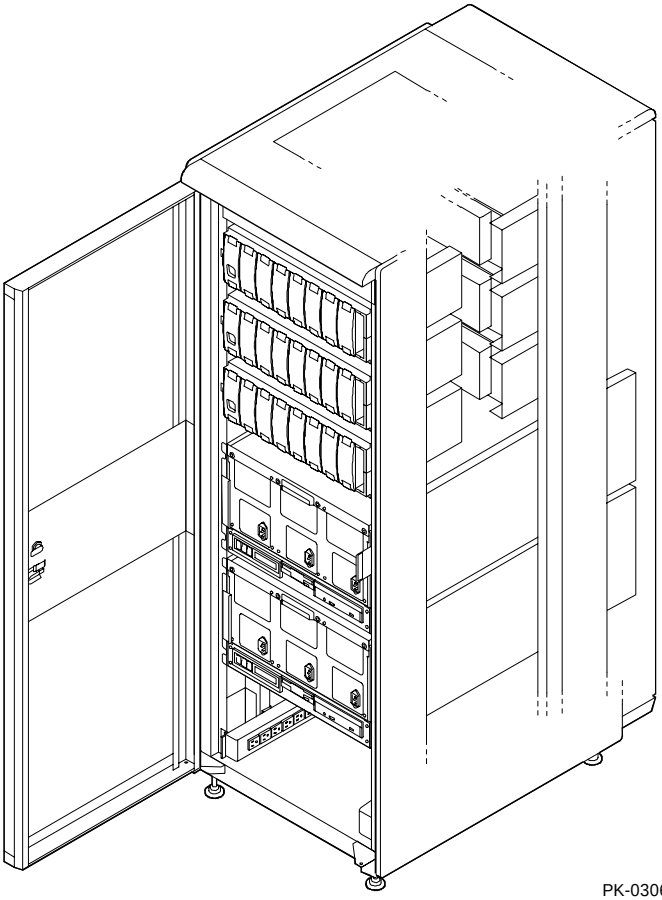


NOTE: The cover interlocks must be engaged to enable power-up. To override the cover interlocks, find a suitable object to close the interlock circuit.

Cabinet System

The DIGITAL Server 7300/7300R series cabinet system can accommodate multiple systems in a single cabinet. There are two cabinet variations that can hold different system configurations. From the outside, the cabinets look almost identical and are of one basic type. The differences are in power controllers.

Figure 1-3 DIGITAL Server 7300/7300R Cabinet System



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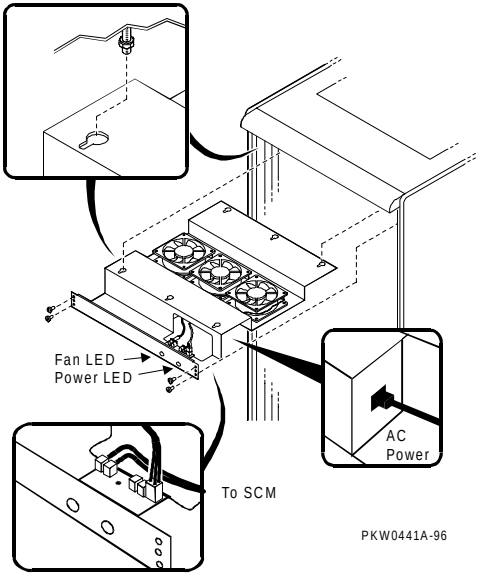
Cabinet Differences

Cabinet	Power	Mounting	Destination
H9A10-EN	Two 120 volt H7600-AA power controllers	Pull-out tray (max drawers: 3)	North America Asia Pacific
H9A10-EP	Two 240 volt H7600-DB power controllers	Pull-out tray (max drawers: 3)	Europe

Cabinet System Fan Tray

At the top of cabinet systems is a fan tray containing three exhaust fans, a small 12-volt power supply, and a module that distributes power to the server control module in each drawer.

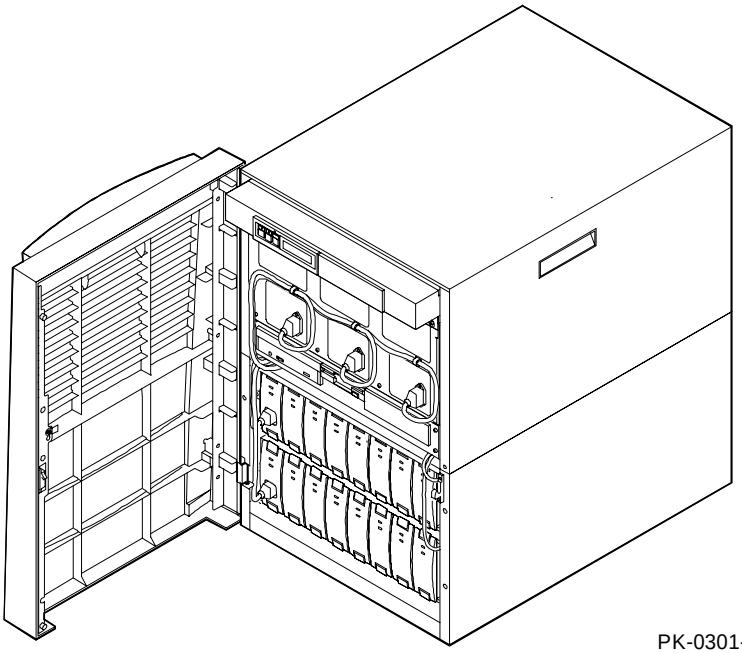
Figure 1-4 Cabinet Fan Tray



Pedestal System

The pedestal system contains one system drawer with a control panel, a CD-ROM drive, and a floppy drive. In the pedestal control panel area there is space for an optional tape or disk drive. Three StorageWorks shelves provide up to 90 Gbytes of in-cabinet storage.

Figure 1-5 Pedestal System Front



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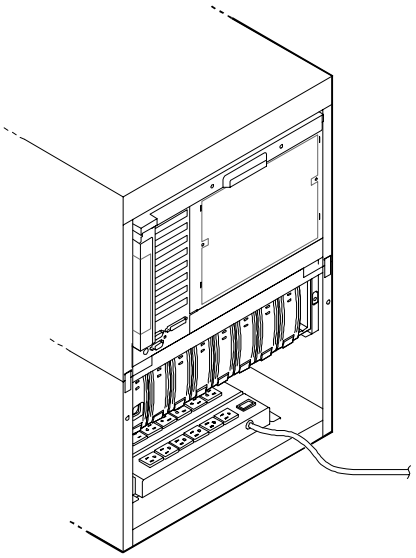
In the pedestal system, the control panel is located at the top left in a tray. There is space for an optional device beside it.

Figure 1-6 Pedestal System Rear



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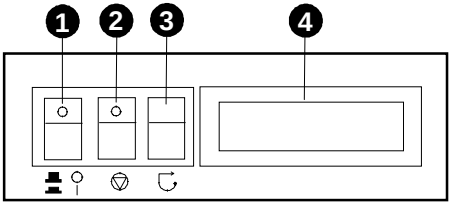
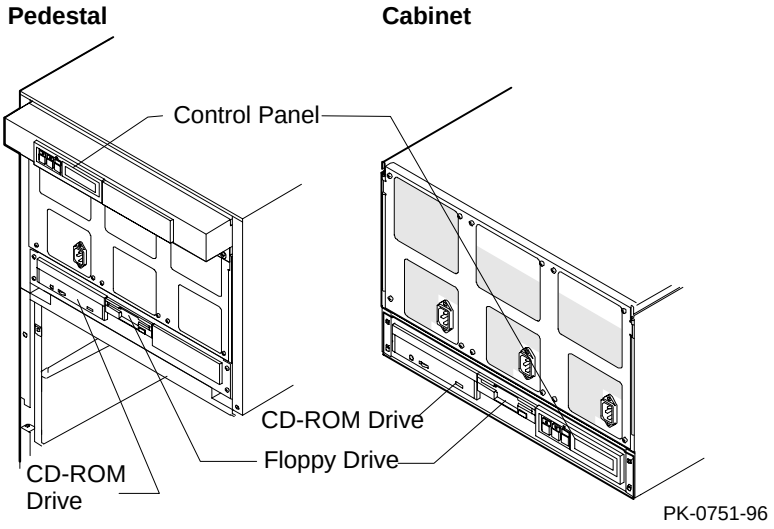
Control Panel and Drives

The control panel includes the On/Off, Halt, and Reset buttons and a display. In a pedestal system the control panel is located in a tray at the top of the system drawer. In a cabinet system, the control panel is at the bottom of the system drawer with the CD-ROM drive and the floppy drive.

Figure 1-7 Control Panel Assembly





❶ On/Off button. Powers the system drawer on or off. When the LED at the top of the button is lit, the power is on. The On/Off button is connected to the power supplies and the system interlocks.

NOTE: The LEDs on some modules are on when the line cord is

missing, regardless of the position of the On/Off button.

❷ Halt button. Pressing this button in (so the LED at the top of the button is on) has no effect on Windows NT.

If the Halt button is in when the system is reset or powered up, the system halts in the SRM console. AlphaBIOS is not loaded and started.

❸ Reset button. Initializes the system drawer. If the Halt button is pressed (LED on) when the system is reset, the SRM console is loaded and remains in the system regardless of any other conditions.

❹ Control panel display. Indicates status during power-up and self-test. The OCP display is a 16-character LCD. Its controller is on the XBUS on the PCI motherboard.

While the operating system is running, displays the system type as a default. This message can be changed by the user.

CD-ROM drive. The CD-ROM drive is used to load software, firmware, and updates. Its controller is on PCI1 on the PCI motherboard.

Floppy disk drive. The floppy drive is used to load software and firmware updates. The floppy controller is on the XBUS on the PCI motherboard.

System Consoles

There are two console programs: the SRM console and the AlphaBIOS console.

SRM Console

The SRM console is a command-line interface that tests the system after power-up or reset and launches the AlphaBIOS graphical interface. For some configuration and diagnostic or testing tasks, you may need to use the SRM console interface rather than launch the AlphaBIOS console. To reach the SRM console interface, power up or reset the system with the Halt button pressed in. You then see the SRM console prompt:

```
P00>>>
```

NOTE: The console prompt displays only after the entire power-up sequence is complete. This can take up to several minutes if the memory is very large.

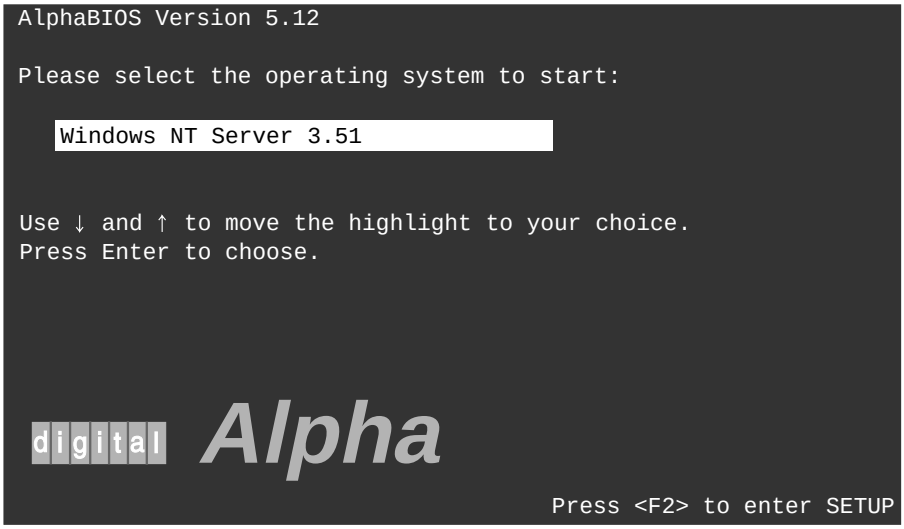
After the SRM console prompt appears, you should change the Halt button back to the "out" position

AlphaBIOS Console

The AlphaBIOS console is a menu-based interface that supports the Microsoft Windows NT operating system. You use AlphaBIOS to set up operating system selections, boot Windows NT, and display information about the system configuration. You also run the EISA Configuration Utility and the RAID Standalone Configuration Utility from the AlphaBIOS console. With the DIGITAL Server 7300/7300R series, AlphaBIOS runs on either a serial (character-cell) terminal or a graphics monitor.

When you invoke the AlphaBIOS console, you see the following Boot menu:

Figure 1-8 AlphaBIOS Boot Menu



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Environment Variables

Environment variables are software parameters that, among other things, define the system configuration. You can use them to pass information to different pieces of software running in the system at various times.

The **os_type** environment variable determines which of the two consoles is to be used. The SRM console is always brought into memory, but AlphaBIOS is loaded if **os_type** is set to **NT** (which it must be on the DIGITAL Server 7300/7300R series) and the Halt button is out (not lit).

See the section "Summary of SRM Environment Variables" in Chapter 8 of this manual for a list of the environment variables used to configure DIGITAL Server 7300/7300R series systems.

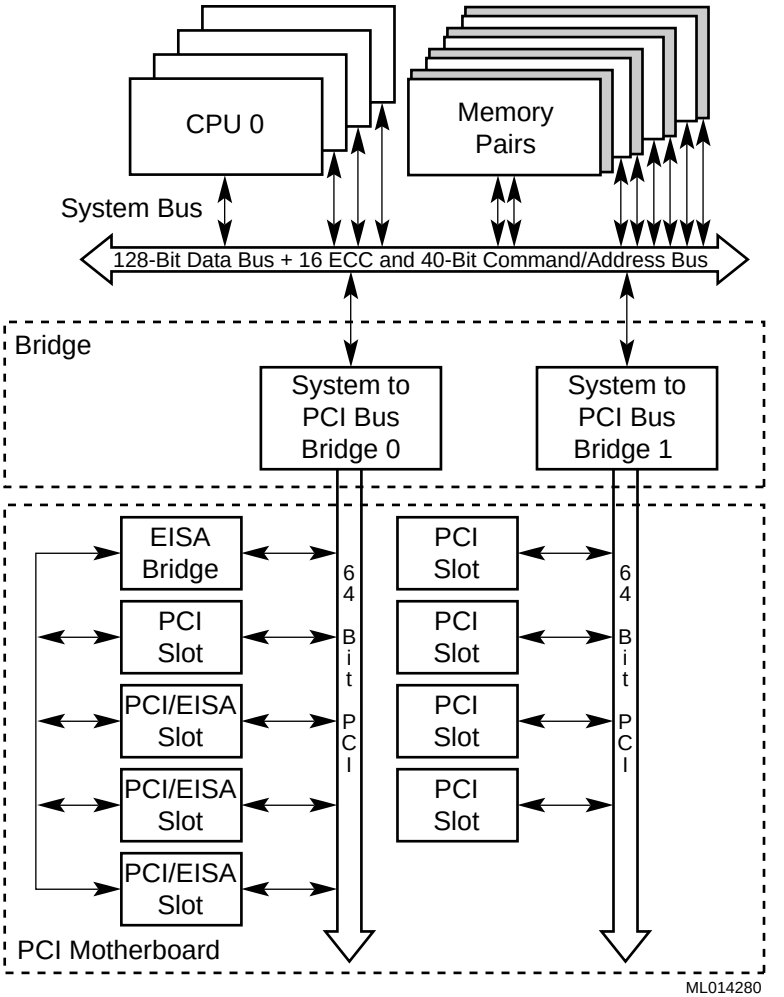
Refer to the *DIGITAL Server 7300/7300R Series System Drawer User's Guide* for information on setting environment variables.

You should keep a record of the environment variables for each system that you service. Some environment variable settings are lost when a module is swapped and must be restored after the new module is installed. Refer to Table 8-3 for a convenient worksheet for recording environment variable settings.

System Architecture

Alpha microprocessor chips are used in these systems. The CPU, memory and the I/O bridge module are connected to the system bus motherboard.

Figure 1-9 Architecture Diagram



DIGITAL Server 7300/7300R series systems use the Alpha chip for the CPU. The CPU, memory, and I/O bridge module to PCI/EISA I/O buses are connected to the system bus motherboard. A fourth type of module, the power control module, also plugs into the system motherboard.

A fully configured DIGITAL Server 7300/7300R series system drawer can have up to four CPUs, four memory pairs, and a total of eight I/O options. The I/O options can be all PCI options or a combination of PCI options and EISA options. However, there can be no more than three EISA options.

The system bus has a 144-bit data bus protected by 16 bits of ECC and a 40-bit command/address bus protected by parity. The bus speed depends on the speed of the CPU in slot 0 which provides the clock for the buses. The 40-bit address bus can create one terabyte of addresses (that's a million billion). The bus connects CPUs, memory, and the system bus to PCI bus bridge(s).

The CPU modules are available with an onboard cache. The Alpha chip has an 8-Kbyte instruction cache (I-cache), an 8-Kbyte write-through data cache (D-cache), and a 96-Kbyte, write-back secondary data cache (S-cache). The cache system is write-back. The system drawer supports up to four CPUs.

The memory modules are placed on the system motherboard in pairs. Each module drives half of the system bus, along with the associated ECC bits. Memory pairs consist of two modules that are the same size and type. Two types are available: synchronous and asynchronous (EDO) memory.

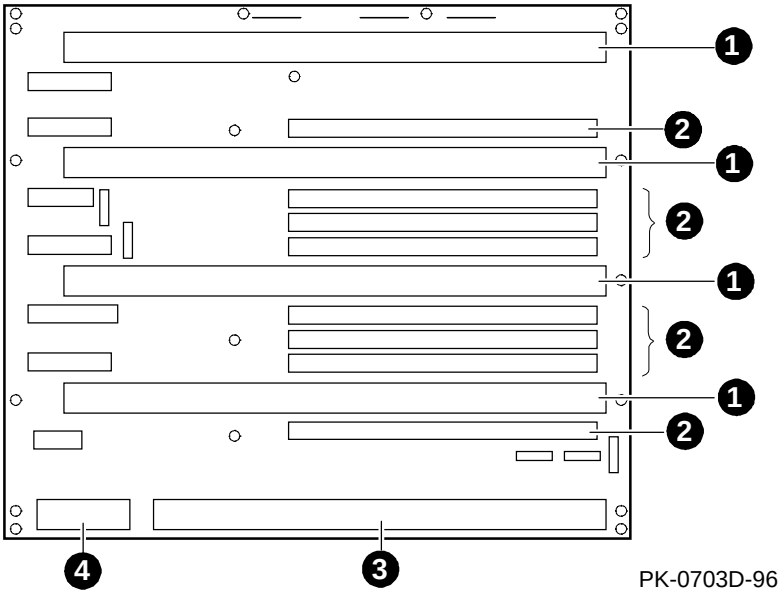
The system bus to PCI bus bridge module translates system bus commands and data addressed to I/O space to PCI commands and data. It also translates PCI bus commands and data addressed to system memory or CPUs to system bus commands and data. The PCI bus is a 64-bit wide bus used for I/O. The 7300/7300R series has one PCI/EISA card cage.

The power control module, which is on the system motherboard, monitors power and the system environment.

System Motherboard

The system motherboard is on the floor of the system card cage. It has slots for the CPU, memory, power control, and bridge modules.

Figure 1-10 System Motherboard Module Locations



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The system motherboard has the logic for the system bus. It is the backplane that holds the CPU, memory, bridge, and power control modules. Figure 1-10 shows a diagram of the motherboard used in DIGITAL Server 7300/7300R series systems. The module locations are designated by the call outs.

❶ CPU module

❷ Memory module

❸ Bridge module

❹ Power control module

CPU Types

DIGITAL Server 7300/7300R series systems can be configured with one of two CPU variants.

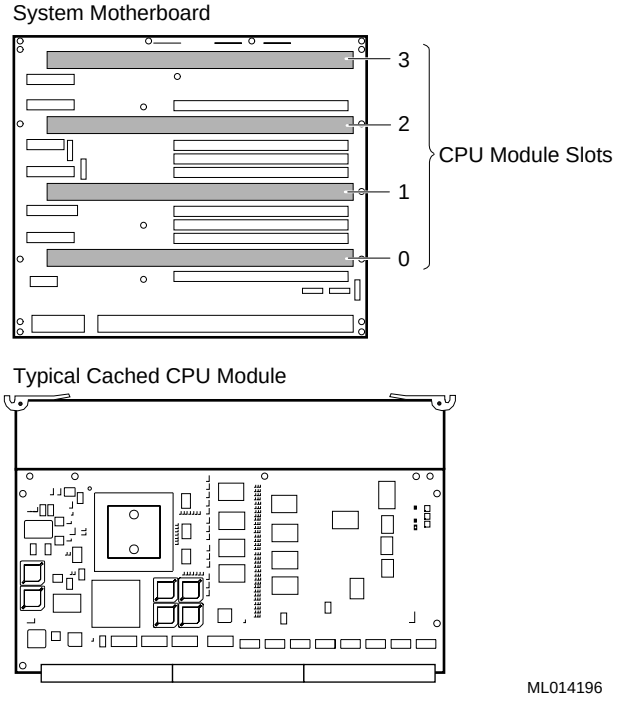
CPU Variants

Module Variant	Clock Frequency	Onboard Cache
B3105-AA	400 MHz	4 Mbytes
B3105-CA	533 MHz	4 Mbytes

CPU Module Layout

Figure 1-11 shows the layout of the CPU module.

Figure 1-11 CPU Module Layout



Alpha Chip Composition

The Alpha chip is made using state-of-the-art chip technology, has a transistor count of 9.3 million, consumes 50 watts of power, and is air cooled (a fan is on the chip). The default cache system is write-back and when the module has an external cache, it is write-back.

Chip Description

Unit	Description
Instruction	8-byte cache, 4-way issue
Execution	4-way execution; 2 integer units, 1 floating-point adder, 1 floating-point multiplier
Memory	Merge logic, 8-Kbyte write-through first-level data cache, 96-Kbyte write-back second-level data cache, bus interface unit

CPU Configuration Rules

- The first CPU must be in CPU slot 0 to provide the system clock.
- Additional CPU modules should be installed in ascending order by slot number.
- All CPUs must have the same Alpha chip clock speed. The system bus hangs without an error message if the oscillators clocking the CPUs are different.

CPU Module Color Codes

The top edge of the CPU module variant is color coded for easy identification.

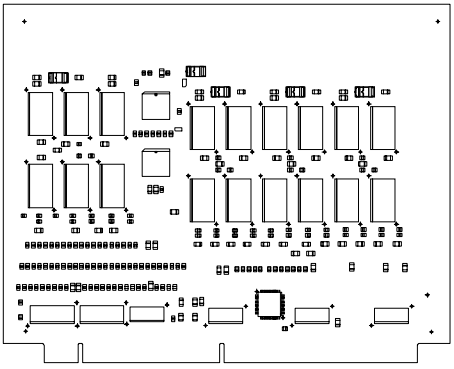
Color	Option Number	Description
Orange	B3105-AA	400 MHz, 4MB cached
Violet	B3105-CA	533 MHz, 4MB cached

Memory Modules

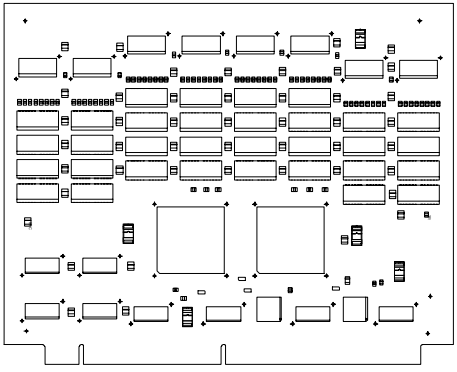
Memory modules are used only in pairs — two modules of the same size and type. Each module provides either the low half or the high half of the memory space. The 7300/7300R series system drawer can hold up to four memory module pairs.

Figure 1-12 Memory Module Layout

Typical Synchronous Memory



Typical EDO Memory



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Memory Variants

Each memory option consists of two identical modules. Each DIGITAL Server 7300/7300R series drawer supports up to four memory options, for a total of 4 Gbytes of memory. Memory modules are used only in pairs and are available in 128 Mbyte, 512 Mbyte, 1 Gbyte, and 2 Gbyte sizes. The 128-Mbyte option is synchronous memory, while the larger sizes are asynchronous memory (EDO).

				DRAM	
Option Part No	**Size**	**Module**	**Type**	**Number**	**Size**
FR-ACSMA-AA	128 MB	B3020-CA	Synch.	36	4 MB x 4
FR-ACSMA-AB	512 MB	B3030-EA	Asynch. (EDO)	144	4 MB x 4
FR-ACSMA-AC	1 GB	B3030-FA	Asynch. (EDO)	72	16 MB x 4
FR-ACSMA-AD	2 GB	B3030-GA	Asynch. (EDO)	144	16 MB x 4

Memory Operation

Memory modules are used only in pairs; each module provides half the data, or 64 bits plus 8 ECC bits, of the octaword (16 byte) transferred on the system bus. Modules are placed in slots designated MEMxL and MEMxH.

NOTE: Modules in slots MEMxL do not drive the lower 8 bytes, and modules in slots MEMxH do not drive the higher 8 bytes of the 16 byte transfer.

Unless otherwise programmed, memory drives the system bus in bursts. Upon each memory fetch, data is transferred in 4 consecutive cycles transferring 64 bytes. There are situations, however, when memories made with EDO DRAMs cannot provide data fast enough to complete the system bus transactions. When these situations arise, EDO type memories assert a signal that causes the system bus to stall for one (occasionally more) clock tick. When memory completes such an operation, it releases the system bus.

Memory Configuration Rules

In a system, memories of different sizes and types are permitted, but:

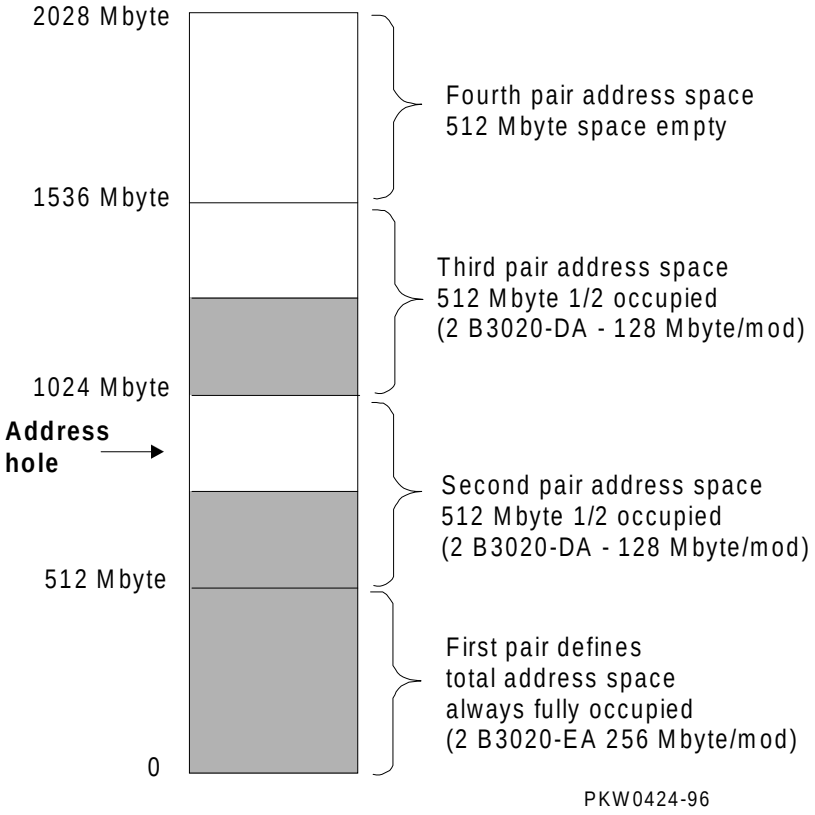
- Memory modules are installed and used in pairs. Both modules in a memory pair must be of the same size and type.

- The largest memory pair must be in slots MEM 0L and MEM 0H.
- Other memory pairs must be the same size or smaller than the first memory pair.
- Memory pairs must be installed in consecutive slots.

Memory Addressing

Alpha system memory addressing is unusual because memory address space is determined not by the amount of physical memory but is calculated by a multiple of the size of the memory pair in slot MEM0x.

Figure 1-13 How Memory Addressing Is Calculated



The rules for addressing memory are as follows:

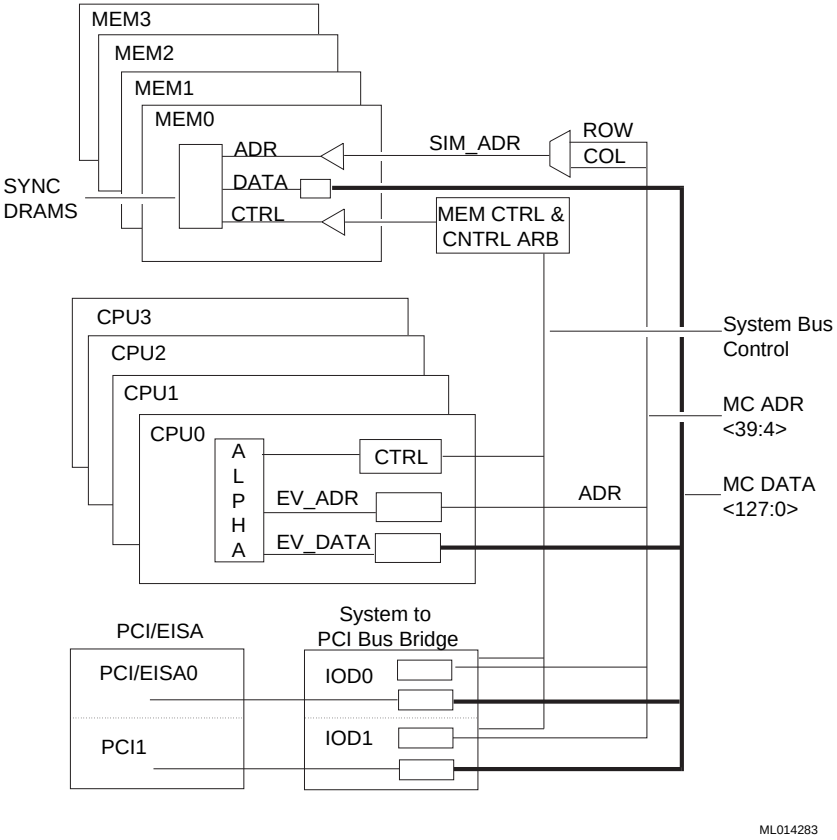
- Address space is determined by the memory pair in slot MEM0.
- Memory pairs need not be the same size.
- The memory pair in slot MEM0 must be the largest of all memory pairs. Other memory pairs may be as large but none may be larger.
- The starting address of each memory pair is N times the size of the memory pair in slot MEM0. N=0,1,2,3.
- Memory addresses are contiguous within each module pair.
- If memory pairs are of different sizes, memory “holes” can occur in the physical address space. See Figure 1-13.

Software creates contiguous virtual memory even though physical memory may not be contiguous.

System Bus

The system bus consists of a 40-bit command/address bus, a 128-bit plus ECC data bus, and several control signals and clocks.

Figure 1-14 System Bus Block Diagram



The system bus motherboard consists of a 40-bit command/address bus, a 128-bit plus ECC data bus, and several control signals, clocks, and a bus arbiter. The bus requires that all CPUs have the same high-speed oscillator providing the clock to the Alpha chip.

The DIGITAL Server 7300/7300R series system bus connects up to four CPUs, four pairs of memory modules, and a single I/O bus bridge module. The I/O bus bridges may be designated as IOD*n* where *n* is the number of the PCI bus. The bridge is designated IOD0 and IOD1.

The system bus clock is provided by an oscillator on the CPU in slot CPU0. This oscillator has a 1:5 ratio to the Alpha chip. With 400 MHz CPUs, for example, the system bus operates at 80 MHz.

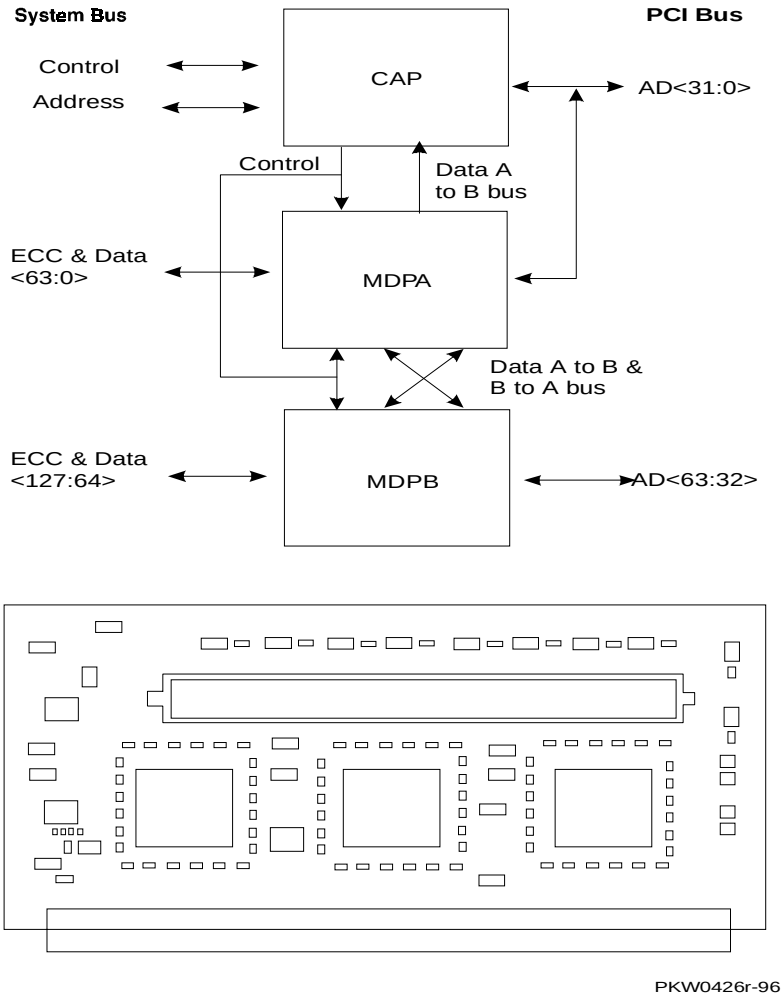
The system bus motherboard initiates memory refresh transactions. The motherboard sits at the bottom of the system drawer, and in addition to CPUs, memory, and I/O bridges, holds a power control module.

5 volt and 3.43 volt power is provided directly to the motherboard from the power supplies.

System Bus to PCI Bus Bridge Module

The bridge module is the physical interconnect between the system motherboard and any PCI motherboard in the system.

Figure 1-15 Bridge Module



The system bus to PCI bus bridge module converts:

- System bus commands and data addressed to I/O space to PCI commands and data
- PCI bus commands and data addressed to system memory or CPUs to system bus commands and data.

A DIGITAL Server 7300/7300R series system has one bridge module. The bridge module has two major components:

- Command/address processor (CAP) chip
- Two data path chips (MDPA and MDPB)

There are two sets of these three chips, one set on each side of the module. Each set bridges to one of the PCI buses on the PCI motherboard.

The interface on the system bus side of the bridge responds to system bus commands addressed to the upper 64 Gbytes of I/O space. I/O space is addressed whenever bit <39> on the system bus address lines is set. The space so defined is 512 Gbytes in size. The first 448 Gbytes are reserved and the last 64 Gbytes, when bits <38:36> are set, are mapped to the PCI I/O buses.

The interface on the PCI side of the bridge responds to commands addressed to CPUs and memory on the system bus. On the PCI side, the bridge provides the interface to the PCIs. Each PCI bus is addressed separately. The bridge does not respond to devices communicating with each other on the same PCI bus. However, should a device on one PCI address a device on the other PCI bus, commands, addresses, and data run through the bridge out onto the system bus and back through the bridge to the other PCI bus.

In addition to its bridge function, the system bus to PCI bus bridge module monitors every transaction on the system bus for errors. It monitors the data lines for ECC errors and the command/address lines for parity errors.

PCI I/O Subsystem

The I/O subsystem is PCI. The DIGITAL Server 7300/7300R series has two four-slot PCI buses that hold up to eight I/O options. One of these buses can be both PCI and EISA, but can hold not more than four options three of which may be EISA.

Figure 1-16 PCI Block Diagram

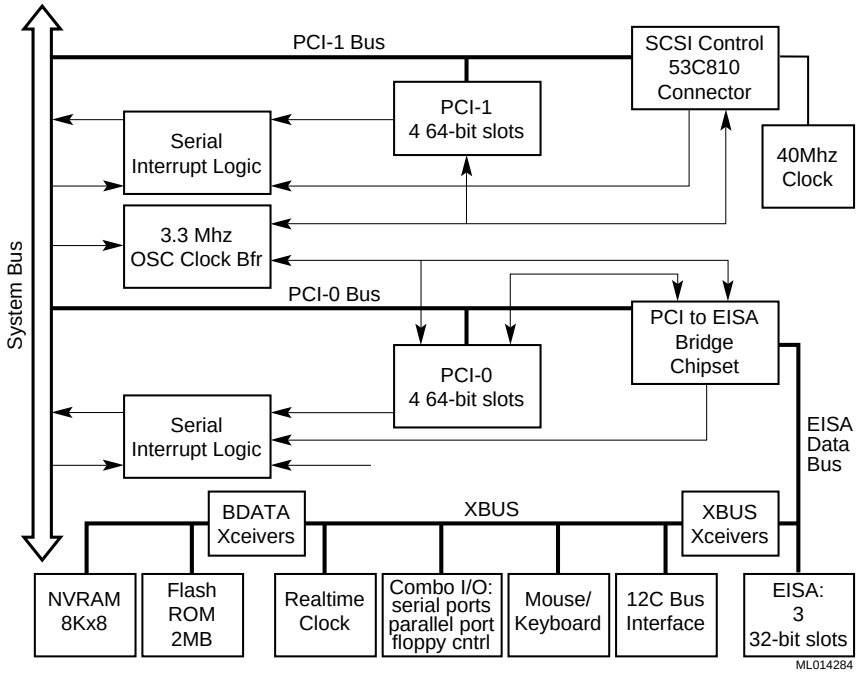


Table 1-1 PCI Motherboard Slot Numbering

Slot	PCI0	PCI1
0	Reserved	Reserved
1	PCI to EISA bridge	Internal CD-ROM controller
2	PCI or EISA slot	PCI slot
3	PCI or EISA slot	PCI slot
4	PCI or EISA slot	PCI slot
5	PCI slot	PCI slot

The logic for two PCI buses is on each PCI motherboard.

PCI0 is a 64-bit bus with a built-in PCI to EISA bus bridge. PCI0 has one dedicated PCI slot and three slots, though there are six connectors, that can be PCI or EISA slots. Each slot has an EISA connector and a PCI connector only one of which may be used at a time. PCI0 is powered by 5V.

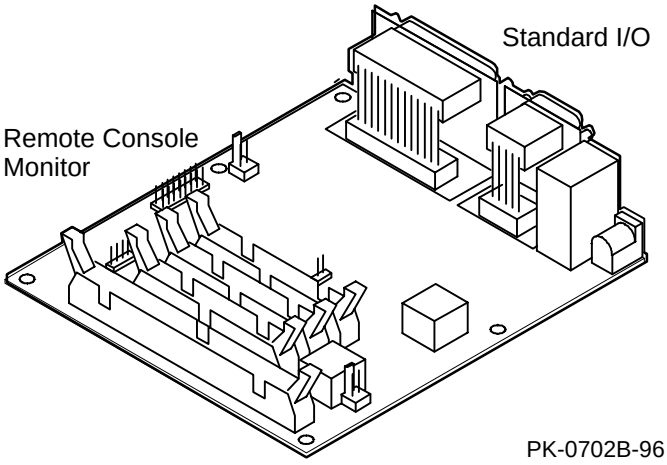
PCI1 is a 64-bit bus with a built-in CD-ROM controller and four PCI slots. PCI1 is powered by 5V.

An 8-bit XBUS is connected to the EISA bus. On this bus there is an interface to the system I^2C bus; mouse and keyboard support; an I/O combo controller supporting two serial ports, the floppy controller, and a parallel port; a real-time clock; two 1-Mbyte flash ROMs containing system firmware, and an 8-Kbyte NVRAM.

Server Control Module

The server control module enables remote console connections to the system drawer. The module passes signals to COM ports 1 and 2, the keyboard, and the mouse to the standard I/O connectors.

Figure 1-17 Server Control Module



The server control module has two sections: the remote console monitor (RCM) and the standard I/O. See Chapter 9 for information on controlling the system remotely.

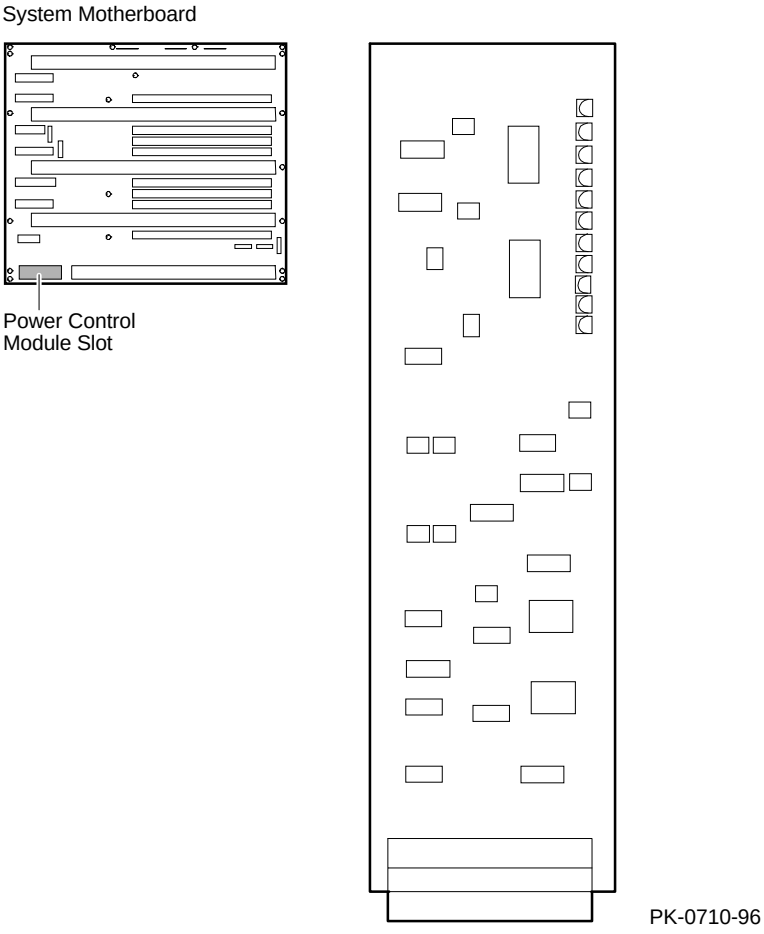
The remote console monitor connects to a modem through the modem port on the bulkhead. The RCM requires a 12V power connection.

The standard I/O ports (keyboard, mouse, COM1 and COM2 serial, and parallel ports) are on the same bulkhead.

Power Control Module

The power control module controls power sequencing and monitors power supply voltage, temperature, and fans.

Figure 1-18 Power Control Module



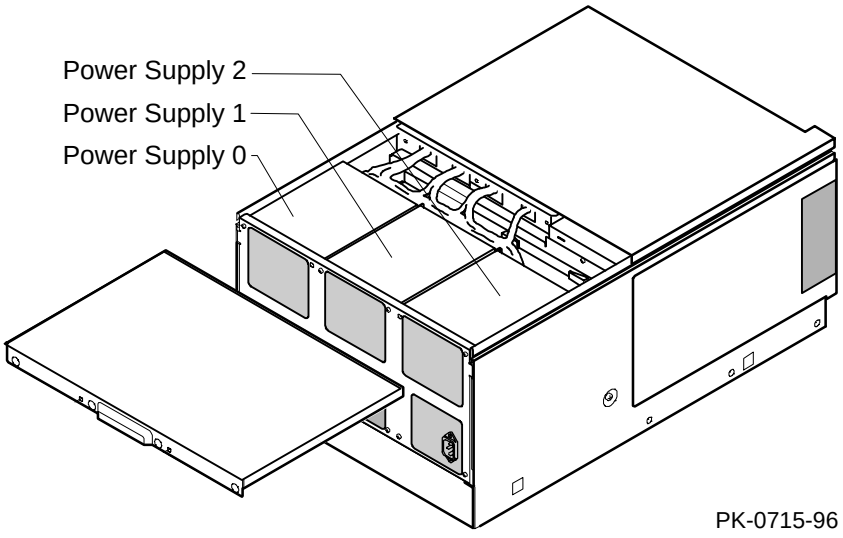
The power control module performs the following functions:

- Controls power sequencing.
- Monitors the combined output of power supplies and shuts down power if it is not in range.
- Monitors system temperature and shuts off power if it is out of range.
- Monitors the fans in the system drawer and on the CPU modules and shuts down power if a fan fails.
- Provides visual indication of faults through LEDs.

Power Supply

The system drawer power supplies provide power only to components in the drawer. One or two power supplies are required, depending on the number of CPU modules and PCI card cages; a second or third can be added for redundancy. The power system is described in detail in Chapter 4.

Figure 1-19 Location of Power Supply



Description

One to three power supplies provide power to components in the system drawer. (They supply power only for the drawer in which they are located.) Three power supplies provide redundant power in fully loaded DIGITAL Server 7300/7300R series systems.

These power supplies share the load, and redundant configurations are supported. They autoselect line voltage (120V to 240V). Each has 450 W output and supplies up to 75A of 3.43V, 50A of 5.0V, 11A of 12V, and small amounts of –5V, –12V, and auxiliary voltage (Vaux).

NOTE: The LEDs on some modules are on when the line cord is plugged in, regardless of the position of the On/Off button.

Configuration

A DIGITAL Server 7300/7300R series system with one or two CPUs requires one power supply (two for redundancy).

A DIGITAL Server 7300/7300R series system with three or four CPUs requires two power supplies (three for redundancy).

Power supply 0 is installed first, power supply 2 second, and power supply 1 third. See Figure 1-19 Location of Power Supply. (The power supply numbering shown here corresponds to the numbering displayed by the SRM console's **show power** command.)

2
Power-Up

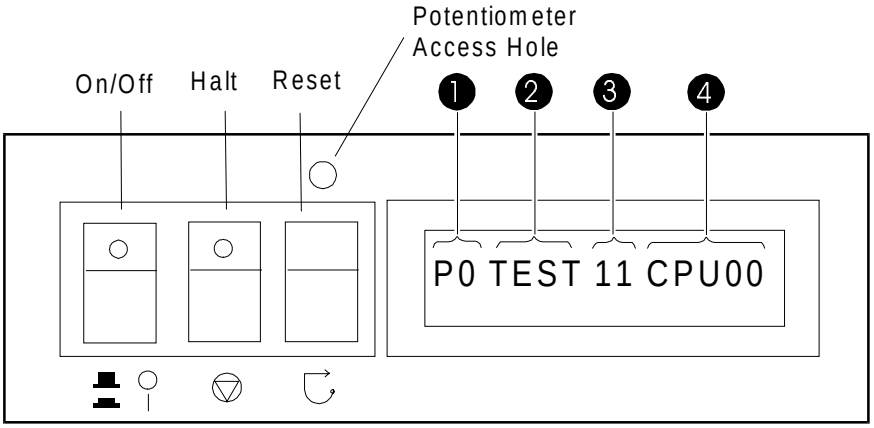
This chapter describes system power-up testing and explains the power-up displays. The following topics are covered:

- Control Panel
- Power-Up Sequence
- SROM Power-Up Test Flow
- SROM Errors Reported
- XSROM Power-UP Test Flow
- XSROM Errors Reported
- Console Power-Up Tests
- Console Device Determination
- Console Power-Up Display
- Fail-Safe Loader

Control Panel

The control panel display indicates the likely device when testing fails.

Figure 2-1 Control Panel and LCD Display



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When the On/Off button LED is on, power is applied and the system is running. When it is off, the system is not running, but power may or may not be present. If power is present, the PCM or the power LED on the system bus to PCI bus bridge module should be flashing. Otherwise, there is a power problem.

When the Halt button LED is lit and the On/Off button is on, the system should be running either the SRM console or Windows NT. If the Halt button is in, but the LED is off, the OCP, its cables, or the PCM are likely to be broken.

Table 2-1 Control Panel Display

Field	Content	Display	Meaning
❶	CPU number	P0–P3	CPU reporting status
❷	Status	TEST	Tests are executing
		FAIL	Failure has been detected
		MCHK	Machine check has occurred
		INTR	Error interrupt has occurred
❸	Test number		
❹	Suspected device	CPU0–3	CPU module number[1]
		MEM0–3 and L, H, or *	Memory pair number and low module, high module, or either[2]
		IOD0	Bridge to PCI bus 0[3]
		IOD1	Bridge to PCI bus 1[3]
		FROM0	Flash ROM[4]
		COMBO	COM controller[4]
		PCEB	PCI-to-EISA bridge[4]
		ESC	EISA system controller[4]
		NVRAM	Nonvolatile RAM[4]
		TOY	Real-time clock[4]
		I8242	Keyboard and mouse controller[4]

The potentiometer, accessible through the access hole just above the Reset button controls the intensity of the LCD. Use a small Phillips head screwdriver to adjust.

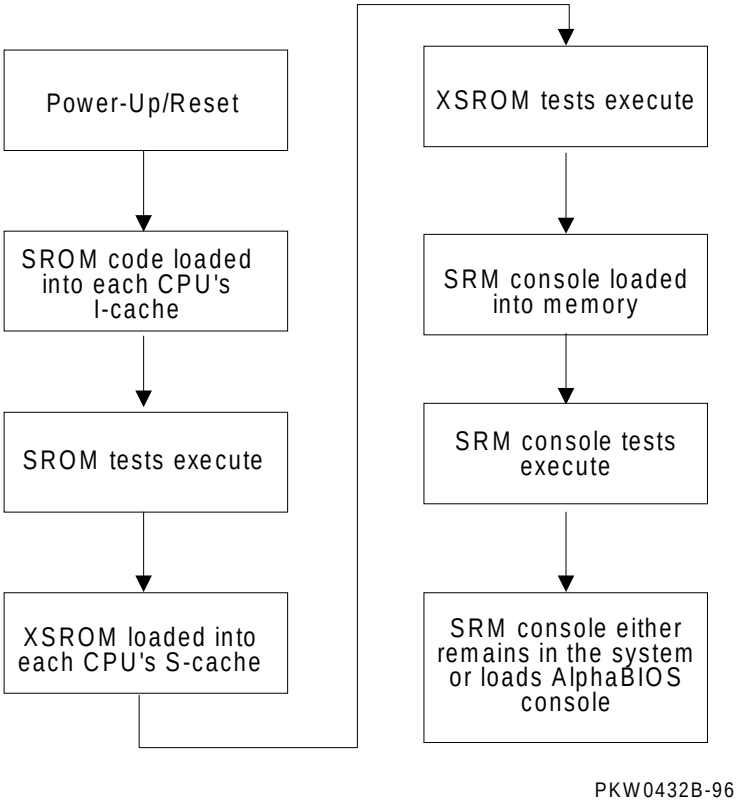
---

[1] CPU module
[2] Memory module
[3] Bridge module (B3040-AA)
[4] EISA/PCI motherboard

Power-Up Sequence

Console and most power-up tests reside on the I/O subsystem, not on the CPU nor on any other module on the system bus.

Figure 2-2 Power-Up Flow



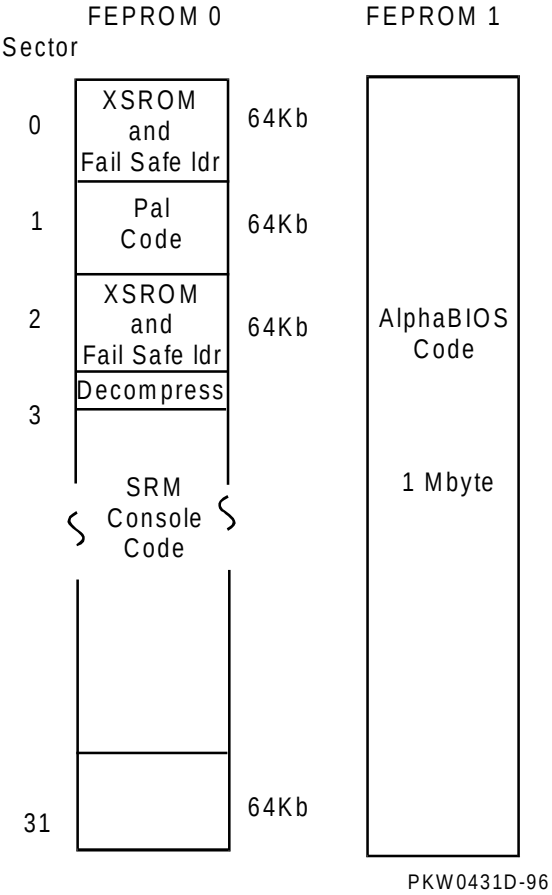
Definitions

SROM. The SROM is a 128-Kbit ROM on each CPU module. SROM contains minimal diagnostics that test the Alpha chip and the path to the XSROM. Once the path is verified, it loads XSROM code into the Alpha chip and jumps to it.

XSROM. The XSROM, or extended SROM, contains back-up cache and memory tests, and a fail-safe loader. The XSROM code resides in sector 0 of FEPROM 0 on the XBUS. Sector 2 of FEPROM 0 contains a duplicate copy of the code and is used if sector 0 is bad.

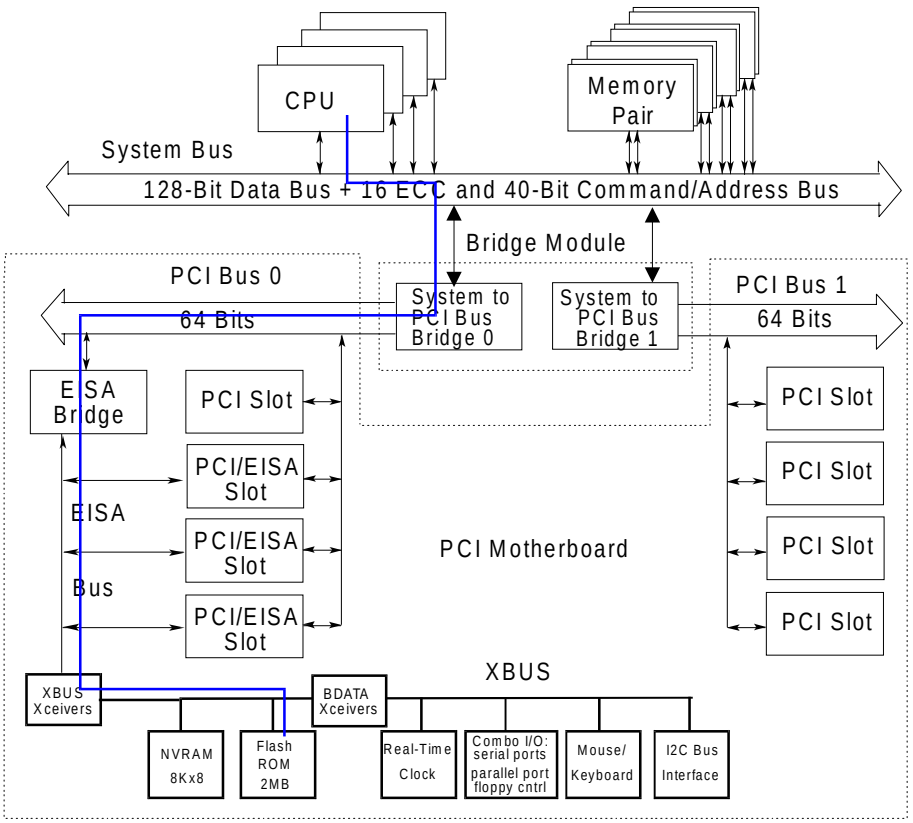
FEPROM. Two 1-Mbyte programmable ROMs are on the XBUS on PCI0. FEPROM 0 contains two copies of the XSROM, and the SRM console and decompression code. FEPROM 1 contains the AlphaBIOS and NT HALcode. These two FEPROMs can be flash updated. Refer to Chapter 7.

Figure 2-3 Contents of FEPROMs



For the console to run, the path from the CPU to the XSROM must be functional. The XSROM resides in FEPROM0 on the XBUS, off the EISA bus, off PCI 0, off IOD 0. See Figure 2-4. This path is minimally tested by SROM.

Figure 2-4 Console Code Critical Path



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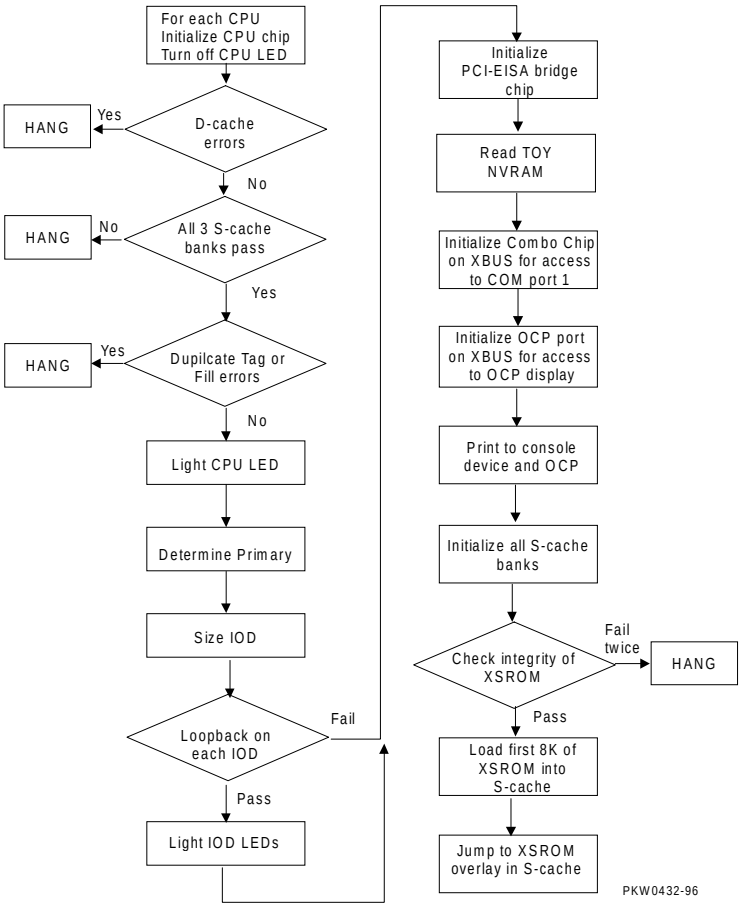
The SROM contents are loaded into each CPU's I-cache and executed on power-up/reset. After testing the caches on each processor chip, it tests the path to the XSROM. Once this path is tested and deemed reliable, layers of the XSROM are loaded sequentially into the processor chip on each CPU. None of the SROM or XSROM power-up tests are run from memory—all run from the caches in the CPU chip, thus providing excellent diagnostic isolation. Later power-up tests, run under the console, are used to complete testing of the I/O subsystem.

There are two console programs: the SRM console and the AlphaBIOS console, as detailed in the *DIGITAL Server 7300/7300R Series System Drawer User's Guide* (ER–K9FWW–UA). By default, the SRM console is always loaded and I/O system tests are run under it before the system loads AlphaBIOS. To load AlphaBIOS, the **os_type** environment variable must be set to **NT** and the Halt button should be out (LED not lit).

SROM Power-Up Test Flow

The SROM tests the CPU chip and the path to the XSROM.

Figure 2-5 SROM Power-Up Test Flow



The Alpha chip built-in self-test tests the I-cache at power-up and upon reset.

Each CPU chip loads its SROM code into its I-cache and starts executing it. If the chip is partially functional, the SROM code continues to execute. However, if the chip cannot perform most of its functions, that CPU hangs and that CPU pass/fail LED remains off.

If the system has more than one CPU and at least one passes both the SROM and XSROM power-up tests, the system will bring up the console. The console checks the FW_SCRATCH register where evidence of the power-up failure is left. Upon finding the error, the console sends these messages to COM1 and the OCP:

- COM1 (or VGA): Power-up tests have detected a problem with your system
- OCP: Power-up failure

Table 2-2 lists the tests performed by the SROM.

Table 2-2 SROM Tests

Test Name	Logic Tested
D-cache RAM March test	D-cache access, D-cache data, D-cache address logic
D-cache Tag RAM March test	D-cache tag store RAM, D-cache bank address logic
S-cache Data March test	S-cache RAM cells, S-cache data path, S-cache address path
S-cache Tag RAM March test	S-cache tag store RAM, S-cache bank address logic
I-cache Parity Error test	I-cache parity error detection, ISCR register and error forcing logic, IC_PERR_STAT register and reporting logic
D-cache Parity Error test	D-cache parity error detection, DC_MODE register and parity error forcing logic, DC_PERR_STAT register and reporting logic
S-cache Parity Error test	S-cache parity error detection, AC_CTL register and parity error forcing logic, SC_STAT register and reporting logic
IOD Access test	Access to IOD CSRs, data path through CAP chip and MDP0 on each IOD, PCI0 A/D lines <31:0>

SROM Errors Reported

The SROM reports machine checks, pending interrupt/exception errors, and errors related to corruption of FEPROM 0. If SROM errors are fatal, the particular CPU will hang and only the CPU self-test pass LEDs and/or the LEDs on the system bus to PCI bus bridge module will indicate the failure.

Example 2-1 SROM Errors Reported at Power-Up

Unexpected Machine Check (CPU Error)

```
UNEX MCHK on CPU 0
EXC_ADR 42a9
EI_STAT fffffff004ffffff
EI_ADDR ffffff000000801f
SC_STAT 0
SC_ADDR FFFFFF0000005F2F
```

Pending Interrupt/Exception (CPU Error)

```
INT-EXC on CPU0
ISR         400000
EI_STAT fffffff007ffffff
EI_ADDR ffffff7fffffffdf
FIL_SYN 631B
BCTGADR ffffffa7fffcafff
```

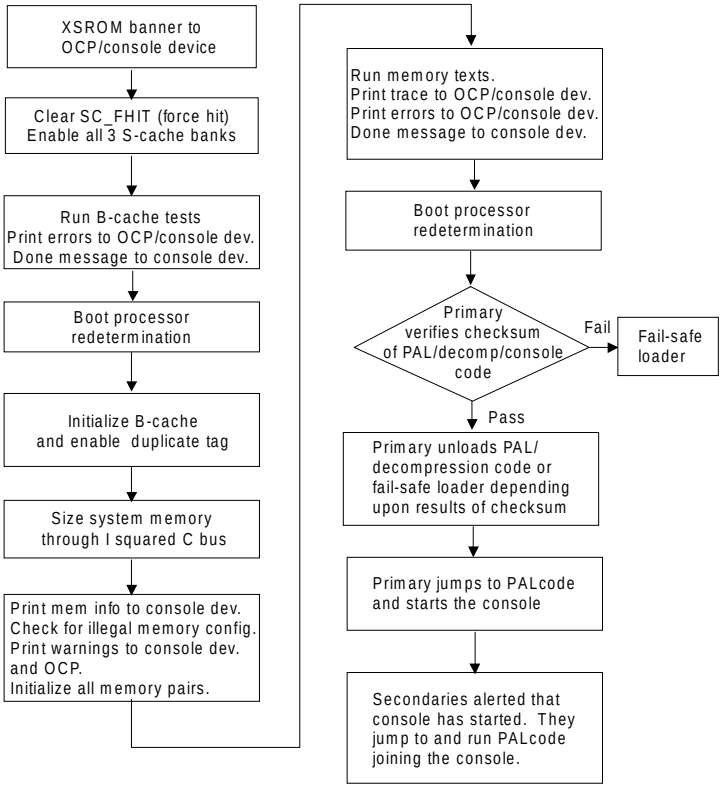
FEPROM Failures (PCI Motherboard Error)

```
Sctr 0 -XSROM headr PTTRN fail
Sctr 0 -XSROM headr CHKSM fail
Sctr 0 -XSROM code CHKSM fail
Sctr 2 -XSROM headr PTTRN fail
Sctr 2 -XSROM headr CHKSM fail
Sctr 2 -XSROM code CHKSM fail
```

XSROM Power-Up Test Flow

After the SROM has completed its tests and verified the path to the FEPROM containing the XSROM code, it loads the first 8 Kbytes of XSROM into the primary CPU's S-cache and jumps to it.

Figure 2-6 XSROM Power-Up Flowchart



Note: The XSROM can only print to the console device if the environment variable console = serial. It always sends output to the OCP.

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XSROM tests are described in following table. Failure indicates a CPU failure.

After jumping to the primary CPU's S-cache, the code then intentionally I-caches itself and is completely register based (no D-stream for stack or data storage is used). The only D-stream accesses are writes/reads during testing.

Each FEPROM has sixteen 64-Kbyte sectors. The first sector contains B-cache tests, memory tests, and a fail-safe loader. The second sector contains PALcode. The third sector contains a copy of the first sector. The remaining thirteen sectors contain the SRM console and decompression code.

NOTE: Memory tests are run during power-up and reset (see Table 2-3). They are also affected by the state of the memory_test environment variable, which can have the following values:

FULL	*Test all memory*
PARTIAL	*Test up to the first 256 Mbytes*
NONE	*Test 32 Mbytes*

Table 2-2 XSROM Tests

Test	Test Name	Logic Tested
11	B-cache Tag Data Line test	Access to B-cache tags, shorts between tag data and its status and parity bits
12	B-cache Tag March test	B-cache tag store RAMs, B-cache STAT store RAMs
13	B-cache Data Line test	B-cache data lines to B-cache data RAMs, B-cache read/write logic
14	B-cache Data March test	B-cache data RAMs, CPU chip B-cache control, CPU chip B-cache address decode, INDEX_H<2x:6> (address bus)
15	B-cache ECC Data Line test	CPU chip ECC generation and checking logic, ECC lines from CPU chip to B-cache, B-cache ECC RAMs
16	B-cache Data ECC March test	Portion of B-cache data RAMs used for ECC
17	CPU chip ECC Single/Double bit Error test	CPU chip ECC single-bit error detection and correction, ECC double-bit error detection, ECC error reporting
18	B-cache Tag Store Parity Error test	B-cache tag array, CPU parity detection, EI_ADDR and EI_STAT register operation
19	B-cache STAT Store Parity Error test	B-cache STAT array, CPU chip B-cache STAT parity generation/detection

Table 2-3 Memory Tests

Test	Test Name	Logic Tested	Description
20	Memory Data test	Data path to and from memory Data path on memory and RAMs	01 – FF Errors are reported as an 8-bit binary field. A set bit indicates a module failure. Bit <0> indicates pass/fail of MEM0_L; <1> indicates pass/fail of MEM0_H; <2> indicates pass/fail of MEM1_L; <7> indicates pass/fail of MEM3_H.
21	Memory Address test	Address path to and from memory Address path on memory and RAMs	Same as test 20.
23*	Memory Bitmap Building	No new logic	Maps out bad memory by way of the bitmap. It does not completely fail memory.
24	Memory March test	No new logic	Maps out bad memory.

* There is no test 22.

XSROM Errors Reported

The XSROM reports B-cache test errors and memory test errors. The XSROM also reports a warning if memory is illegally configured.

Example 2-2 XSROM Errors Reported at Power-Up

B-Cache Error (CPU Error)

```
TEST ERR on cpu0        #CPU running the test
FRU         cpu0
err#  2
tst#  11
exp:  5555555555555555  #Expected data
rcv:  aaaaaaaaaaaaaaaa  #Received data
adr:  ffff8             #B-cache location error
                        #occurred
```

Memory Error (Memory Module Indicated)

```
20..21..
TEST ERR on cpu0              #CPU running test
FRU:  MEM1L                   #Low member of memory pair 1

err#  c
tst#  21
22..23..24..Memory testing complete on cpu0
```

Memory Configuration Error (Operator Error)

```
ERR!  mem_pair0 misconfigured
ERR!  mem_pair1 card size mismatch
ERR!  mem_pair1 card type mismatch
ERR!  mem_pair1 EMPTY
```

FEPROM Failures (PCI Motherboard Error)

```
Sctr 1 -PAL headr PTTRN fail
```

```
Sctr 1 -PAL headr CHKSM fail
Sctr 1 -PAL code CHKSM fail
Sctr 3 -CONSLE headr PTTRN fail
Sctr 3 -CONSLE headr CHKSM fail
Sctr 3 -CONSLE code CHKSM fail
```

Console Power-Up Tests

Once the SRM console is loaded, it does further testing of each IOD. Table 2-4 describes the IOD power-up tests, and Table 2-5 describes the PCI motherboard power-up tests.

Table 2-4 IOD Tests

Test Number	Test Name	Description
1	IOD CSR Access test	Read and write all CSRs in each IOD.
2	Loopback test	Dense space writes to the IOD's PCI dense space to check the integrity of ECC lines on the IODs.
3	ECC test	Loopback tests similar to test 2 but with a varying pattern to create an ECC of 0s. Single- and double-bit errors are checked.
4	Parity Error and Fill Error tests	Parity errors are forced on the address and data lines on system bus and PCI buses. A fill error transaction is forced on the system bus.
5	Translation Error test	A loopback test using scatter/gather address translation logic on each IOD.
6	Write Pending test	Runs test 2 with the write-pending bit set and clear in the CAP chip control register.
7	PCI Loopback test	Loops data through each PCI on each IOD, testing the mask field of the system bus.
8	PCI Peer-to-Peer Byte Mask test	Tests that devices on the same PCI and on different PCIs can communicate.

Table 2-5 PCI Motherboard Tests (B3050/B3052)

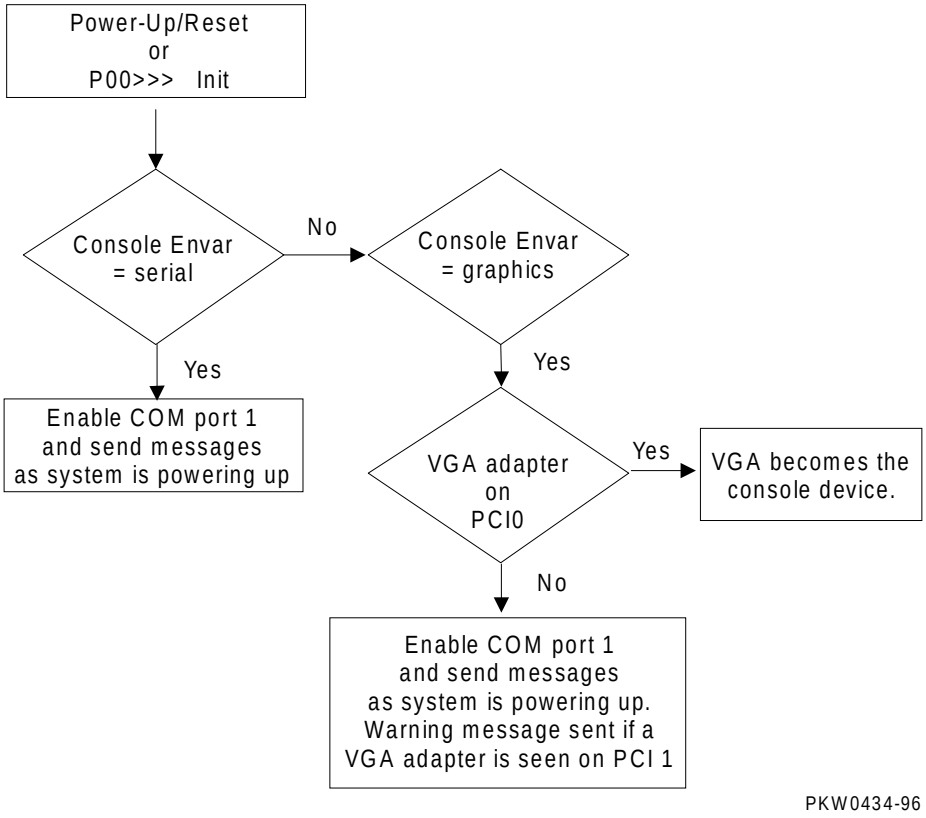
Test Number	Test Name	Diagnostic Name	Description
1	PCEB	pceb_diag	Tests the PCI to EISA bridge chip
2	ESC	esc_diag	Tests the EISA system controller
3	8K NVRAM	nvram_diag	Tests the NVRAM
4	Real-Time Clock	ds1287_diag	Tests the real-time clock chip
5	Keyboard and Mouse	i8242_diag	Tests the keyboard/mouse chip
6	Flash ROM	flash_diag	Dumps contents of flash ROM
7	Serial and Parallel Ports and Floppy	combo_diag	Tests COM ports 1 and 2, the parallel port, and the floppy
8	CD-ROM	ncr810_diag	Tests the CD-ROM controller

For both IOD tests and PCI 0 and PCI 1 tests, trace and failure status is sent to the OCP. If any of these tests fail, a warning is sent to the SRM console device after the console prompt (or AlphaBIOS pop-up box). The LEDs on the system bus to PCI bus bridge module are controlled by the diagnostics. If a LED is off, a failure occurred.

Console Device Determination

After the SROM and XSROM have completed their tasks, the SRM console program, as it starts, determines where to send its power-up messages.

Figure 2-7 Console Device Determination Flowchart



Console Device Options

The console device on a DIGITAL Server 7330/7300R series must be either a serial terminal connected to COM1 off the server control module set at 9600 baud or a graphics monitor off an adapter on PCI0. The console program must be AlphaBIOS.

During power-up, the SROM and the XSROM always send progress and error messages to the OCP. Since the **console** environment variable is set to **graphics**, no messages are sent to COM1.

Console power-up messages are sent to the graphics monitor console device, but SROM and XSROM power-up messages are lost. No matter what the **console** environment variable setting, each of the three programs sends messages to the control panel display.

Messages Sent By	To a Graphics Console Device Are
SROM	Lost
XSROM	Lost
SRM console	Sent to VGA

Console Power-Up Display

The last several lines of the power-up display prints appear on a graphics monitor and parts of it print to the control panel display.

Example 2-3 Power-Up Display

```
 SROM V1.0 on cpu0                                          ❶
 SROM V1.0 on cpu1
 SROM V1.0 on cpu2
 SROM V1.0 on cpu3
XSROM V1.0 on cpu2                                          ❷
XSROM V1.0 on cpu1
XSROM V1.0 on cpu3
XSROM V1.0 on cpu0
BCache testing complete on cpu2                             ❸
BCache testing complete on cpu0
BCache testing complete on cpu3
BCache testing complete on cpu1
mem_pair0 - 128 MB                                          ❹
mem_pair1 - 128 MB
20..20..21..20..21..20..21..21..23..24..24..24..24..        ❺
Memory testing complete on cpu0
Memory testing complete on cpu1
Memory testing complete on cpu3
Memory testing complete on cpu2
```

❶ At power-up or reset, the SROM code on each CPU module is loaded into that module's I-cache and tests the module. If all tests pass, the processor's LED lights. If any test fails, the LED remains off and power-up testing terminates on that CPU.

The first determination of the primary processor is made, and the primary processor executes a loopback test to each PCI bridge. If this test passes, the bridge LED lights. If it fails, the LED remains off and power-up continues. The EISA system controller, PCI-to-EISA bridge, COM1 port, and control panel port are all initialized thereafter.

Each CPU prints an SROM banner to the device attached to the COM1 port and to the control panel display. (The banner prints to the COM1 port if the **console** environment variable is set to **serial**. If it is set to **graphics**, nothing prints to the console terminal, only to the control panel display, until ❻.

❷ Each processor's S-cache is initialized, and the XSROM code in the FEPROM on the PCI 0 is unloaded into them. (If the unload is not successful, a copy is unloaded from a different FEPROM sector. If the second try fails, the CPU hangs.)

Each processor jumps to the XSROM code and sends an XSROM banner to the COM1 port and to the control panel display.

❸ The three S-cache banks on each processor are enabled, and then the B-cache is tested. If a failure occurs, a message is sent to the COM1 port and to the control panel display.

Each CPU sends a B-cache completion message to COM1.

❹ The primary CPU is again determined, and it sizes memory by reading memory registers on the I^2C bus.

The information on memory pairs is sent to COM1. If an illegal memory configuration is detected, a warning message is sent to COM1 and the control panel display.

❺ Memory is initialized and tested, and the test trace is sent to COM1 and the control panel display. Each CPU participates in the memory testing. The numbers for tests 20 and 21 might appear interspersed. This is normal behavior. Test 24 can take several minutes if the memory is very large. The message "P0 TEST 24 MEM**" is displayed on the control panel display; the second asterisk rotates to indicate that testing is continuing. If a failure occurs, a message is sent to the COM1 port and to the control panel display.

Each CPU sends a test completion message to COM1.

Continued

Example 2-3 Power-Up Display (Continued)

```
starting console on CPU 0                                    ❻
sizing memory                                                ❼
  0    128 MB SYNC
  1    128 MB SYNC
starting console on CPU 1
starting console on CPU 2
starting console on CPU 3
probing IOD1 hose 1                                          ❽
  bus 0 slot 1 - NCR 53C810
  bus 0 slot 2 - DECchip 21041-AA
  bus 0 slot 3 - NCR 53C810
  bus 0 slot 4 - DECchip 21040-AA
probing IOD0 hose 0
  bus 0 slot 1 - PCEB
Configuring I/O adapters...
DIGITAL Server 7300 Console V1.0, 13-MAR-1997 18:18:26 ❾
P00>>>
```

❻ The final primary CPU determination is made. The primary CPU unloads PALcode and decompression code from the FEPROM on the PCI 0 to its B-cache. The primary CPU then jumps to the PALcode to start the SRM console.

The primary CPU prints a message indicating that it is running the console. Starting with this message, the power-up display is printed to the default console terminal, regardless of the state of the **console** environment variable. (If **console** is set to **graphics**, the display from here to the end is saved in a memory buffer and printed to the graphics monitor after the PCI buses are sized and the graphics device is initialized.)

❼ The size and type of each memory pair is determined.

The console is started on each of the secondary CPUs. A status message prints for each CPU.

❽ The PCI bridges (indicated as IOD*n*) are probed and the devices are reported. I/O adapters are configured.

❾ The SRM console banner and prompt are printed. (The SRM prompt is shown in this manual as P00>>>. It can, however, be P01>>>, P02>>>, or P03>>>. The number indicates the primary processor.)

When the **os_type** environment variable is set to **nt** (as it must be on the DIGITAL Server 7300/7300R series)**,** the SRM console loads and starts the AlphaBIOS console and does not print the SRM banner or prompt.

Fail-Safe Loader

The fail-safe loader is a software routine that loads the SRM console image from floppy. Once the console is running you will want to run LFU to update FEPROM 0 with a new image.

NOTE: FEPROM 0 contains images of the SROM, XSROM, decompression, and SRM console code.

If the fail-safe loader loads, the following conditions exist on the machine:

- The SROM has passed its tests and successfully unloaded the XSROM. If the SROM fails to unload both copies of XSROM, it reports the failure to the control panel display and COM1 if possible, and the system hangs.
- The XSROM reports the errors encountered and loads the fail-safe loader.

3
Troubleshooting

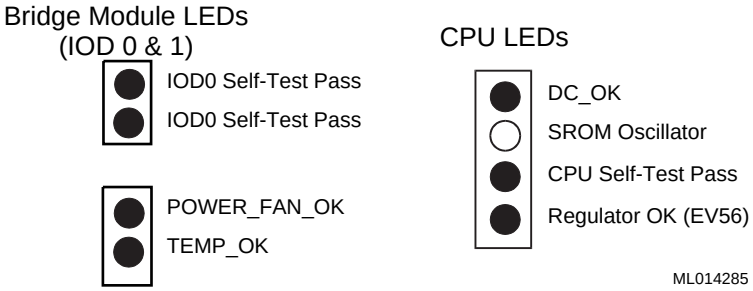
This chapter describes troubleshooting during power-up and booting, as well as diagnostics for DIGITAL Server 7300/7300R series systems. The chapter covers the following topics:

- Troubleshooting with LEDs
- Troubleshooting Power Problems
- Troubleshooting with the Maintenance Bus (I2C Bus)
- Running Diagnostics — Test Command
- Testing an Entire System

Troubleshooting with LEDs

During power-up, reset, initialization, or testing, diagnostics are run on CPUs, memories, bridge modules, PCI motherboards, and sometimes options. The following sections describe possible problems that can be identified by checking LEDs.

Figure 3-1 CPU and Bridge Module LEDs



Processor (CPU) LEDs

If the CPU STP LED on any processor (CPU) module is lit, that CPU chip is functioning properly. If the CPU STP LED is off, that CPU may or may not be functioning.

You can use the Halt button on the OCP to prevent the AlphaBIOS console (which turns off the CPU STP LED) from booting, thus assuring the validity of the CPU STP LED. If the LED is off, replace the CPU. If the LED is lit, you can use the SRM console command **alphabios** to load and run the AlphaBIOS console.

The top LED on a CPU module is a DC OK LED. It is driven by the PCM module. If it is not lit, there are probably power problems.

The second from the top LED on a CPU lights only when the SROM on the CPU is loaded.

On modules with EV56 CPU processors a fourth LED is present at the bottom of the column. The LED is normally on indicating that the power regulator on the module is working properly. If the LED is off, replace the module.

System Bus to PCI Bus Bridge Module LEDs (B3040-AA)

There are four LEDs on the B3040-AA system bus to PCI bus bridge module:

The top two LEDs indicate the condition of the bridge module. If either is off, the module should be replaced.

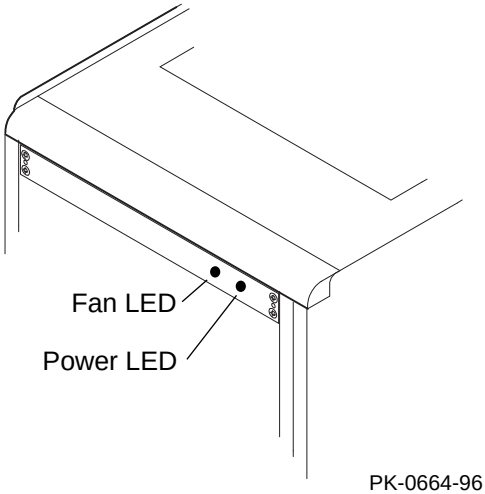
The bottom two LEDs are passed from the PCM. Both should be on during normal operation. If either is off while the system is on, the LEDs on the PCM module should indicate what failed. If they do not, the PCM could be broken or the bridge module is not passing the signals to the LEDs.

NOTE: If AC power is applied and the system is off and a power supply is in operation, the power LED, the top one of the bottom two, flashes, indicating the presence of Vaux (auxiliary voltage).

Cabinet Power and Fan LEDs

Figure 3-2 shows the cabinet power and fan LEDs.

Figure 3-2 Cabinet Power and Fan LEDs



A cabinet system has three exhaust fans at the top of the cabinet. They are powered from a small power supply in the fan tray. This power supply also powers the server control module at the bottom of the PCI card cage to allow remote access to the system. A failure of the power supply is indicated only by the LEDs. No messages are displayed.

There are two LEDs on the top panel: a fan LED and a power LED.

When the fan LED (amber) is flashing, a cabinet fan needs replacing. Look to see which fan appears broken (either not functioning at all; or turningh slower than the others).

When the power LED (green) is off, either the power supply in the fan tray is broken or there is a power problem.

Troubleshooting Power Problems

Power problems can occur before the system is up or while the system is running. If a system stops running, make a habit of checking the PCM.

Power Problem List

The system will halt for the following:

1. A CPU fan failure
2. A system fan failure
3. An overtemperature condition
4. Power supplied out of tolerance
5. Circuit breaker(s) tripped
6. AC problem
7. Interlock switch activation or failure
8. PCM failure
9. Environmental electrical failure or unrecoverable system fault with auto_action ev = halt or boot
10. Operator error - failure to unplug all power supplies and letting Vaux drain (10 sec delay) before restarting
11. Cable failure
12. Module failure - System motherboard, PCI motherboard, or system bus to PCI bus bridge
13. SCM breaking the interlock circuit

Indications of failure:

1. Power control module LEDs indicate CPU fan, system fan, overtemperature, and power supply failures
2. Circuit breaker(s) tripped

No obvious indications for failures 7 - 13 from the power system.

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If Halt Is Caused by Power, Fan, or Over-Temperature Problems

If a system is stopped because of a power, fan, or over-temperature problem, use the PCM LEDs to diagnose the problem..

If Power Problem Occurs at Power-Up

If the system has a power problem on a cold start, the PCM LEDs are not valid until after DCOK_SENSE has been asserted. The cause is one of the following:

- Broken system fan
- Broken CPU fan
- Power supplied to the system is out of tolerance (a power supply could be broken and the system could still power up)
- PCM failure
- Interlock failure
- Wire problems
- Temperature problem (unlikely)

Recommended Order for Troubleshooting Failure at Power-Up

1. Check to see if any CPU fan or system fan is not spinning. Fans can fail by not spinning and/or not putting out the tachometer output necessary as input to the PCM comparator that checks the fans. (See steps 4 and 5.) Replace broken fan.
2. Replace the PCM.
3. Sequentially remove CPUs and try to power up after you remove a CPU. If the system powers up, the last CPU you removed had a fan failure.
4. Check the output of the power supplies. See the section "Power Supply" in Chapter 4 for locations of +5 and +3.43 volt output pins. If the output is above or below the threshold, replace the faulty power supply.
5. Check the output of each system fan with a voltmeter. Probe the middle of three outputs of the fans with the positive lead of the meter and ground the other probe. The meter should read 2.5 volts to 3 volts. If a fan's output is out of this range, replace the fan.

   NOTE: You will have to disable the interlocks to check the voltages in step 5. You will have only 10 seconds to measure them. There is a 10-second delay before the PCM turns off the power.

   The PCM must sense a change in Vaux (auxiliary voltage) to start the power supplies. Pressing the On button has no effect if the machine halted because of a failure in the power system. The power supplies must be unplugged and plugged back in for the On button to work.

Power Control Module LEDs

The PCM has 11 LEDs visible through the system card cage. The LED display shows the relative placement of the LEDs.

Figure 3-3 PCM LEDs

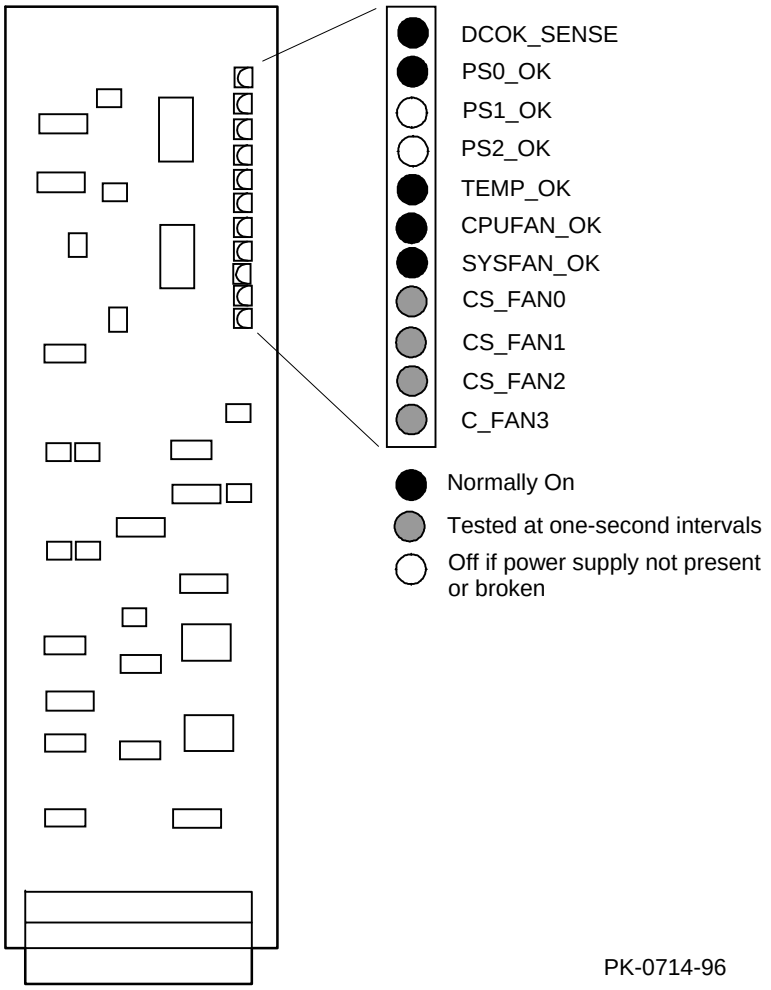


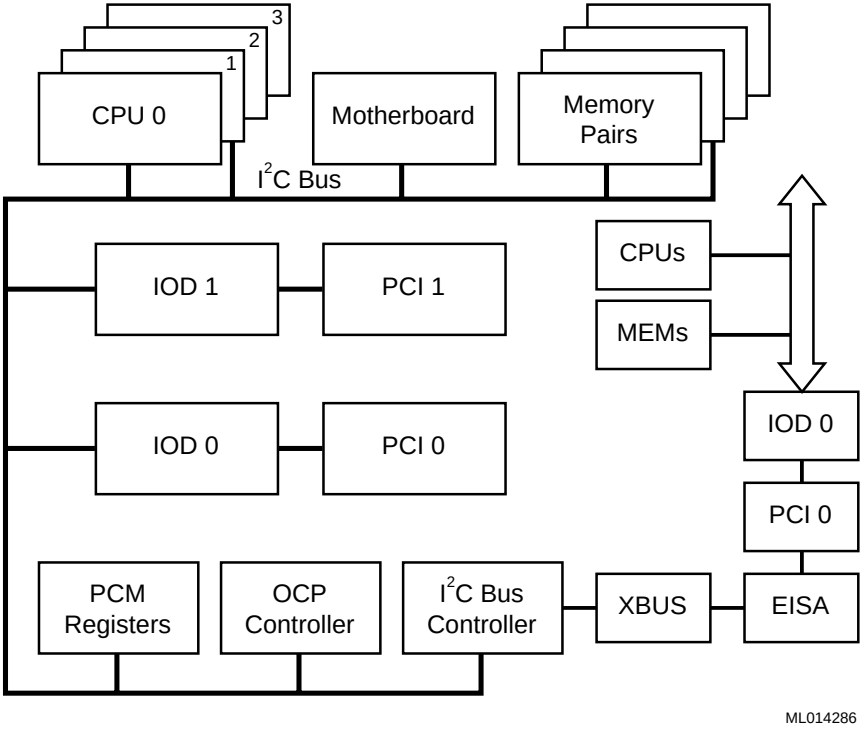
Table 3-1 Power Control Module LED States

LED	State	Description
DCOK_SENSE	On	Both +5.0V and +3.43V are present and within limits.
PS0_OK	On	Power supply 0 is present and has asserted POK_H.
PS1_0K	On Off	Power supply 1 is present and has asserted POK_H. Power supply 1 not present.
PS2_OK	On Off	Power supply 2 is present and has asserted POK_H. Power supply 2 not present.
TEMP_OK	On	The system temperature is below 55° C.
CPUFAN_OK	On Off	All CPU fans are OK. A CPU fan has failed. The specific fan is identified by the CS_FANx or C_FAN3 LED that remains lit.
SYSFAN_OK	On Off	All system fans are OK. A system fan has failed. The specific fan is identified by the CS_FANx that remains lit.
CS_FAN0	On Off	CPU fan 0 and system fan 0 are being sampled or one of them has failed as indicated by CPUFAN_OK and SYSFAN_OK. CPU fan 0 and system fan 0 are not being sampled and are functioning properly.
CS_FAN1	On Off	CPU fan 1 and system fan 1 are being sampled or one of them has failed as indicated by CPUFAN_OK and SYSFAN_OK. CPU fan 1 and system fan 1 are not being sampled and are functioning properly.
CS_FAN2	On Off	CPU fan 2 and system fan 2 are being sampled or one of them has failed as indicated by CPUFAN_OK and SYSFAN_OK. CPU fan 2 and system fan 2 are not being sampled and are functioning properly.
C_FAN3	On Off	CPU fan 3 is being sampled or has failed as indicated by CPUFAN_OK and SYSFAN_OK. Off CPU fan 3 and system fan 3 are not being sampled and are functioning properly.

Troubleshooting with the Maintenance Bus (I^2C Bus)

The I^2C bus (referred to as the "I squared C bus") is a small internal maintenance bus used to monitor system conditions scanned by the power control module, write the fault display, store error state, and track configuration information in the system. Although all system modules (not I/O modules) sit on the maintenance bus, only the I^2C controller accesses it. Everything written or read on the I^2C bus is done by the controller.

Figure 3-4 I^2C Bus Block Diagram



Monitoring System Conditions

The I^2C bus monitors the state of system conditions scanned by the PCM. There are two registers on the PCM:

One records the state of the fans and power supplies and is latched when there is a fault.

The other causes an interrupt on the I^2C bus when a CPU or system fan fails, an over-temperature condition exists, or power supplied to the system is out of tolerance.

The interrupt received by the I^2C bus controller on PCI 0 alerts the system of imminent power shutdown. The controller has 30 seconds to read the two registers and store the information in the EEPROM on the PCM. The SRM console command **show power** reads these registers.

Displaying Faults

The OCP display is written through the I^2C bus.

Writing Error States

Error state is written and read for power conditions. The state of the Halt button (in/out) is read on the I^2C bus.

Tracking Configurations

Each CPU, PCI bridge, PCI motherboard, and system motherboard has an EEPROM that contains information about the module that can be written and read over the I^2C bus. All modules contain the following information:

- Module type
- Module serial number
- Hardware revision
- Firmware revision
- Memory size (only required for memory modules)

Running Diagnostics — Test Command

The test command runs diagnostics on the entire system, CPU devices, memory devices, and the PCI I/O subsystem. The test command runs only from the SRM console. Ctrl/C stops the test.

Example 3-1 Test Command Syntax

```
P00>>> help test

FUNCTION


SYNOPSIS

  test ([-q] [-t <time>] [option]

  where option is:

  cpun

  memn

  pcin


  and n can be one of 0, 1, 2, 3, or *.
```

The entire system is tested by default if no option specified.

*NOTE: Switch from AlphaBIOS to the SRM console to enter the **test** command. From the AlphaBIOS console, press in the Halt button (the LED will light) and reset the system.*

test [**-t** *time*] [**-q**] [*option*]

-t *time*	Specifies the run time in seconds. The default for system test is 600 seconds (10 minutes).
-q	Disables the display of status messages as exerciser processes are started and stopped during testing.
option	Either **cpu***n*, **mem***n*, or **pci***n*, where *n* is 0, 1, 2, 3, or *. If nothing is specified, the entire system is tested.

Testing an Entire System

A test command with no modifiers runs all exercisers for subsystems and devices on the system. I/O devices tested are supported boot devices. The test runs for 10 minutes.

Example 3-2 Sample Test Command

```
P00>>> test
Console is in diagnostic mode
System test, runtime 600 seconds


Type ^C to stop testing


Configuring system..
polling ncr0 (NCR 53C810) slot 1, bus 0 PCI, hose 1   SCSI Bus ID 7
dka500.5.0.1.1     DKa500                   RRD45  1645
polling ncr1 (NCR 53C810) slot 3, bus 0 PCI, hose 1   SCSI Bus ID 7
dkb200.2.0.3.1     DKb200                   RZ29B  0007
dkb400.4.0.3.1     DKb400                   RZ29B  0007
polling floppy0 (FLOPPY) PCEB - XBUS hose 0
dva0.0.0.1000.0    DVA0                      RX23
polling tulip0 (DECchip 21040-AA) slot 2, bus 0 PCI, hose 1
ewa0.0.0.2.1: 08-00-2B-E5-B4-1A


Testing EWA0 network device


Testing VGA (alphanumeric mode only)


Starting background memory test, affinity to all CPUs..
Starting processor/cache thrasher on each CPU..
Starting processor/cache thrasher on each CPU..
Starting processor/cache thrasher on each CPU..
```

```
Starting processor/cache thrasher on each CPU..


Testing SCSI disks (read-only)
No CD/ROM present, skipping embedded SCSI test
Testing other SCSI devices (read-only)..


Testing floppy drive (dva0, read-only)
```

ID	Program	Device	Pass	Hard/Soft		Bytes Written	Bytes Read
00003047	memtest	memory	1	0	0	134217728	134217728
00003050	memtest	memory	205	0	0	213883392	213883392
00003059	memtest	memory	192	0	0	200253568	200253568
00003062	memtest	memory	192	0	0	200253568	200253568
00003084	memtest	memory	80	0	0	82827392	82827392
000030d8	exer_kid	dkb200.2.0.3	26	0	0	0	13690880
000030d9	exer_kid	dkb400.4.0.3	26	0	0	0	13674496
0000310d	exer_kid	dva0.0.0.100	0	0	0	0	0

ID	Program	Device	Pass	Hard/Soft		Bytes Written	Bytes Read
00003047	memtest	memory	1	0	0	432013312	432013312
00003050	memtest	memory	635	0	0	664716032	664716032
00003059	memtest	memory	619	0	0	647940864	647940864
00003062	memtest	memory	620	0	0	648989312	648989312
00003084	memtest	memory	263	0	0	274693376	274693376
000030d8	exer_kid	dkb200.2.0.3	90	0	0	0	47572992
000030d9	exer_kid	dkb400.4.0.3	90	0	0	0	47523840
0000310d	exer_kid	dva0.0.0.100	0	0	0	0	327680

```
ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
00003047      memtest memory            1    0    0     727711744    727711744
00003050      memtest memory         1054    0    0    1104015744   1104015744
00003059      memtest memory         1039    0    0    1088289024   1088289024
00003062      memtest memory         1041    0    0    1090385920   1090385920
00003084      memtest memory          447    0    0     467607808    467607808
000030d8     exer_kid dkb200.2.0.3    155    0    0             0     81488896
000030d9     exer_kid dkb400.4.0.3    155    0    0             0     81472512
0000310d     exer_kid dva0.0.0.100      1    0    0             0       607232
Testing aborted. Shutting down tests.
Please wait..

System test complete

^C
P00>>>
```

Testing Memory

The test mem command tests individual memory devices or all memory. The test shown in Example 3-3 runs for 2 minutes.

Example 3-3 Sample Test Memory Command

```
P00>>> test memory
Console is in diagnostic mode
System test, runtime 120 seconds

Type ^C to stop testing

Starting background memory test, affinity to all CPUs..
Starting memory thrasher on each CPU..
Starting memory thrasher on each CPU..
Starting memory thrasher on each CPU..
Starting memory thrasher on each CPU..

 ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
000046d7      memtest memory            1    0    0      48234496     48234496
000046e0      memtest memory          122    0    0     126862208    126862208
000046e9      memtest memory          111    0    0     115329280    115329280
000046f2      memtest memory          109    0    0     113232384    113232384
000046fb      memtest memory           41    0    0      41937920     41937920

 ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
000046d7      memtest memory            1    0    0     226492416    226492416
000046e0      memtest memory          566    0    0     592373120    592373120
000046e9      memtest memory          555    0    0     580840192    580840192
000046f2      memtest memory          554    0    0     579791744    579791744
```

```
000046fb      memtest memory          211    0    0     220174080    220174080

 ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
000046d7      memtest memory            1    0    0     404750336    404750336
000046e0      memtest memory         1011    0    0    1058932480   1058932480
000046e9      memtest memory         1000    0    0    1047399552   1047399552
000046f2      memtest memory          999    0    0    1046351104   1046351104
000046fb      memtest memory          381    0    0     398410240    398410240
 ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
000046d7      memtest memory            1    0    0     583008256    583008256
000046e0      memtest memory         1456    0    0    1525491840   1525491840
000046e9      memtest memory         1446    0    0    1515007360   1515007360
000046f2      memtest memory         1444    0    0    1512910464   1512910464
000046fb      memtest memory          550    0    0     575597952    575597952
 ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
000046d7      memtest memory            1    0    0     761266176    761266176
000046e0      memtest memory         1901    0    0    1992051200   1992051200
000046e9      memtest memory         1892    0    0    1982615168   1982615168
000046f2      memtest memory         1889    0    0    1979469824   1979469824
000046fb      memtest memory          720    0    0     753834112    753834112

 ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
000046d7      memtest memory            1    0    0     937426944    937426944
000046e0      memtest memory         2346    0    0    2458610560   2458610560
000046e9      memtest memory         2337    0    0    2449174528   2449174528
000046f2      memtest memory         2333    0    0    2444980736   2444980736
000046fb      memtest memory          890    0    0     932070272    932070272
```

```
Memory test complete
Test time has expired...
P00>>>
```

Testing PCI Buses and Devices

The test pci command tests PCI buses and devices. The test runs for 2 minutes.

Example 3-4 Sample Test Command for PCI

```
P00>>> test pci*
Console is in diagnostic mode
System test, runtime 120 seconds

Type ^C to stop testing

Configuring all PCI buses..
polling ncr0 (NCR 53C810) slot 1, bus 0 PCI, hose 1   SCSI Bus ID 7
dka500.5.0.1.1     DKa500                   RRD45  1645
polling ncr1 (NCR 53C810) slot 3, bus 0 PCI, hose 1   SCSI Bus ID 7
dkb200.2.0.3.1     DKb200                   RZ29B  0007
dkb400.4.0.3.1     DKb400                   RZ29B  0007
polling tulip0 (DECchip 21040-AA) slot 2, bus 0 PCI, hose 1
ewa0.0.0.2.1: 08-00-2B-E5-B4-1A
polling floppy0 (FLOPPY) PCEB - XBUS hose 0
dva0.0.0.1000.0    DVA0                      RX23

Testing all PCI buses..

Testing EWA0 network device

Testing VGA (alphanumeric mode only)

Testing SCSI disks (read-only)

Testing floppy (dva0, read-only)
```

```
 ID       Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read

-------- ------------ ------------ ------ --------- ------------- ------------
00002c29     exer_kid dkb200.2.0.3     27    0    0             0     14642176
00002c2a     exer_kid dkb400.4.0.3     27    0    0             0     14642176
00002c5e     exer_kid dva0.0.0.100      0    0    0             0            0

Program      Device       Pass  Hard/Soft Bytes Written  Bytes Read
-------- ------------ ------------ ------ --------- ------------- ------------
00002c29     exer_kid dkb200.2.0.3     92    0    0             0     48689152
00002c2a     exer_kid dkb400.4.0.3     92    0    0             0     48689152
00002c5e     exer_kid dva0.0.0.100      0    0    0             0       286720
Testing aborted. Shutting down tests.
Please wait..

Testing complete

^C
P00>>>
```

4
Power System

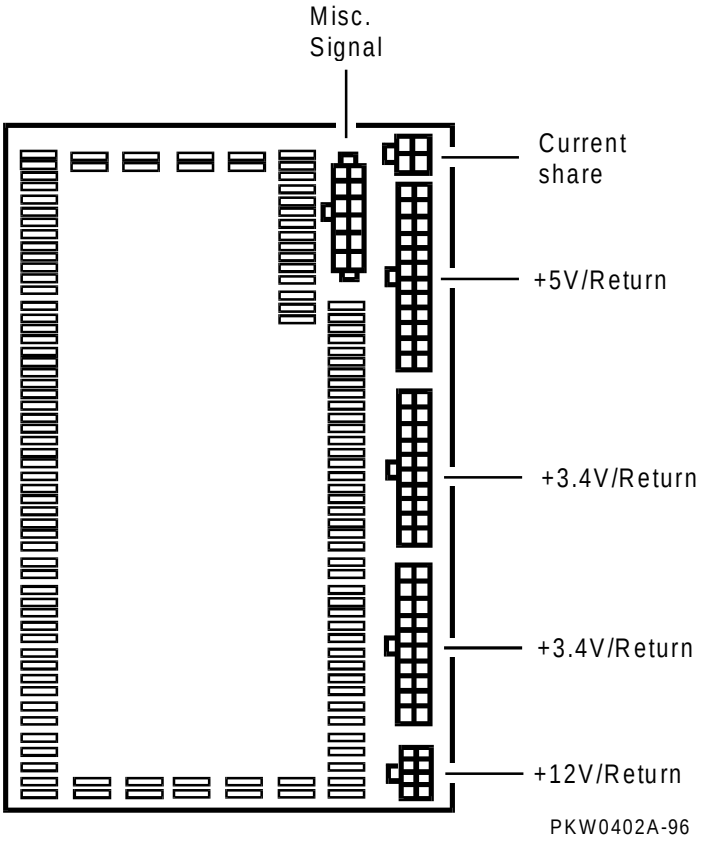
This chapter describes the DIGITAL Server 7300/7300R series power system:

- Power Supply
- Power Control Module Features
- Power Circuit and Cover Interlocks
- Power-Up/Down Sequence
- Cabinet Power Configuration Rules
- Pedestal Power Configuration Rules (North America and Japan)
- Pedestal Power Configuration Rules (Europe and Asia Pacific)

Power Supply

Power supply outputs are shown in Figure 4-1.

Figure 4-1 Power Supply Outputs



Power Supply Features

- 90–264 Vrms input
- 450 watts output. Output voltages are as follows:

Output Voltage	Min. Voltage	Max. Voltage	Max. Current
+5.0	4.85	5.25	50
+3.43	3.400	3.465	75
+12	11.5	12.6	11
–12	–10.9	–13.2	0.2
–5.0	–4.6	–5.5	0.2
Vaux	8.5	9.5	0.05

- Remote sense on +5.0V and +3.43V

  +5.0V is sensed on all CPUs in the system, the system bus motherboard, and the PCI bus motherboard(s).

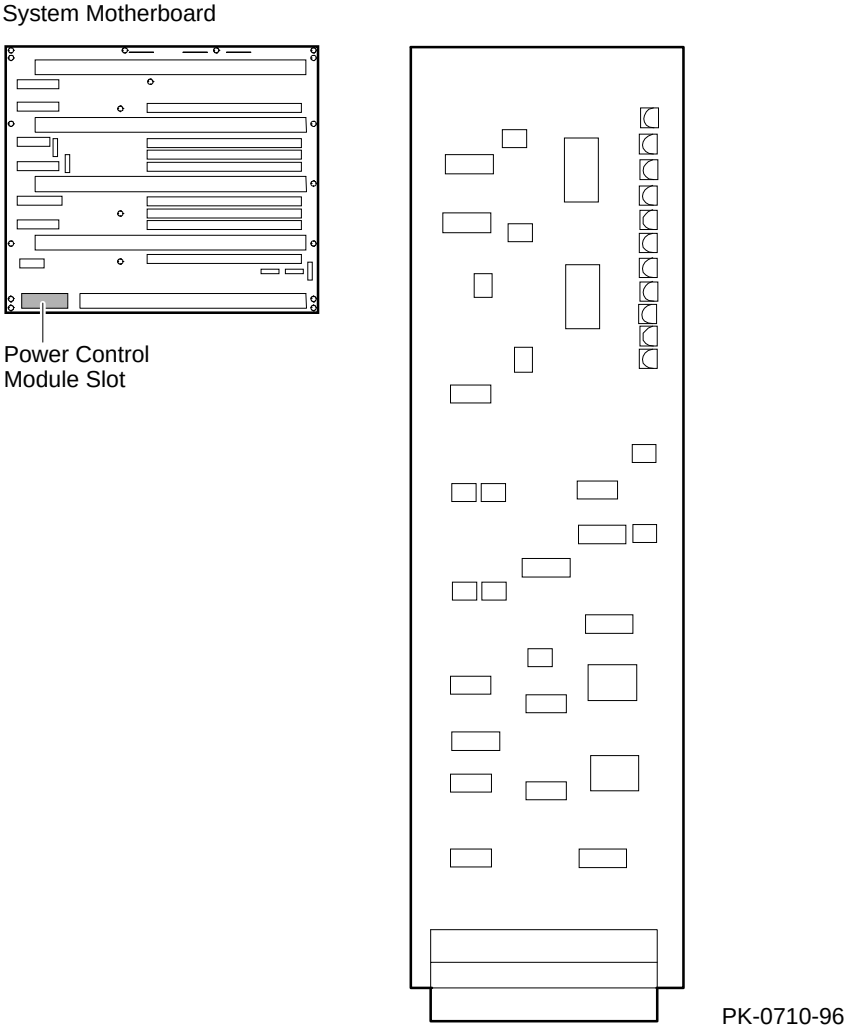
  +3.43V is sensed on all CPUs in the system and the system bus motherboard.
- Current share on +5.0V, +3.43V, and +12V.
- 1 % regulation on +3.43V.
- Fault protection (latched). If a fault is detected by the power supply, it will shut down. The faults detected are:

  Overvoltage
  Overcurrent
  Power overload
- DC_ENABLE_L input signal starts the DC outputs.
- POK_H output signal indicates that the power supply is operating properly.

Power Control Module Features

The power control module (54-24117-01) is located behind the B3040-AA module, the system bus to PCI bus bridge module.

Figure 4-2 Power Control Module



The power control module performs the following functions:

- Controls the power-up/down sequencing.
- Monitors the combined output of power supplies VDD (3.43V) and VCC (5.0V) and asserts DCOK_SENSE if these voltages are within range and asserts POWER_FAULT_L causing an immediate power shutdown if either is not.
- Monitors system temperature and asserts TEMP_FAIL, if temperature exceeds 55° C.
- Monitors CPU and system drawer fans and asserts CPUFAN_OK if all CPU fans are functioning properly, asserts SYSTEM_FAN_OK if the drawer cooling fans are functioning properly; otherwise it asserts FAN_FAULT_L. Each fan is checked at 1 second intervals.
- Powers down the system 30 seconds after detecting TEMP_FAIL, or the absence of CPUFAN_OK, or the absence of SYSTEM_FAN_OK by asserting POWER_FAULT_L.
- Provides visual indication of faults through LEDs.
- Has two registers, one that generates interrupts when bits change, and one that latches errors but does not generate interrupts.

Power Circuit and Cover Interlocks

Figure 4-3 is a diagram of the power circuit. Note that B305n in the diagram stands for either the B3050-AA or B3052-AA PCI Motherboard.

Figure 4-3 Power Circuit Diagram

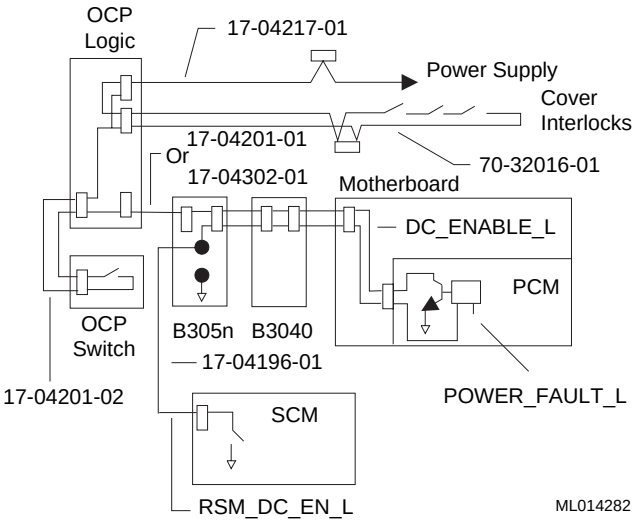


Figure 4-3 shows the distribution of power throughout the system drawer.
Opens in the circuit, the PCM signal POWER_FAULT_L or the SCM signal RSM_DC_EN_L interrupt DC power applied to the system. The opens can be caused by the On/Off button or by the cover interlocks. The POWER_FAULT_L signal is asserted by the PCM module if it detects a fault and the RSM_DC_EN_L is controlled remotely.

A failure anywhere in the circuit results in the removal of DC power. A potential failure is the relay used on the SCM modules to control the RSM_DC_EN_L signal.

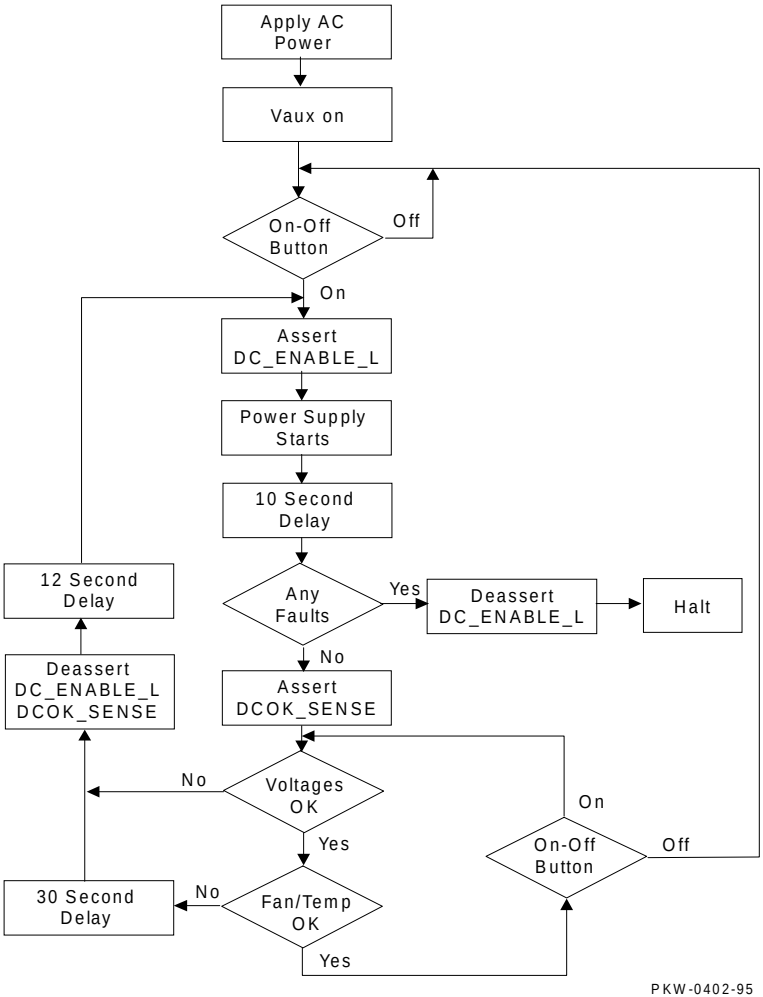
The DIGITAL Server 7300/7300R series system drawers have three cover interlocks: one for the system bus card cage, one for the PCI card cage, and one for the power and system fan area.

To override the cover interlocks, find a suitable object to close the interlock circuit at the location identified in Figure 4-3. The switch assembly that contains single switches for all three covers is located where all three covers meet.

Power-Up/Down Sequence

The On/Off button can be controlled manually or remotely. The button is on the OCP. Remote power control is provided though the remote I/O port connected to the PCI. The power-up/down sequence flow is shown below.

Figure 4-4 Power Up/Down Sequence Flowchart



When AC is applied to the system, Vaux (auxiliary voltage) is asserted and is sensed by the PCM. The PCM asserts DC_ENABLE_L starting the power supplies. If there is a

hard fault on power-up, the power supplies shut down immediately. If there is not a hard fault on power-up, the power system powers up and remains up until the system is shut off or the PCM senses a fault. If the PCM senses a power fault, the power system attempts to restore power and will restore power if the fault is not sensed a second time. If the fault is still present, the power system shuts down.

Because Vaux is independent of the power supply start, you must remove the AC plugs at the front of the supplies to reset Vaux, allowing capacitors to drain voltage. All power failures require this procedure since the PCM must sense a change in Vaux to start the power supplies.

Cabinet Power Configuration Rules

There are different cabinets with different power delivery systems. See Chapter 1 for a description of the differences. A bar code label designating the cabinet variation is located inside the back door in the upper left corner of the bezel holding the door. The two variations are: H9A10-EN and H9A10-EP.

Figure 4-5 shows the H9A10-EN and -EP single-drawer cabinet power configuration. The single-drawer H9A10-EP is shown with the H7600-DB controller.

Figure 4-5 -EN & -EP Single Drawer Cabinet Power Configuration

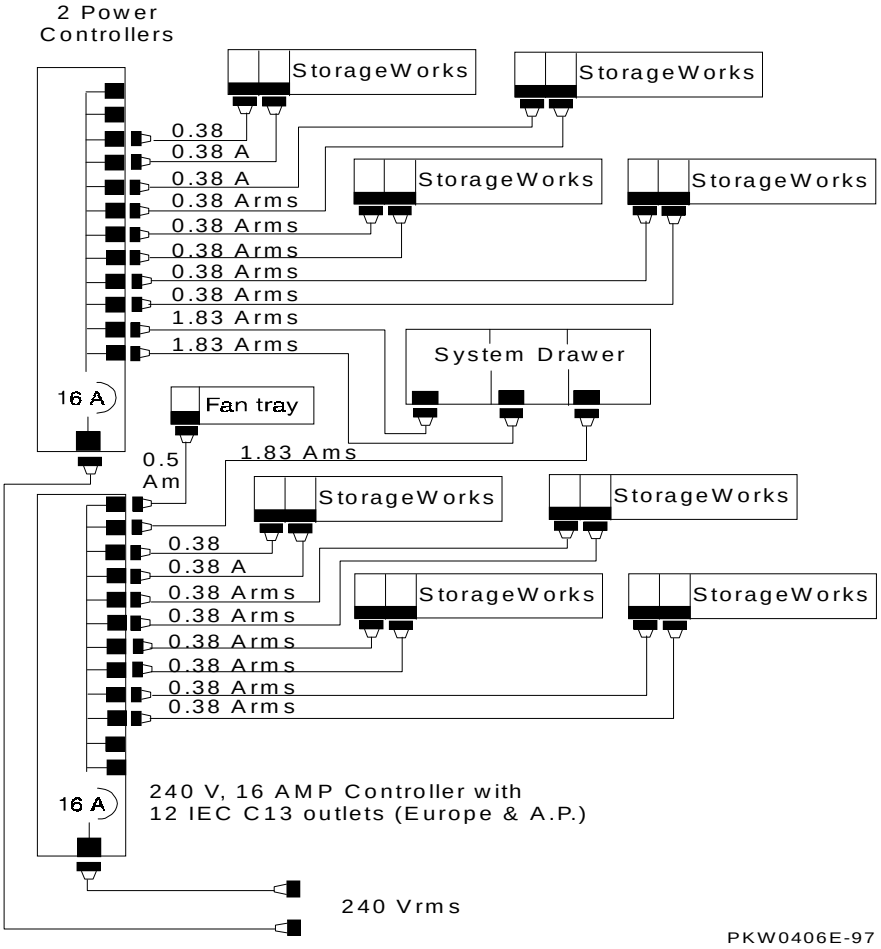
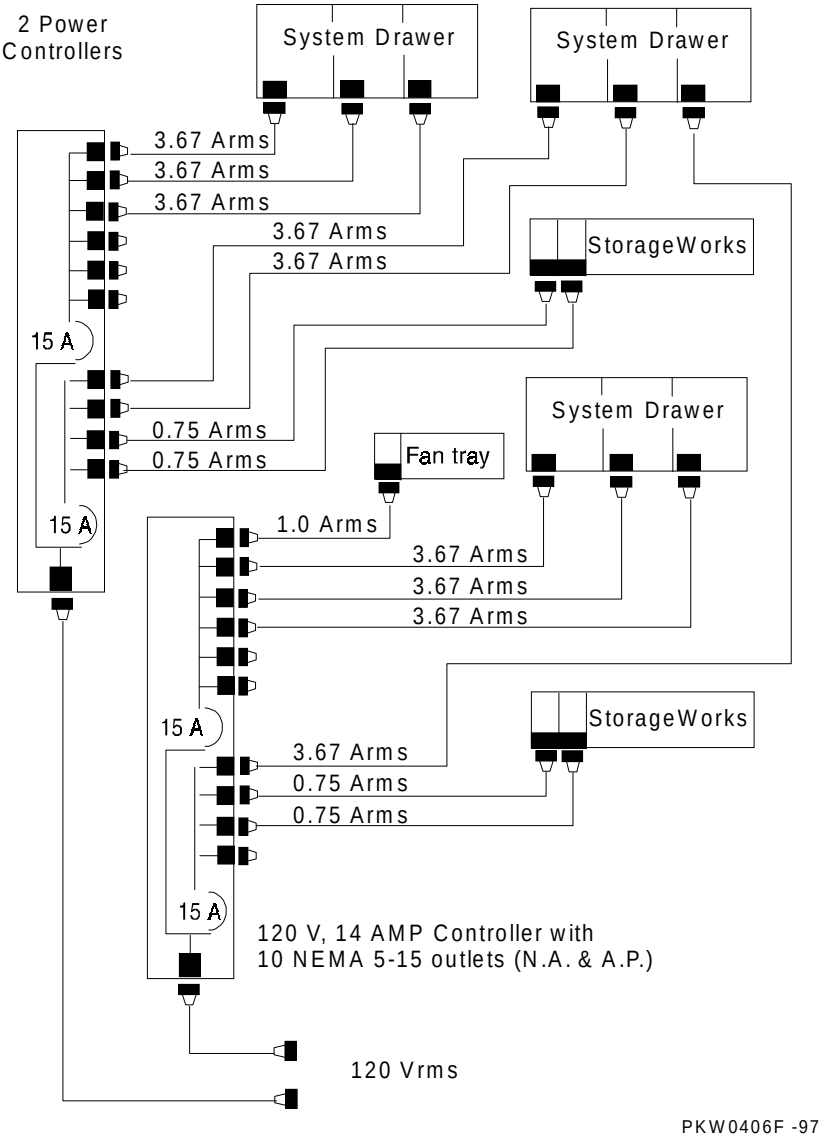


Figure 4-6 shows an -EN three-drawer cabinet power configuration. The three-drawer -EN is shown with the H7600-AA controller.

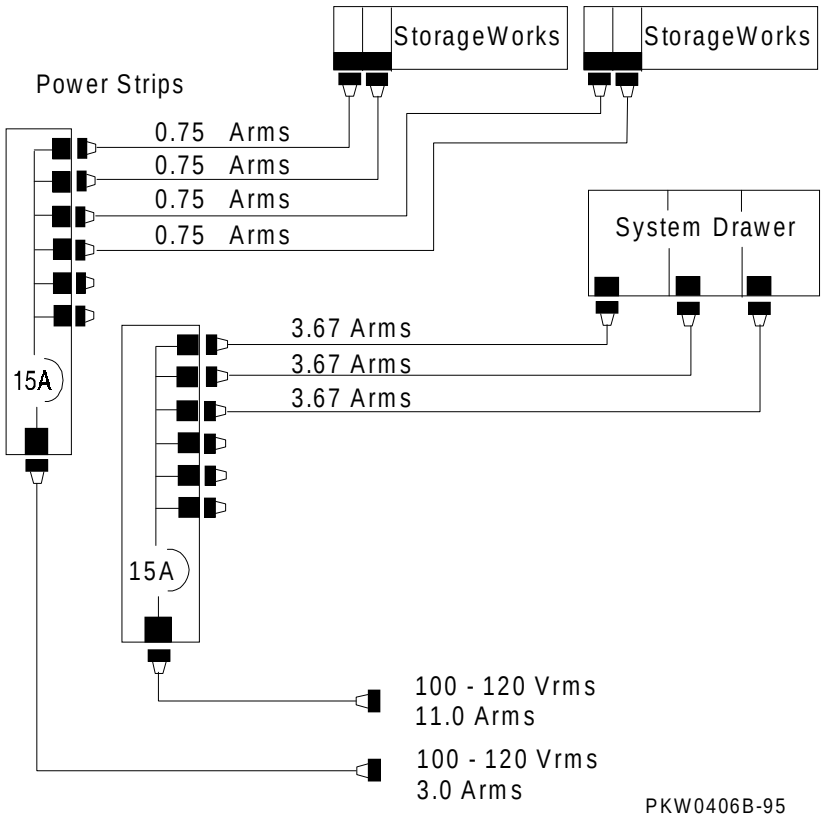
Figure 4-6 -EN Three Drawer Cabinet Power Configuration



Pedestal Power Configuration Rules (North America and Japan)

Figure 4-7 show pedestal power distribution in North America and Japan.

Figure 4-7 Pedestal Power Distribution (N.A. and Japan)



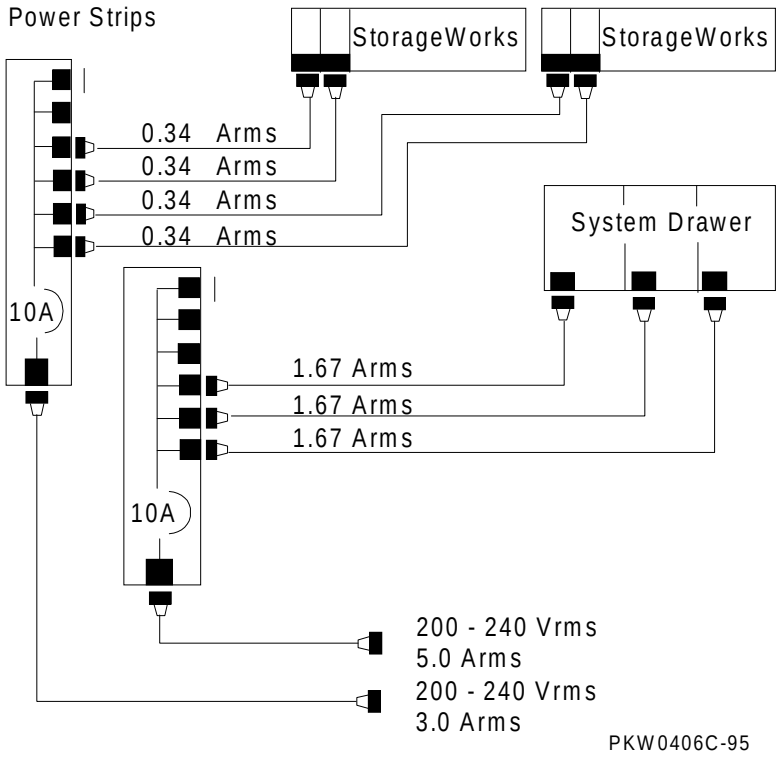
Total Power Available (Assuming a 15 A branch)	N. America: 1800 VA per branch circuit and 1400 VA per line cord Japan: 1500 VA per branch circuit and 1200 VA per line cord
Single Drawer	1100 VA
Single StorageWorks Shelf	150 VA
Outlets	12 NEMA receptacles

Power Strip	Single AC power strip supports one system drawer and one StorageWorks shelf. When two AC power strips are used, combined AC input line current cannot exceed the site circuit breaker restriction, assuming both strips are plugged in to the same circuit.

Pedestal Power Configuration Rules (Europe and Asia Pacific)

Figure 4-8 shows pedestal power distribution in Europe and Asia/Pacific.

Figure 4-8 Pedestal Power Distribution (Europe and AP)



Total Power Available	2200 VA per power strip
Single Drawer	1100 VA
Single StorageWorks Shelf	150 VA
Outlets	10 IEC 320 receptacles max. One receptacle is blocked on each power strip to control leakage.
Power Strip	Single AC power strip supports one system drawer and three StorageWorks shelves.

5

Error Detection with Error Registers

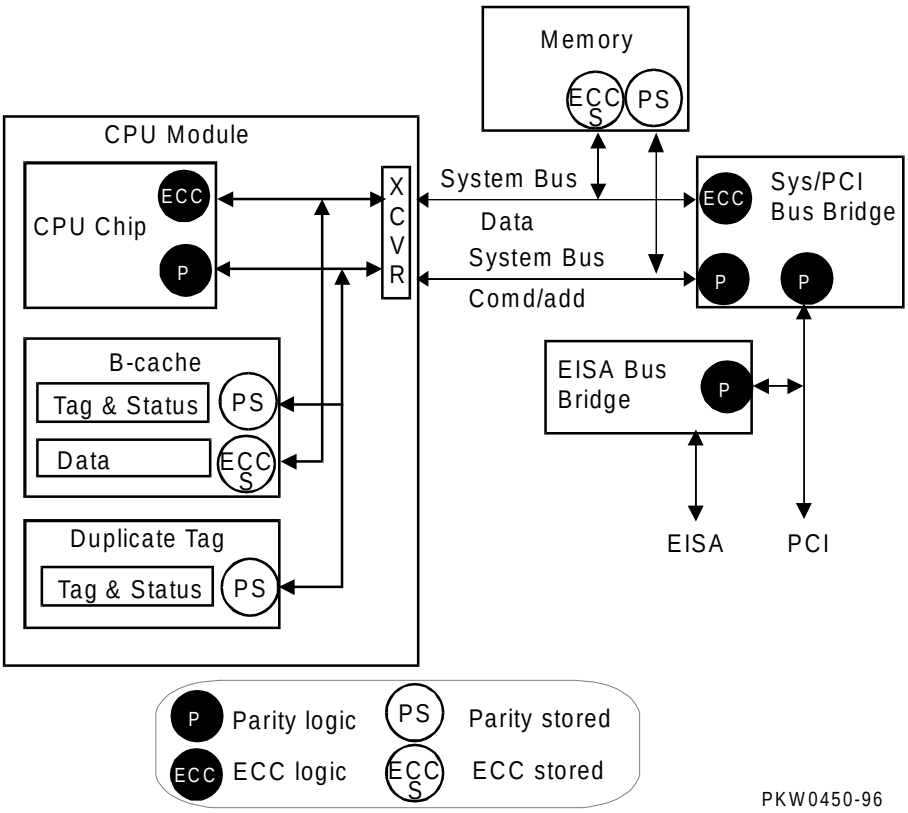
This chapter describes error detection with error registers. It includes the following topics:

- Overview of Error Detection
- Error Registers
- Troubleshooting IOD-Detected Errors
- Double Error Halts and Machine Checks While in PAL Mode

Overview of Error Detection

Error detection is performed by CPUs, the IOD, and the EISA to PCI bus bridge. (The IOD is the acronym used by software to refer to the system bus to PCI bus bridge.)

Figure 5-1 Error Detector Placement



Lines Protected	Device
ECC Protected	
System bus data lines	IOD on every transaction, CPU when using the bus
B-cache	IOD on every transaction, CPU when using the bus
Parity Protected	
System bus command/address lines	IOD on every transaction, CPU when using the bus
Duplicate tag store	IOD on every transaction, CPU when using the bus
B-cache index lines	CPU
PCI bus	IOD
EISA bus	EISA bridge

As shown in Figure 5-1 and the accompanying table, the CPU chip is isolated by transceivers (XVER) from the data and command/address lines on the module. This allows the CPU chip access to the duplicate tag and B-cache while the system bus is in use. The CPU detects errors only when it is the consumer of the data. The IOD detects errors on each system bus cycle regardless of whether it is involved in the transaction.

System bus errors detected by the CPU may also be detected by the IOD. You need to check the IOD for errors any time there is a CPU machine check.

If the CPU sees bad data and the IOD does not, the CPU is at fault.

If both the CPU and the IOD see bad data on the system bus, either memory or a secondary CPU is the cause. In such a case, the Dirty bit, bit<20>, in the IOD MC_ERR1 Register should be set or clear. If the Dirty bit is set, the source of the data is a CPU's cache destined for a different CPU. If the Dirty bit is not set, memory caused the bad data on the bus. In this case, multiple error log entries occur and must be analyzed together to determine the cause of the error.

Hard Errors

There are two categories of hard errors:

- System-independent errors detected by the CPU. These errors are processor machine checks and are:

Internal EV5 or EV56 cache errors
CPU B-cache module errors

- System-dependent errors detected by both the CPU and IOD. These errors are system machine checks and are:

  CPU-detected external reference errors
  IOD hard error interrupts

  The IOD can detect hard errors on either side of the bridge.

Soft Errors

There are two categories of soft errors:

- System-independent errors detected and corrected by the CPU.
- System-dependent errors that are correctable single-bit errors on the system bus.

Error Registers

The DIGITAL Server 7300/7300R include registers that hold error information that you can use for troubleshooting. These registers include:

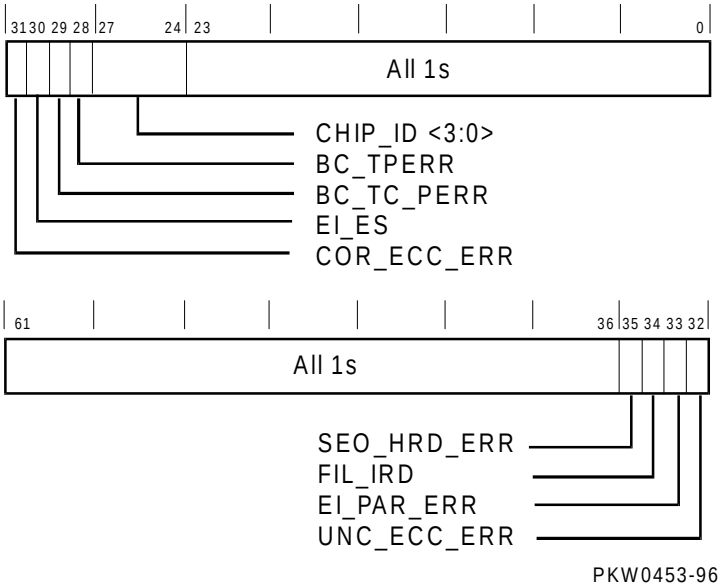
- External Interface Status Register – EI_STAT
- External Interface Address Register - EI_ADDR
- MC Error Information Register 0 (MC_ERR0 - Offset = 800)
- MC Error Information Register 1 (MC_ERR1 - Offset = 840)
- CAP Error Register (CAP_ERR - Offset = 880)
- PCI Error Status Register 1 (PCI_ERR1 - Offset = 1040)

External Interface Status Register – EI_STAT

The EI_STAT register is a read-only register that is unlocked and cleared by any PALcode read. Subject to some restrictions, a read of EI_STAT also unlocks the EL_ADDR, BC_TAG_ADDR, and FILL_SYN registers. EI_STAT is not unlocked or cleared by reset.

Address FF FFF0 0168

Type R



Fill data from B-cache or main memory can have correctable or non-correctable errors in ECC mode. In parity mode, fill data parity errors are treated as non-correctable hard errors. System address/command parity errors are always treated as non-correctable hard errors, irrespective of the mode. The sequence for reading, unlocking, and clearing EI_STAT, EI_ADDR, BC_TAG_ADDR, and FILL_SYN is as follows:

1. Read the EI_ADDR, BC_TAG_ADDR, and FIL_SYN registers in any order. Does not unlock or clear any register.
2. Read the EI_STAT register. This operation unlocks the EI_ADDR, BC_TAG_ADDR, and FILL_SYN registers. It also unlocks the EI_STAT register subject to conditions given in Table 5-2, which defines the loading and locking rules for external interface registers.

   NOTE: If the first error is correctable, the registers are loaded but not locked. On the second correctable error, the registers are neither loaded nor locked.

   Registers are locked on the first non-correctable error except the second hard error bit. This bit is set only for an non-correctable error that follows an non-correctable error. A correctable error that follows an non-correctable error is not logged as a second error. B-cache tag parity errors are non-correctable in this context.

Table 5-1 External Interface Status Register

Name	Bits	Type	Description
COR_ECC_ERR	<31>	R	**Correctable ECC Error.** Indicates that fill data received from outside the CPU contained a correctable ECC error.
EI_ES	<30>	R	**External Interface Error Source.** When set, indicates that the error source is fill data from main memory or a system address/command parity error. When clear, the error source is fill data from the B-cache. This bit is only meaningful when <COR_ECC_ERR>, <UNC_ECC_ERR>, or <EI_PAR_ERR> is set in this register. This bit is not defined for a B-cache tag error (BC_TPERR) or a B-cache tag control parity error (BC_TC_ERR).
BC_TC_PERR	<29>	R	**B-Cache Tag Control Parity Error.** Indicates that a B-cache read transaction encountered bad parity in the tag control RAM.
BC_TPERR	<28>	R	**B-Cache Tag Address Parity Error.** Indicates that a B-cache read transaction encountered bad parity in the tag address RAM.
CHIP_ID	<27:24>	R	**Chip Identification.** Read as "4." Future update revisions to the chip will return new unique values.
	<23:0>		All ones.

Continued

Table 5-1 External Interface Status Register (continued)

Name	Bits	Type	Description
	<63:36>		All ones.
SEO_HRD_ERR	<35>	R	Second External Interface Hard Error. Indicates that a fill from B-cache or main memory, or a system address/command received by the CPU has a hard error while one of the hard error bits in the EI_STST register is already set.
FIL_IRD	<34>	R	Fill I-Ref D-Ref. When set, indicates that the error occurred during an I-ref fill. When clear, indicates that the error occurred during a D-ref fill. This bit has meaning only when one of the ECC or parity error bits is set. This bit is not defined for a B-cache tag parity error (BC_TPERR) or a B-cache tag control parity error (BC_TC_ERR).
EI_PAR_ERR	<33>	R	External Interface Command/Address Parity Error. Indicates that an address and command received by the CPU has a parity error.
UNC_ECC_ER	<32>	R	Non-correctable ECC Error. Indicates that fill data received from outside the CPU contained an non-correctable ECC error. In parity mode, this bit indicates a data parity error.

External Interface Address Register - EI_ADDR

The EI_ADDR register contains the physical address associated with errors reported by the EI_STAT register. It is unlocked by a read of the EI_STAT Register. This register is meaningful only when one of the error bits is set.

Address FF FFF0 0148

Access R

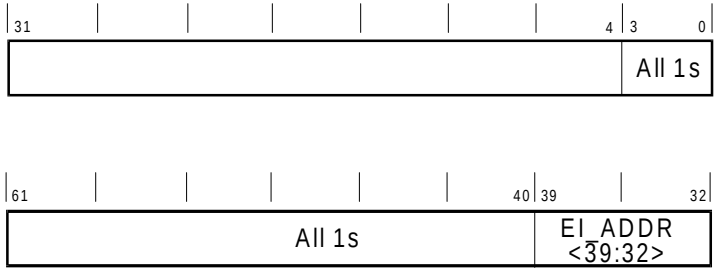


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Table 5-2 Loading and Locking Rules for External Interface Registers

Correct -able Error	Non-correct -able Error	Second Hard Error	Load Register	Lock Register	Action When EI_STAT is Read
0	0	Not possible	No	No	Clears and unlocks all registers
1	0	Not possible	Yes	No	Clears and unlocks all registers
0	1	0	Yes	Yes	Clears and unlocks all registers
1[1]	1	0	Yes	Yes	Clear bit (c) does not unlock. Transition to "0,1,0" state.
0	1	1	No	Already locked	Clears and unlocks all registers
1[1]	1	1	No	Already locked	Clear bit (c) does not unlock. Transition to "0,1,1" state.

[1] These are special cases. It is possible that when EI_ADDR is read, only the correctable error bit is set and the registers are not locked. By the time EI_STAT is read, a non-correctable error is detected and the registers are loaded again and locked. The value of EI_ADDR read earlier is no longer valid. Therefore, for the "1,1,x" case, when EI_STAT is read correctable, the error bit is cleared and the registers are not unlocked or cleared. Software must re-execute the IPR read sequence. On the second read operation, error bits are in "0,1,x" state, all the related IPRs are unlocked, and EI_STAT is cleared.

MC Error Information Register 0 (MC_ERR0 - Offset = 800)

The low-order MC bus (system bus) address bits are latched into this register when the system bus to PCI bus bridge detects an error event. If the event is a hard error, the register bits are locked. A write to clear symptom bits in the CAP Error Register unlocks this register. When the valid bit (MC_ERR_VALID) in the CAP Error Register is clear, the contents are undefined.

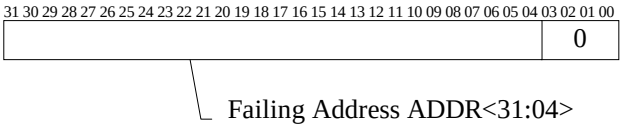


Table 5-3 MC Error Information Register 0

Name	Bits	Type	Initial State	Description
ADDR<31:4>	<31:4>	RO	0	Contains the address of the transaction on the system bus when an error is detected.
Reserved	<3:0>	RO	0	

MC Error Information Register 0 (MC_ERR0 - Offset = 800)

The low-order MC bus (system bus) address bits are latched into this register when the system bus to PCI bus bridge detects an error event. If the event is a hard error, the register bits are locked. A write to clear symptom bits in the CAP Error Register unlocks this register. When the valid bit (MC_ERR_VALID) in the CAP Error Register is clear, the contents are undefined.

Table 5-4 MC Error Information Register 0

Name	Bits	Type	Initial State	Description
ADDR<31:4>	<31:4>	RO	0	Contains the address of the transaction on the system bus when an error is detected.
Reserved	<3:0>	RO	0	

MC Error Information Register 1 (MC_ERR1 - Offset = 840)

The high-order MC bus (system bus) address bits and error symptoms are latched into this register when the system bus to PCI bus bridge detects an error. If the event is a hard error, the register bits are locked. A write to clear symptom bits in the CAP Error Register unlocks this register. When the valid bit (MC_ERR_VALID) in the CAP Error Register is clear, the contents are undefined.

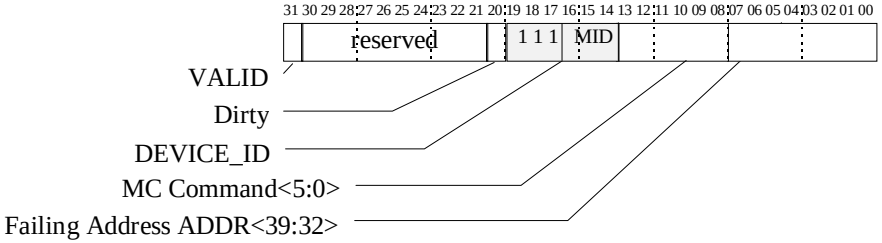


Table 5-5 MC Error Information Register 1

Name	Bits	Type	Initial State	Description
VALID	<31>	RO	0	Logical OR of bits <30:23> in the CAP_ERR Register. Set if MC_ERR0 and MC_ERR1 contain a valid address.
Reserved	<30:21>	RO	0	
Dirty	<20>	RO	0	Set if the system bus error was associated with a Read/Dirty transaction. When set, the device ID field <19:14> does not indicate the source of the data.
Reserved	<19:17>			All ones.
DEVICE_ID	<16:14>	RO	0	Slot number of bus master at the time of the error.
MC_CMD<5:0>	<13:8>	RO	0	Active command at the time the error was detected.
ADDR<39:32>	<7:0>	RO	0	Address bits <39:32> of the transaction on the system bus when an error is detected.

CAP Error Register (CAP_ERR - Offset = 880)

CAP_ERR is used to log information pertaining to an error detected by the CAP or MDP ASIC. If the error is a hard error, the register is locked. All bits, except the LOST_MC_ERR bit, are locked on hard errors. CAP_ERR remains locked until the CAP error is written to clear each individual error bit.

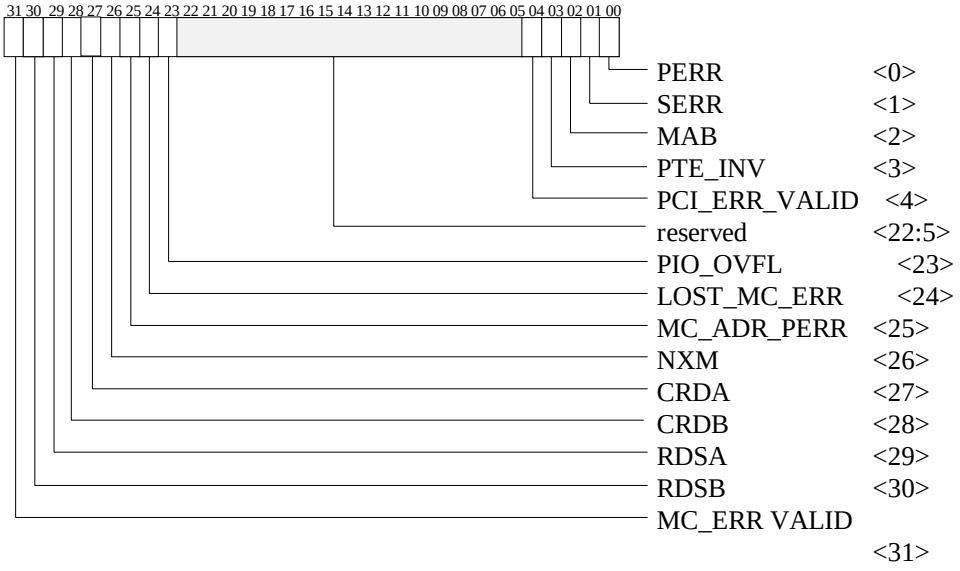


Table 5-6 CAP Error Register

Name	Bits	Type	Initial State	Description
MC_ERR VALID	<31>	RO	0	Logical OR of bits <30:23> in this register. When set MC_ERR0 and MC_ERR1 are latched.
RDSB	<30>	RW1C	0	Non-correctable ECC error detected by MDPB. Clear state in MDPB before clearing this bit.
RDSA	<29>	RW1C	0	Non-correctable ECC error detected by MDPA. Clear state in MDPA before clearing this bit.
CRDB	<28>	RW1C	0	Correctable ECC error detected by MDPB. Clear state in MDPB_STAT before clearing this bit.
CRDA	<27>	RW1C	0	Correctable ECC error detected by MDPA. Clear state in MDPA_STAT before clearing this bit.
NXM	<26>	RW1C	0	System bus master transaction status NXM (Read with Address bit <39> set but transaction not pended or transaction target above the top of memory register.) CPU will also get a fill error on reads.
MC_ADR_PERR	<25>	RW1C	0	Set when a system bus command/address parity error is detected.

Continued

Table 6-5 CAP Error Register (continued)

Name	Bits	Type	Initial State	Description
LOST_MC_ERR	<24>	RW1C	0	Set when an error is detected but not logged because the associated symptom fields and registers are locked with the state of an earlier error.
PIO_OVFL	<23>	RW1C	0	Set when a transaction that targets this system bus to PCI bus bridge is not serviced because the buffers are full. This is a symptom of setting the PEND_NUM field in CAP_CNTL to an incorrect value.
Reserved	<22:5>	RO	0	
PCI_ERR_VALID	<4>	RO	0	Logical OR of bits <3:0> of this register. When set, the PCI error address register is locked.
PTE_INV	<3>	RW1C	0	Invalid page table entry on scatter/gather access.
MAB	<2>	RW1C	0	PCI master state machine detected PCI Target Abort (likely cause: NXM) (except Special Cycle). On reads fill error is also returned.
SERR	<1>	RW1C	0	PCI target state machine observed SERR#. CAP asserts SERR when it is master and detects target abort.
PERR	<0>	RW1C	0	PCI master state machine observed PERR#.

PCI Error Status Register 1 (PCI_ERR1 - Offset = 1040)

PCI_ERR1 is used by the system bus to PCI bus bridge to log bus address <31:0> pertaining to an error condition logged in CAP_ERR. This register always captures PCI address <31:0>, even for a PCI DAC cycle. When the PCI_ERR_VALID bit in CAP_ERR is clear, the contents are undefined.

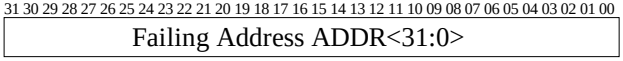


Table 5-7 PCI Error Status Register 1

Name	Bits	Type	Initial State	Description
ADDR<31:0>	<31:0>	RO	0	Contains address bits <31:0> of the transaction on the PCI bus when an error is detected.

Troubleshooting IOD-Detected Errors

Step 1

Read the CAP Error Registers on both PCI bridges (F9E0000880 and FBE0000880). If one or both of these registers shows an error, match the register contents with the data pattern and perform the action indicated.

Table 5-8 CAP Error Register Data Pattern

Data Pattern	Most Likely Cause	Action
110x x00x x000 0000 0000 0000 000x xxxx	RDSB - Uncorrectable ECC error detected on upper QW of MC bus (D127:64>)	Go to Step 2
101x x00x x000 0000 0000 0000 000x xxxx	RDSA - Uncorrectable ECC error detected on lower QW of MC bus (D63:0>)	Go to Step 2
111x x00x x000 0000 0000 0000 000x xxxx	RDS detected in both QWs	Go t to Step 2
1001 1000 x000 0000 0000 0000 000x xxxx	CRDB - Correctable ECC error detected on upper QW of MC bus (D127:64>)	Go to Step 2
1000 0000 x000 0000 0000 0000 000x xxxx	CRDA - Correctable ECC error detected on lower QW of MC bus (D63:0>)	Go to Step 2
1001 1000 x000 0000 0000 0000 000x xxxx	CRD detected in both QWs.	
100x x10x x000 0000 0000 0000 000x xxxx	NXM - Nonexistent MC bus address	Go to Step 3
100x x01x x000 0000 0000 0000 000x xxxx	MC_ADR_PERR - MC bus address parity error	Go to Step 4
100x x00x 1000 0000 0000 0000 000x xxxx	PIO_OVFL - PIO buffer overflow	Go to Step 5
0000 0000 0000 0000 0000 0000 0001 1xxx	PTE_INV - Page table entry is invalid	Go to Step 6
0000 0000 0000 0000 0000 0000 0001 x1xx	MAB - Master abort	Go to Step 7
0000 0000 0000 0000 0000 0000 0001 xx1x	SERR - PCI system error	Go to Step 8
0000 0000 0000 0000 0000 0000 0001 xxx1	PERR - PCI parity error	Go to Step 9

System Bus ECC Error

Step 2

Read the MC_ERR1 register and match the contents with the data pattern. Perform the action indicated.

Table 5-9 System Bus ECC Error Data Pattern

MC_ERR1 Data Pattern	Most Likely Cause	Action
For Memory Read		
1000 0000 0000 xxxx xxxx 10xx 0xxx xxxx	Bad nondirty data from memory (bad memory)	Go to Step 10
1000 0000 0000 xxxx xxxx 111x 0xxx xxxx	Bad nondirty data from memory (bad memory)	Go to Step 10
1000 0000 0001 xxxx xxxx 10xx 0xxx xxx	Bad dirty data from a CPU	Replace CPU(s)
1000 0000 0001 xxxx xxxx 111x 0xxx xxxx	Bad dirty data from a CPU	Replace CPU(s)
For Memory or I/O Write		
1000 0000 000x xxx0 10xx 011x xxxx xxxx	Bad data from MID = 2	Replace CPU0
1000 0000 000x xxx0 11xx 011x xxxx xxxx	Bad data from MID = 3	Replace CPU1
1000 0000 000x xxx1 00xx 011x xxxx xxxx	Bad data from MID = 4	Replace IOD0
1000 0000 000x xxx1 01xx 011x xxxx xxxx	Bad data from MID = 5	Replace IOD0
1000 0000 000x xxx1 10xx 011x xxxx xxxx	Bad data from MID = 6	Replace CPU2
1000 0000 000x xxx1 11xx 011x xxxx xxxx	Bad data from MID = 7	Replace CPU3
For Memory Fill Transactions		
1000 0000 000x xxx1 00xx 110x xxxx xxxx	Bad data from MID = 4	Replace IOD0
1000 0000 000x xxx1 01xx 110x xxxx xxxx	Bad data from MID = 5	Replace IOD0

NOTE: IOD0 = B3040-AA bridge module

System Bus Nonexistent Address Error

Step 3

Determine which node (if any) should have responded to the command/address identified in MC_ERR1. Perform the action indicated.

Table 5-10 System Bus Nonexistent Address Error Troubleshooting

MC_ERR1 Data Pattern	Most Likely Cause	Action
1000 0000 000x xxxx xxxx xxxx 0xxx xxxx	Software generated an MC ADDR > TOP_OF_MEM reg	Fix software
1000 0000 0000 xxxx xxxx xxxx 1xxx 100x	PCI0 bridge did not respond	Replace IOD0
1000 0000 0000 xxxx xxxx xxxx 1xxx 101x	PCI1 bridge did not respond	Replace IOD0

NOTE: IOD0 = B3040-AA bridge module

System Bus Address Parity Error

Step 4

Determine which node put the bad command/address on the system bus identified in MC_ERR1. Perform the action indicated.

Table 5-11 Address Parity Error Troubleshooting

MC_ERR1 Data Pattern	Most Likely Cause	Action
1000 0000 000x xxx0 10xx xxxx xxxx xxxx	Data sourced by MID = 2	Replace CPU0
1000 0000 000x xxx0 11xx xxxx xxxx xxxx	Data sourced by MID = 3	Replace CPU1
1000 0000 000x xxx1 00xx xxxx xxxx xxxx	Data sourced by MID = 4	Replace IOD0
1000 0000 000x xxx1 01xx xxxx xxxx xxxx	Data sourced by MID = 5	Replace IOD0
1000 0000 000x xxx1 10xx xxxx xxxx xxxx	Data sourced by MID = 6	Replace CPU2
1000 0000 000x xxx1 11xx xxxx xxxx xxxx	Data sourced by MID = 7	Replace CPU3

NOTE: IOD0 = B3040-AA bridge module

PIO Buffer Overflow Error (PIO_OVFL)

Step 5

Enter the value of the CAP_CTRL register bits<19:16> (Actual_PEND_NUM) in the following formula. Compare the results as indicated in Table 5-12 to determine the most likely cause of the error. When an IOD is implicated in the analysis of the error, replace the one that captured the error in its CAP Error Register.

Expected_PEND_NUM = 12 - ((2 * (X - 1)) + Y)

Where: X = Number of PCIs

Y = Number of CPUs

Table 5-12 Cause of PIO_OVFL Error

Comparison	Most Likely Cause	Action
Actual_PEND_NUM = Expected_PEND_NUM	Broken hardware on IOD	Replace IOD
Actual_PEND_NUM < Expected_PEND_NUM	Broken hardware on IOD	Replace IOD
Actual_PEND_NUM > Expected_PEND_NUM	PEND_NUM setup incorrect	Fix the software

NOTE: IOD0 = B3040-AA bridge module

Page Table Entry Invalid Error

Step 6

This error is almost always a software problem. However, if the software is known to be good and the hardware is suspected, swap the IOD.

PCI Master Abort

Step 7

Master aborts normally occur when the operating system is sizing the PCI bus. However, if the master abort occurs after the system is booted, read PCI_ERR1 and determine which PCI device should have responded to this PCI address. Replace this device.

PCI System Error

Step 8

For this error to occur a PCI device asserted SERR. Read the error registers in all the PCI devices to determine which device. The PCI device that set SERR should have information logged in its error registers that should indicate a device.

PCI Parity Error

Step 9

Read PCI_ERR1 and determine which PCI device normally uses that PCI address space. Replace that device. Also, read the error registers in all the PCI devices to determine which device was driving the PCI bus when the parity error occurred.

Broken Memory

Step 10

Refer to the following sections.

For a Read Data Substitute Error (Non-Correctable ECC Error)

When a read data substitute (RDS) error occurs, determine which memory module pair caused the error as follows:

1. Run the memory diagnostic to see if it catches the bad memory. If so, replace the memory module that it reports as bad.
2. Do either of the following:

- At the SRM console prompt, enter the **show mem** command.

  ```
  P00>>> show mem
  ```

  This command displays the base address and size of the memory module pair for each slot.

- Read the configuration packet, found in the error log, to retrieve the base address and size of the memory module pair.

3. Compare this address to the failing address from the MC_ERR1 and MC_ERR0 Registers to determine which memory slot is failing.
4. Replace both memory modules (high and low) for that slot. For an RDS error, there is no way to know which memory module (high or low) is bad.

For a Corrected Read Data Error (CRD)

When a CRD error occurs, determine which memory module pair caused the error as follows:

1. At the SRM console prompt, enter the **show mem** command. This command displays the base address and size of the memory module pair for each slot.

   ```
   P00>>> show mem
   ```

2. Compare this address to the failing address from the MC_ERR1 and MC_ERR0 Registers to determine which memory slot is failing.

3. When you have isolated the failing memory pair, determine which of the two modules is bad. (You cannot do this if the operating system is Windows NT.) Read the CPU FIL SYNDROME Register. If this register is non-zero, use the ECC syndrome bits in Table 5-13 to determine which module had the single-bit error.

Table 5-13 ECC Syndrome Bits Table

MDP Syndrome Values for Low-Order Memory								
01	02	04	08	10	20	40	80	CE
CB	D3	D5	D6	D9	DA	DC	23	25
26	29	2C	31	13	19	4F	4A	52
54	57	58	5B	5D	A2	A4	A8	B0
MDP Syndrome Values for High-Order Memory								
2A	34	0E	0B	15	16	1A	1C	E3
E5	E6	E9	EA	EC	F1	F4	A7	AB
AD	B5	8F	8A	92	94	97	98	9B
9D	62	64	67	68	6B	6D	70	75

Command Codes

Table 5-14 shows the codes for transactions on the system bus and how they are affected by the commander in charge of the bus during the transaction. The command is a six-bit field in the command address (bits<5:0>). Bit-to-text translations give six-bit data (although the top two bits may or may not be relevant). Note that address bit<39> defines the command as being either a system space or an I/O command.

Table 5-14 Decoding Commands

5 4	MC_CMD 3 2 1 0	CMD in Hex	MC_ADR <39>	Description	No B-Cache CPU	B-Cache CPU	IOD
x x	0 0 0 0	X 0	1	Mem Idle		Y	Y
0 0	0 0 1 0	0 2	1	Write Pend Ack			Y
x x	0 0 1 1	X 3	1	Mem Refresh			
x x	0 1 0 1	X 4	0	Set Dirty		Y	
x 0	0 1 1 0	0/2 6	0	Write Thru - Mem	Y	Y	
x 0	0 1 1 0	0/2 6	1	Write Thru - I/O	Y	Y	
x 1	0 1 1 0	3/1 6	0	Write Back - Mem	Y	Y	
x 1	0 1 1 0	3/1 6	1	Write Intr - I/O			Y
0 0	0 1 1 1	0 7	0	Write Full - Mem			Y
1 0	0 1 1 1	2 7	0	Write Part - Mem (B-cache CPU only)			Y
x 0	0 1 1 1	0/2 7	1	Write Mask - I/O			Y

Continued

Table 5-14 Decoding Commands (continued)

5 4	MC_CMD 3 2 1 0	CMD in Hex	MC_ADR <39>	Description	No B-Cache CPU	B-Cache CPU	IOD
x 0	0 1 1 1	0/2 7	0	Write Merge - Mem			Y
x x	1 0 0 0	X 8	0	Read0 - Mem	Y	Y	Y
x x	1 0 0 0	X 8	1	Read0 - I/O	Y	Y	
x x	1 0 0 1	X 9	0	Read1 - Mem	Y	Y	Y
x x	1 0 0 1	X 9	1	Read1 - I/O	Y	Y	
x x	1 0 1 0	X A	0	Read Mod0 - Mem	Y	Y	Y
x x	1 0 1 0	X A	1	Read Peer0 - I/O			Y
x x	1 0 1 1	X B	0	Read Mod1 - Mem	Y	Y	Y
x x	1 0 1 1	X B	1	Read Peer1 - I/O			Y
1 0	1 1 0 0	2 C	1	Fill0 (due to Read0/Peer0)			Y
1 0	1 1 0 1	2 D	1	FILL1 (due to Read1/Peer1)			Y
x x	1 1 1 0	X E	0	Read0 - Mem	Y	Y	
x x	1 1 1 1	X F	0	Read1 - Mem	Y	Y	

Node IDs

The node ID is a six-bit field in the command address (bits<38:33>). The high-order three bits are always set, and the last three indicate the node. Bit-to-text translations give six-bit data, although only the last three bits define the node.

Table 5-15 Node IDs

Node ID <2:0>	Six Bit (Hex)	Node
0 0 0	38	
0 0 1	39	Memory
0 1 0	3A	CPU0
0 1 1	3B	CPU1
1 0 0	3C	IOD0
1 0 1	3D	IOD1
1 1 0	3E	CPU2
1 1 1	3F	CPU3

Double Error Halts and Machine Checks While in PAL Mode

Two error cases require special attention: double error halts and machine checks while the machine is in PAL mode. Information is available that can help determine what error occurred.

PALcode Overview

PALcode, privileged architecture library code, is used to implement a number of functions at the machine level without the use of microcode. This allows the operating system to make common calls to PALcode routines without knowing the hardware specifics of each system the operating system is running on. PALcode routines handle the following:

- Instructions that require complex sequencing, such as atomic operations
- Instructions that require VAX-style interlocked memory access
- Privileged instructions
- Memory management
- Context swapping
- Interrupt and exception dispatching
- Power-up initialization and booting
- Console functions
- Emulation of instructions with no hardware support

Double Error Halt

A double error halt occurs under the following conditions:

- A machine check occurs.
- PAL completes its tasks and returns control of the system to the operating system.
- A second machine check occurs before the operating system completes its tasks.

The machine returns to the console and displays the following message:

```
halt code = 6

double error halt

C  =  20000004

Your system has halted due to an irrecoverable  error.  Record the
error  halt code and PC and contact your Digital Services
representative.  In addition, type INFO 5 and INFO 8 at the console
and record the results.
```

The **info 5** command (Example 5-2) causes the SRM console to read the PAL-built logout area that contains all the data used by the operating system to create the error entry.

The **info 8** command (Example 5-3) causes the SRM console to read the IOD 0 and IOD 1 registers.

Machine Checks While in PAL

If a machine check occurs while the system is running PALcode, PALcode returns to the SRM console, not to the operating system. The SRM console writes the following message:

```
halt code = 7

machine check while in PAL mode

PC  =  20000004

Your system has halted due to an irrecoverable  error.  Record the
error halt code and PC and contact your Digital Services
representative.  In addition, type INFO 3 and INFO 8 at the console
and   record the results.
```

The **info 3** command (Example 5-1) causes the SRM console to read the "impure area," which contains the state of the CPU before it entered PAL.

Example 5-1 INFO 3 Command

```
P00>>> info 3
                        cpu00


per_cpu impure area  00004400
cns$flag             00000001 : 0000
cns$flag+4           00000000 : 0004
cns$hlt              00000000 : 0008
cns$hlt+4            00000000 : 000c
cns$mchkflag         00000228 : 0210
cns$mchkflag+4       00000000 : 0214
cns$exc_addr         20000004 : 0318
cns$exc_addr+4       00000000 : 031c
cns$pal_base         00000000 : 0320
cns$pal_base+4       00000000 : 0324
cns$mm_stat          0000da10 : 0338
cns$mm_stat+4        00000000 : 033c
cns$va               00080000 : 0340
cns$va+4             00000002 : 0344
cns$icsr             40000000 : 0348
cns$icsr+4           000000c1 : 034c
cns$ipl              0000001f : 0350
cns$ipl+4            00000000 : 0354
cns$ps               00000000 : 0358
cns$ps+4             00000000 : 035c
cns$itb_asn          00000000 : 0360
cns$itb_asn+4        00000000 : 0364
cns$aster            00000000 : 0368
cns$aster+4          00000000 : 036c
```

```
cns$astrr             00000000 : 0370
cns$astrr+4           00000000 : 0374
cns$isr               00400000 : 0378
cns$isr+4             00000000 : 037c
cns$ivptbr            00000000 : 0380
cns$ivptbr+4          00000002 : 0384
cns$mcsr              00000000 : 0388
cns$mcsr+4            00000000 : 038c
cns$dc_mode           00000001 : 0390
cns$dc_mode+4         00000000 : 0394
cns$maf_mode          00000080 : 0398
cns$maf_mode+4        00000000 : 039c
cns$sirr              00000000 : 03a0
cns$sirr+4            00000000 : 03a4
cns$fpcsr             00000000 : 03a8
cns$fpcsr+4           ff900000 : 03ac
cns$icperr_stat       00000000 : 03b0
cns$icperr_stat+4     00000000 : 03b4
cns$pmctr             00000000 : 03b8
cns$pmctr+4           00000000 : 03bc
cns$exc_sum           00000000 : 03c0
cns$exc_sum+4         00000000 : 03c4
cns$exc_mask          00000000 : 03c8
cns$exc_mask+4        00000000 : 03cc
cns$intid             00000016 : 03d0
cns$intid+4           00000000 : 03d4
cns$dcperr_stat       00000000 : 03d8
cns$dcperr_stat+4     00000000 : 03dc
cns$sc_stat           00000000 : 03e0
cns$sc_stat+4         00000000 : 03e4
cns$sc_addr           000047cf : 03e8
cns$sc_addr+4         ffffff00 : 03ec
```

```
cns$sc_ctl            0000f000 : 03f0
cns$sc_ctl+4          00000000 : 03f4
cns$bc_tag_addr       ff7fefff : 03f8
cns$bc_tag_addr+4     ffffffff : 03fc
cns$ei_stat           04ffffff : 0400
cns$ei_stat+4         fffffff0 : 0404
cns$fill_syn          000000a7 : 0410
cns$fill_syn+4        00000000 : 0414
cns$ld_lock           0004eaef : 0418
cns$ld_lock+4         ffffff00 : 041c
```

Example 5-2 INFO 5 Command

```
P00>>> info 5
                          cpu00

per_cpu logout area          00004838
mchk$crd_flag                00000320 : 0000
mchk$crd_flag+4              00000000 : 0004
mchk$crd_offsets             00000118 : 0008
mchk$crd_offsets+4           00001328 : 000c
mchk$crd_mchk_code           00980000 : 0010
mchk$crd_mchk_code+4         00000000 : 0014
mchk$crd_ei_stat             eba00003 : 0018
mchk$crd_ei_stat+4           4143040a : 001c
mchk$crd_ei_addr             d1200067 : 0020
mchk$crd_ei_addr+4           47f90416 : 0024
mchk$crd_fill_syn            eba00003 : 0028
mchk$crd_fill_syn+4          d1200068 : 002c
mchk$crd_isr                 7ec38000 : 0030
mchk$crd_isr+4               63ff4000 : 0034
mchk$flag                    00000320 : 0000
mchk$flag+4                  00000000 : 0004
mchk$isr                     00000000 : 0138
mchk$isr+4                   00000000 : 013c
mchk$icsr                    60000000 : 0140
mchk$icsr+4                  000000c1 : 0144
mchk$ic_perr_stat            00000000 : 0148
mchk$ic_perr_stat+4          00000000 : 014c
mchk$dc_perr_stat            00000000 : 0150
```

```
mchk$dc_perr_stat+4             00000000 : 0154
mchk$va                         ff8000a0 : 0158
mchk$va+4                       ffffffff : 015c
mchk$mm_stat                    000149d0 : 0160
mchk$mm_stat+4                  00000000 : 0164
mchk$sc_addr                    0001904f : 0168
mchk$sc_addr+4                  ffffff00 : 016c
mchk$sc_stat                    00000000 : 0170
mchk$sc_stat+4                  00000000 : 0174
mchk$bc_tag_addr                ff7fefff : 0178
mchk$bc_tag_addr+4              ffffffff : 017c
mchk$ei_addr                    066bc3ef : 0180
mchk$ei_addr+4                  ffffff00 : 0184
mchk$fill_syn                   000000a7 : 0188
mchk$fill_syn+4                 00000000 : 018c
mchk$ei_stat                    04ffffff : 0190
mchk$ei_stat+4                  fffffff0 : 0194
mchk$ld_lock                    00005b6f : 0198
mchk$ld_lock+4                  ffffff00 : 019c

IOD: 0 base address: f9e0000000

WHOAMI:   0000003a  PCI_REV:  06008221
CAP_CTL:  02490fb1  HAE_MEM:  00000000 HAE_IO:    00000000
INT_CTL:  00000003  INT_REQ:  00800000 INT_MASK0: 00010000
INT_MASK1:00000000  MC_ERR0:  e0000000 MC_ERR1:   800e88fd
CAP_ERR:  84000000  PCI_ERR:  00000000 MDPA_STAT: 00000000
MDPA_SYN: 00000000  MDPB_STAT:00000000 MDPB_SYN:  00000000
```

```
IOD: 1 base address: fbe0000000

WHOAMI:   0000003a  PCI_REV:  06000221
CAP_CTL:  02490fb1  HAE_MEM:  00000000 HAE_IO:   00000000
INT_CTL:  00000003  INT_REQ:  00800000 INT_MASK0:00010000
INT_MASK1:00000000  MC_ERR0:  e0000000 MC_ERR1:  800e88fd
CAP_ERR:  84000000  PCI_ERR:  00000000 MDPA_STAT:00000000
MDPA_SYN: 00000000  MDPB_STAT:00000000 MDPB_SYN: 00000000
```

Example 5-3 INFO 8 Command

```
P00>>> info 8

IOD 0

WHOAMI:   0000003a PCI_REV:  06008221
CAP_CTL:  02490fb1 HAE_MEM:  00000000 HAE_IO:    00000000
INT_CTL:  00000003 INT_REQ:  00000000 INT_MASK0: 00210000
INT_MASK1:00000000 MC_ERR0:  e0000000 MC_ERR1:   000e88fd
CAP_ERR:  00000000 PCI_ERR:  00000000 MDPA_STAT: 00000000
MDPA_SYN: 00000000 MDPB_STAT:00000000 MDPB_SYN:  00000000
INT_TARG: 0000003a INT_ADR:  00006000 INT_ADR_EXT00000000
PERF_MON: 00406ebf PERF_CONT:00000000 CAP_DIAG:  00000000
DIAG_CHKA:10000000 DIAG_CHKB:10000000 SCRATCH:   21011131
W0_BASE:  00100001 W0_MASK:  00000000 T0_BASE:   00001000
W1_BASE:  00800001 W1_MASK:  00700000 T1_BASE:   00008000
W2_BASE:  8000000  W2_MASK:  3ff00000 T2_BASE:   00000000
W3_BASE:  00000000 W3_MASK:  1ff00000 T3_BASE:   0000b800
W_DAC:    00000000 SG_TBIA:  00000000 HBASE:     00000000

IOD 1

WHOAMI:   0000003a PCI_REV:  06000221
CAP_CTL:  02490fb1 HAE_MEM:  00000000 HAE_IO:    00000000
INT_CTL:  00000003 INT_REQ:  00000000 INT_MASK0: 00000000
INT_MASK1:00000000 MC_ERR0:  e0000000 MC_ERR1:   000e88fd
CAP_ERR:  00000000 PCI_ERR:  00000000 MDPA_STAT: 00000000
MDPA_SYN: 00000000 MDPB_STAT:00000000 MDPB_SYN:  00000000
```

```
INT_TARG: 0000003a INT_ADR:  00006000 INT_ADR_EXT00000000
PERF_MON: 004e31a6 PERF_CONT:00000000 CAP_DIAG:  00000000
DIAG_CHKA:10000000 DIAG_CHKB:10000000 SCRATCH:   00000000
W0_BASE:  00100001 W0_MASK:  00000000 T0_BASE:   00001000
W1_BASE:  00800001 W1_MASK:  00700000 T1_BASE:   00008000
W2_BASE:  80000001 W2_MASK:  3ff00000 T2_BASE:   00000000
W3_BASE:  00000000 W3_MASK:  1ff00000 T3_BASE:   0000a000
W_DAC:    00000000 SG_TBIA:  00000000 HBASE:     00000000
```

6

Removal and Replacement

This chapter describes removal and replacement procedures for field-replaceable units (FRUs). It covers the following topics:

- System Safety
- FRU List
- Power System FRUs
- CPU Removal and Replacement
- Memory Removal and Replacement
- Power Supply Removal and Replacement
- Floppy Removal and Replacement
- CD-ROM Removal and Replacement

System Safety

Observe the safety guidelines in this section to prevent personal injury.

CAUTION: Wear an anti-static wrist strap whenever you work on a system.

The DIGITAL Server 7300/7300R series cabinet system has a wrist strap connected to the frame at the front and rear. The pedestal system does not have an attached strap, so you will have to take one to the site.

WARNING: When the system interlocks are disabled and the system is still powered on, voltages are low in the system drawer, but current is high. Observe the following guidelines to prevent personal injury.

1. *Remove any jewelry that may conduct electricity before working on the system.*
2. *Do not insert your hands between the fan and the power supply.*
3. *If you need to access the system card cage, power down the system and wait 2 minutes to allow components in that area to cool.*

FRU List

Figure 6-1 shows the locations of FRUs in the system drawer. Table 6-1 lists the part numbers of all field-replaceable units.

Figure 6-1 System Drawer FRU Locations

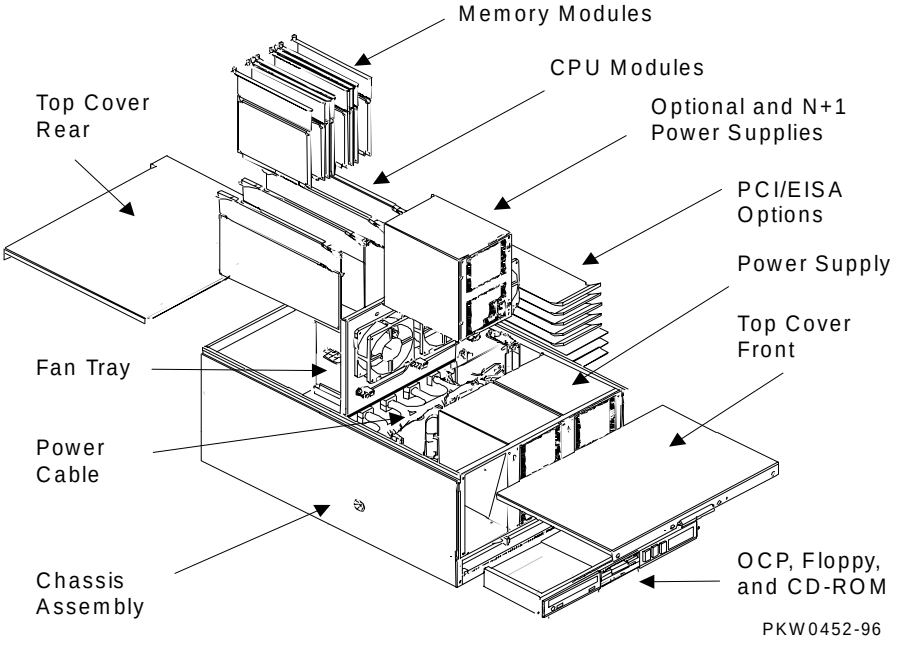


Table 6-1 Field-Replaceable Unit Part Numbers

CPU Modules	
B3105-AA	400Mhz 4MB cached
B3105-CA	533Mhz 4MB cached
Memory Modules	
B3020-CA	64 Mbyte synch
B3030-EA	256 Mbyte asynch (EDO)
B3030-FA	512 Mbyte asynch (EDO)
B3030-GA	2 Gbyte asynch (EDO)
Required System Drawer Modules and Display	
54-23803-01	System motherboard
B3040-AA	System bus to PCI bus bridge module
B3050-AA or B3052-AA	PCI motherboard
54-24117-01	Power control module
54-24364-01	OCP logic module
54-24366-01	OCP switch module
54-24674-01	Server control module
54-24691-01	Fan fail detect module (cabinet only)
30-43049-01	OCP display
70-32013-02	Pedestal door assembly (white)
70-32023-03	Pedestal assembly (white)
Fans	
12-23609-21	4.5-inch fan
12-24701-34	CPU fan

Continued

Table 6-1 Field-Replaceable Unit Part Numbers (continued)

Power System Components	
30-44712-01	Power supply (H7291-AA)
30-46788-01	Internal power source 40W/12V fan tray power (cabinet)
H7600-AA	Power controller (NA/Japan, H9A10-EN cabinet)
H7600-DB	Power controller (Europe/AP, H9A10-EP cabinet)
12-23501-01	NEMA power strip (N.A./Japan, pedestal)
12-45334-02	IEC power strip (Europe/AP, pedestal, and all cabinet systems)
Internal Power Cords	
17-04285-01	.5 meter IEC to IEC
17-00606-02	6 foot NEMA to IEC (N.A./Japan, pedestal)
17-04285-02	2 meter IEC to IEC (Europe/AP, pedestal, and all cabinet systems.)
17-04285-03	IEC to IEC StorageWorks shelf
Fan Tray Cables (Cabinet Only)	
17-04324-01	Electric fan power harness
17-04325-01	12V power for SCM
17-04338-01	Power ground cable
17-04339-01	AC cable power
Server Control Module Power (Pedestal Only)	
30-46485-01	110V North America
30-46485-02	220V Europe
30-46485-03	Australia/N.Z.
30-46485-04	220V U.K.

Continued

Table 6-1 Field-Replaceable Unit Part Numbers (continued)

System Drawer Cables and Jumpers		From	To
17-04196-01	Server control module signal cable (60 pin)	Remote I/O signal conn on PCI mbrd	SCM signal conn
17-04199-01	Current share cable	Current share conn on PS0	Current share conn on PS1 and PS2
17-04200-01	Floppy signal cable (36 pin)	Floppy conn on PCI mbrd	Floppy
17-04201-01	OCP signal	OCP conn on PCI mbrd	OCP signal (system drawer only)
17-04201-02	OCP signal jumper	OCP	OCP
17-04217-01	Power harness	Power supply(s)	7 conns. sys mbrd sys fans 0, 1 5V conn on PCI mbrd CD-ROM drv pwr Floppy pwr 1 OCP DC enable pwr conn or pwr conn on ped tray pwr drive cable (17-04293-01)

Continued

Table 6-1 Field-Replaceable Unit Part Numbers (continued)

System Drawer Cables and Jumpers		From	To
17-04292-01	SCSI CD-ROM sig cable	CD-ROM conn on PCI mbrd	CD-ROM sig conn
70-32016-01	Interlock switches and cable	Interlock switch assy	Other OCP DC enable pwr conn or pwr conn on ped tray pwr drive cable (17-04293-01)
17-04349-01	SCM 12V interlock jumper	Interlock conn on PCI mbrd	12 V DC enable conn on SCM
17-04350-01	SCM 34-position jumper	SCM	SCM
17-04351-01	SCM 12V power jumper	Power harness (17-04217-01)	Sys fan 2 and SCM internal 12V conn
17-04363-01	SCM 16-position jumper	SCM sig conn on PCI mbrd	16 pos conn on SCM

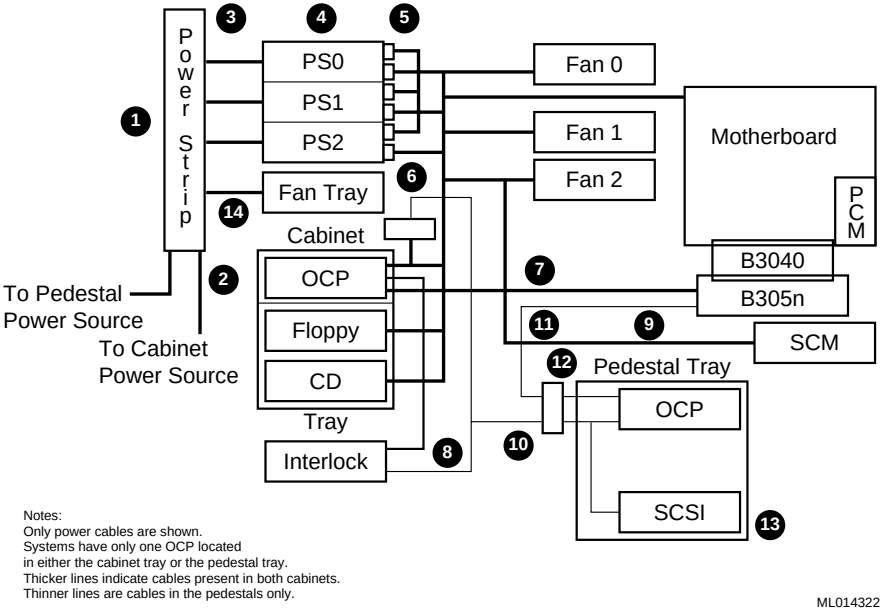
Continued

Table 6-1 Field-Replaceable Unit Part Numbers (continued)

Pedestal Cables		From	To
17-04293-01	Elec harness power cable+5/+12	Power harness (17-04217-01)	Ped tray bulkhead (system side)
17-04302-01	OCP signal cable	OCP sig conn on PCI mbrd	OCP sig conn on ped tray bulkhead (system side)
17-04305-01	Harness power cable +5/+12	Power conn on ped tray bulkhd (tray side)	Both OCP DC enable pwr conn and pwr conn on optional SCSI drive
17-04306-01	SCSI signal cable (narrow)	SCSI sig conn on ped tray bulkhd (tray side)	Optional SCSI drive
17-04380-01	OCP signal cable	OCP sig conn on ped tray bulkhd	OCP sig conn

Power System FRUs

Figure 6-2 Location of Power System FRUs



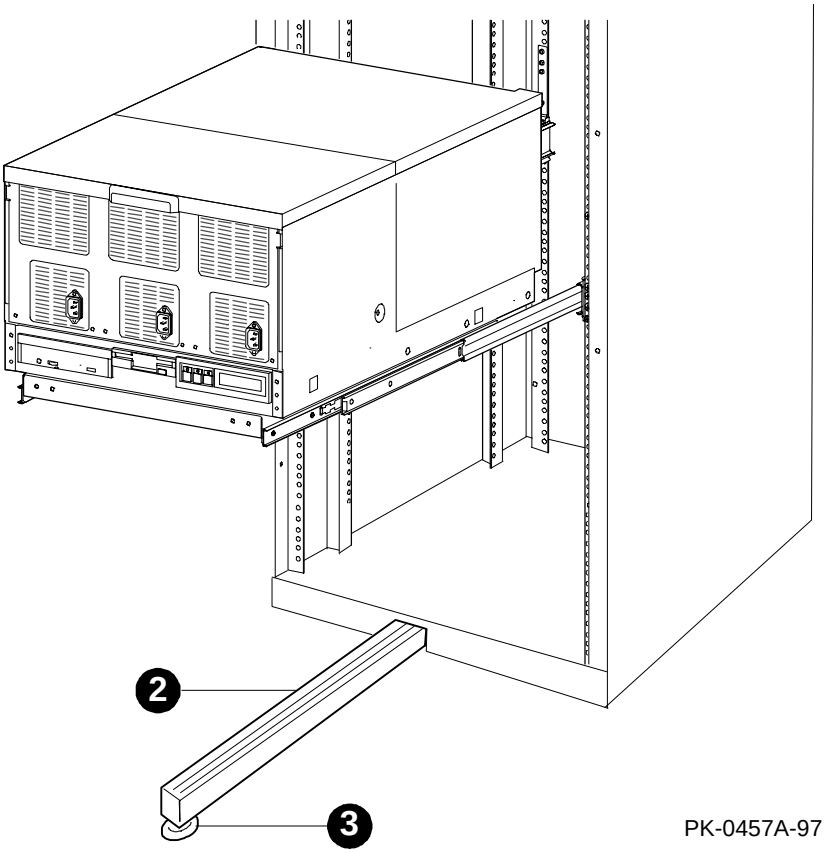
	Part Number	Description
1	12-23501-01 12-45334-02	AC power strip: The 12-23501-01 is used on pedestals in N. Amer./Japan only and has six NEMA outlets and a 15 ft. cord to the wall outlet; the 12-45334-02 is used on pedestals in Eur./AP and on cabinet systems worldwide and has six IEC320 outlets. In pedestal systems, cords match country-specific wall outlets.

	Part Number	Description
2	17-04285-01	Power cord to power strip. .5 meter, IEC320 to IEC320 connector used in cabinet systems only. In pedestal systems, cords match country-specific wall outlets.
1, 2	H7600-AA	Power controller used in place of 12-45334-02 and 17-04285-02 in the H9A10-EN cabinet in N. America/Japan.
1, 2	H7600-DB	Power controller used in place of 12-45334-02, and 17-04285-02 in the H9A10-EP cabinet in Europe/AP,
3	17-00606-02 17-04285-02	Power cord from power strip to power supply: The 17-00606-02 is a 2 m NEMA to IEC320 AC jumper used with the 12-23501-01 power strip in N. Amer./Japan pedestals. The 17-04285-02 is a 2 m IEC320 to IEC320 AC jumper used with the 12-45334-02 power strip used on pedestals in Eur./APA and on cabinet systems worldwide and has six IEC320 outlets. In pedestal systems, cords match country-specific wall outlets.
4	30-44712-01	Power supply; 92 to 264 VAC input; one to three in a system drawer.
5	17-04199-01	Cable connecting power supplies
6	17-04217-01	Power distribution harness
7	17-04201-01	Cable from OCP to PCI motherboard (cabinet system). Note that "B305n" stands for either the B3050-AA or B3052-AA PCI motherboard.
8	70-32016-01	Interlock switches and cable to OCP
9	17-04351-01	Power from power harness between harness and Fan 2 to SCM
10	17-04293-01	Cable from power harness to interconnect cable and pedestal tray connector (pedestal system)
11	17-04302-01	Cable from pedestal tray connector to PCI motherboard (pedestal system)
12	17-04201-01	Cable from pedestal tray connector to OCP (pedestal system)
13	17-04305-01	Cable from pedestal tray connector to OCP and SCSI devices (pedestal system)
14	17-04339-01	Power cord from power strip to cabinet fan tray (cabinet only)

System Drawer Exposure (Cabinet)

There is one type of cabinet for these systems: the H9A10-EN/-EP cabinet. In the H9A10-EN and -EP Cabinet, the system drawer sits on a tray that slides out of the front of the cabinet. You must pull the stabilizer bar out from the bottom to prevent the cabinet from tipping over.

Figure 6-3 Exposing System Drawer (H9A10-EN & -EP Cabinet)



Removal and Replacement

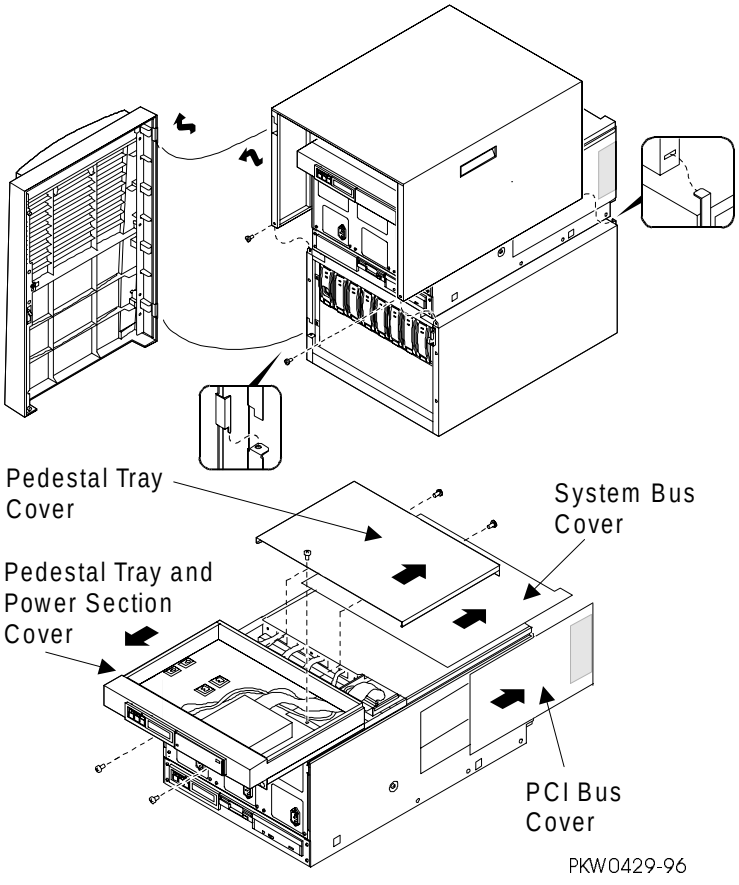
CAUTION: The cabinet could tip over if a system drawer is pulled out and the stabilizing bar is not fully extended and its leveler foot on the floor.

Exposing Any Section of the System Drawer in an H9A10-EN or -EP Cabinet.

1. Open the front door of the cabinet.
2. Pull the stabilizer bar at the bottom of the cabinet out until it stops. See ❷ in Figure 6-3
3. Extend the leveler foot at the end of the stabilizer bar to the floor. See ❸ in Figure 6-3.
4. Unplug the drawer's power supplies.
5. Remove the Phillips screws holding the shipping bracket to the rails so that the drawer can be pulled out.
6. Pull the drawer all the way out until it locks
7. To access the system bus card cage cover, unscrew the two Phillips head screws holding the cover in place and slide it off.
8. To access the PCI/EISA bus card cage, unscrew the three Phillips head screws holding the cover to the right side of the drawer and slide it off.
9. To access the PCI bus card cage, unscrew the three Phillips head screws holding the cover to the left side of the drawer and slide it off.
10. To access the power or fan section, unscrew the two Phillips head screws holding the cover in place and slide it off.

System Drawer Exposure (Pedestal)

Figure 6-4 Exposing System Drawer (Pedestal)



Exposing the System Drawer

1. Open the front door and remove it by lifting and pulling it away from the system.
2. Remove the top cover. Unscrew the two Phillips head screws midway up on each side of the pedestal, tilt the cover up, and lift it away from the frame.
3. Remove the system bus card cage cover at the back of the pedestal if you are replacing any of the following: CPU, memory, power control module, system bus to PCI bus module, system motherboard, cables that attach to the system motherboard, or a system fan. To remove the cover, unscrew the two Phillips head screws and slide the cover off the drawer.
4. Remove the PCI bus card cage cover at the back of the pedestal if you are replacing any of the following: PCI or EISA option, server control module, PCI motherboard, cables attached to the PCI motherboard. To remove the cover, unscrew the three Phillips head screws holding the cover to the side of the drawer and slide the cover off the drawer.
5. Remove the pedestal tray as described below if you are replacing any of the following: system fan, power supply, power cables.

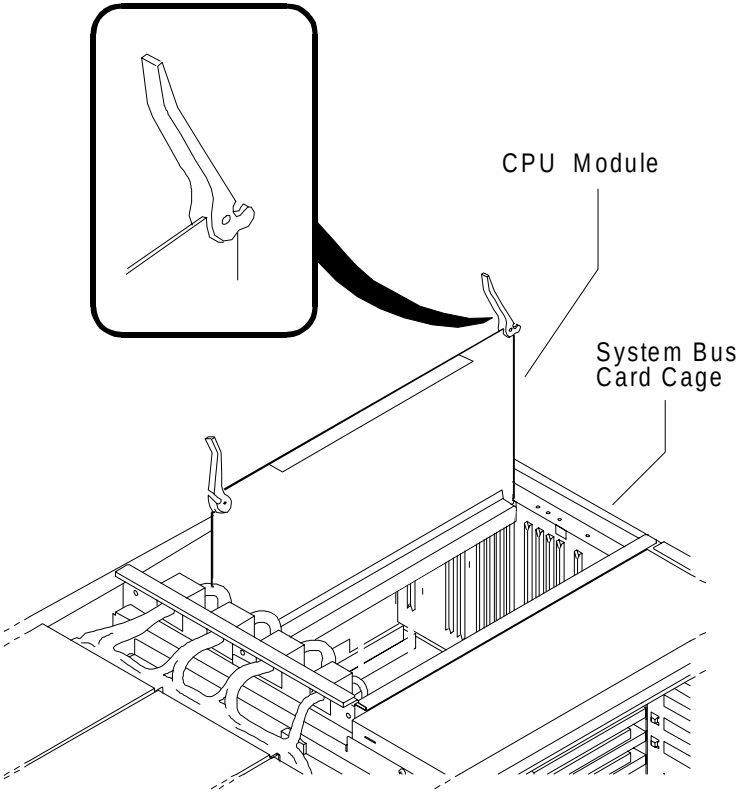
Removing the Pedestal Tray

1. Remove the tray cover by loosening the screws at the back of the tray.
2. Disconnect the cables from the OCP and any optional SCSI device from the bulkhead connector in the rear right corner of the tray.
3. Unscrew the Phillips head screw holding the bulkhead to the tray.
4. Unscrew the two Phillips head retaining screws and slide the tray off the drawer.

CPU Removal and Replacement

CAUTION: Two different CPU modules work in these systems: the B3107-AA and the B3107-CA. Unless you are upgrading, be sure you are replacing the broken module with the same variant.

Figure 6-5 Removing a CPU Module



WARNING: CPU modules have parts that operate at high temperatures. Wait two minutes after power is removed before touching any module.

Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the system bus card cage. Remove the two Phillips head screws holding the cover in place and slide it off the drawer.
4. Identify and remove faulty CPU. A label to the left of the system bus card cage identifies which slot contains CPU0, CPU1, CPU2, or CPU3. The CPU is held in place with levers at both ends; simultaneously raise the levers and lift the CPU from the cage.

Replacement

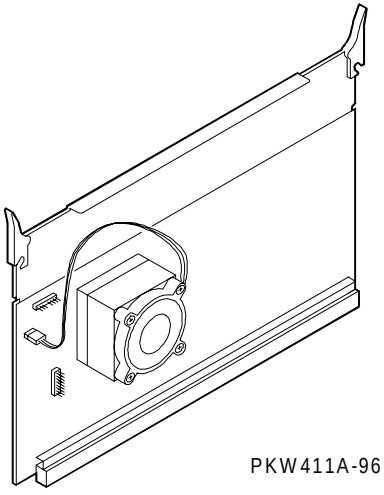
Reverse the steps in the Removal procedure.

Verification

1. Start **AlphaBIOS Setup**, select **Display System Configuration**, and press Enter.
2. Using the arrow keys, select **MC Bus Configuration** to display the status of the new module.

CPU Fan Removal and Replacement

Figure 6-6 Removing CPU Fan



Removal and Replacement

Removal

1. Follow the CPU Removal and Replacement procedure.
2. Unplug the fan from the module.
3. Remove the four Phillips head screws holding the fan to the Alpha chip’s heat sink.

Replacement

Reverse the above procedure.

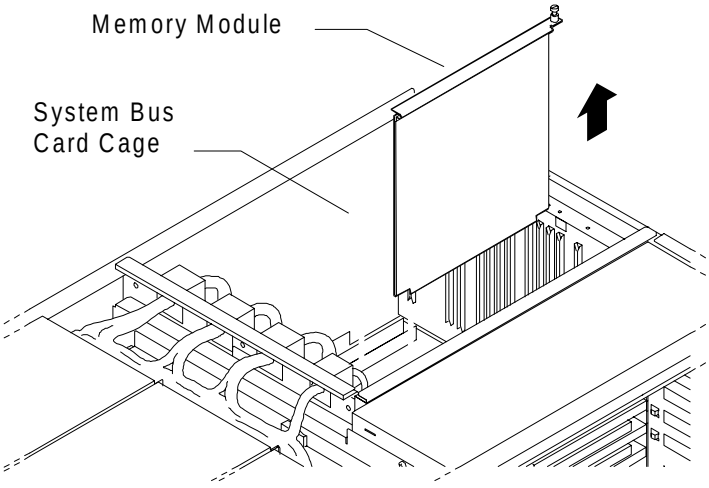
Verification

If the system powers up, the CPU fan is working.

Memory Removal and Replacement

CAUTION: Several different memory modules work in these systems. Be sure you are replacing the broken module with the same variant.

Figure 6-7 Removing a Memory Module



WARNING: Memory modules have parts that operate at high temperatures. Wait two minutes after power is removed before touching any module.

Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the system bus card cage. Remove the two Phillips head screws holding the cover in place and slide it off the drawer.
4. Identify and remove the faulty module. A label to the left of the system card cage identifies which slot contains the high or low halves of memory banks. The memory module is held in place by a flathead captive screw attached to the top brace of the module. Loosen the screw and lift the module from the cage.

Replacement

Reverse the steps in the Removal procedure.

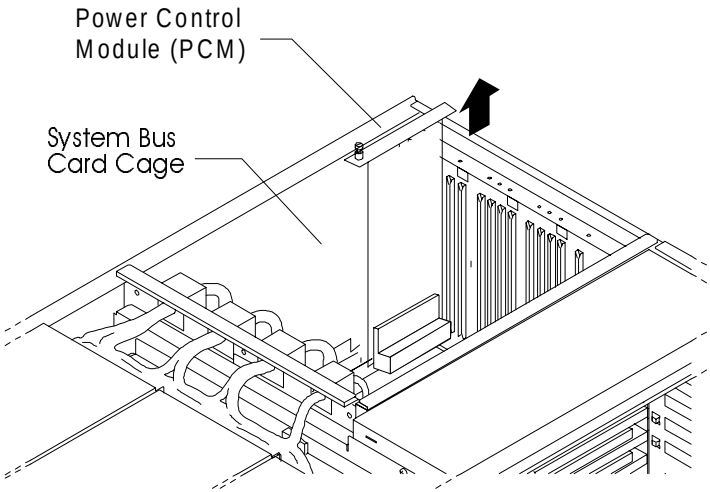
NOTE: Memory modules must be installed in pairs. When you replace a bad module, be sure the second module in the pair is in place.

Verification

1. Start **AlphaBIOS Setup**, select **Display System Configuration**, and press Enter.
2. Using the arrow keys, select **Memory Configuration** to display the status of the new memory.
3. Switch to the SRM console (press the Halt button in so that the LED on the button lights and reset the system). Verify the functioning of the new memory by issuing the command **test mem***n*, where *n* is 0, 1, 2, 3, or *.

Power Control Module Removal and Replacement

Figure 6-8 Removing Power Control Module



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the system bus card cage. Remove the two Phillips head screws holding the cover in place and slide it off the drawer.
4. Remove the faulty PCM. The PCM is located in the back left corner of the system bus card cage. A captive flathead screw and the rear card guide hold the PCM in place. Unscrew the screw and lift the module from the cage.

Replacement

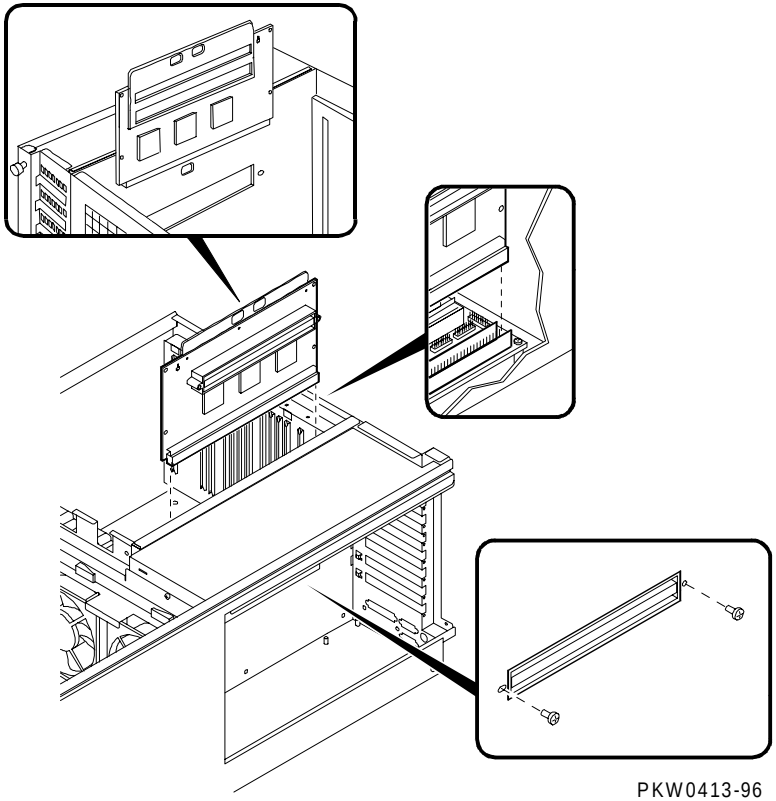
Reverse the steps in the Removal procedure.

Verification

Power up the system. If the PCM is faulty or not seated properly, the system will not come up.

System Bus to PCI Bus Bridge (B3040-AA) Module Removal and Replacement

Figure 6-9 Removing System Bus to PCI/EISA Bus Bridge Module



Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the system bus card cage. Remove the two Phillips head screws holding the cover in place and slide it off the drawer.
4. Expose the PCI bus card cage. Remove three Phillips head screws holding the cover in place and slide it off the drawer.
5. Remove all the PCI/EISA options.
6. Remove the server control module.
7. Remove the PCI motherboard.
8. Remove the two Phillips head screws holding the system bus to PCI bus bridge module to the sheet metal between the system bus card cage and the PCI bus card cage.
9. Remove enough CPU and memory modules to the right of the bridge module to allow a flathead screwdriver to be inserted in the slot in the middle of the module's top bracket.
10. Place a flathead screwdriver into the slot in the middle of the module's top bracket and into the corresponding slot in the sheet metal between the two card cages. Use the screwdriver as a lever to disconnect the bridge module from the connector on the system motherboard.
11. Remove the bridge module from the system bus card cage.

Replacement

Reverse the steps in the Removal procedure.

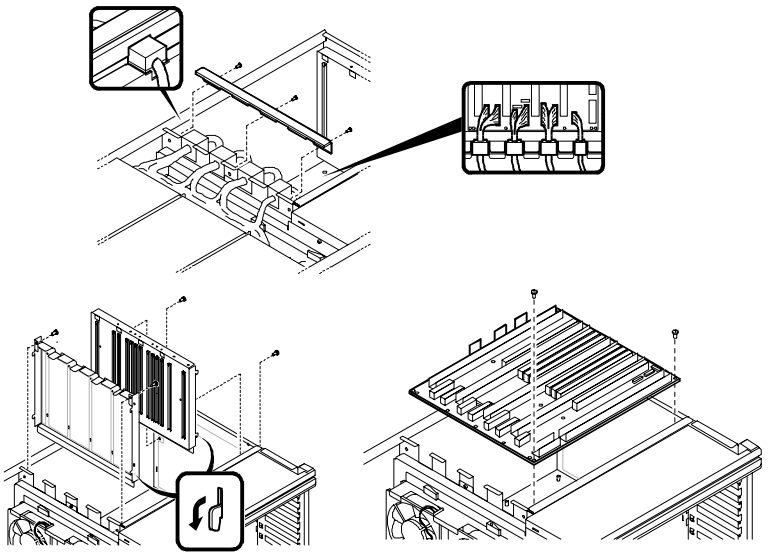
Verification

Power up the system (press the Halt button if necessary to bring up the SRM console) and issue the **show device** command at the console prompt to verify that the system sees all system options and peripherals.

System Motherboard Removal and Replacement

The system motherboard contains an NVRAM that holds the system serial number. Be sure to record this number before replacing the module. The serial number is on a bar code on the side of the system drawer or on the system bus card cage. The part number is 54-23803-01.

Figure 6-10 Removing the System Motherboard



PKW0414-96

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the system bus card cage by removing the two Phillips head screws holding it in place and sliding the cover off the drawer.
4. Remove all CPUs, memory modules, and the PCM from the system motherboard.

Removal and Replacement

5. Expose the PCI bus card cage. Remove three Phillips head screws holding the cover in place and slide it off the drawer.
6. Remove all the PCI/EISA options.
7. Remove the server control module.
8. Remove the PCI motherboard.
9. Remove system bus to PCI bus module from the system motherboard.
10. Remove the bracket holding the power cables in place as they pass from the system bus section to the power section of the drawer.
11. Disconnect all cables to the system motherboard and lay them back over the power supply section of the system drawer.

    CAUTION: Secure the power harness connectors in the system card cage to ensure that they cannot damage the pins in the CPU connectors.
12. Remove both the front and back module card guides. Unscrew the two screws that hold the guides in place.
13. Remove the system motherboard from the card cage by removing the 15 Phillips head screws holding it in place. Record the system serial number. (The serial number is on a bar code on the side of the system drawer or on the system bus card cage.)

Replacement

Reverse the above procedure. To align the motherboard in the cage, start replacing the screws in the corners next to the system bus to PCI bus bridge module and then the PCM module. Subsequent screws should align properly.

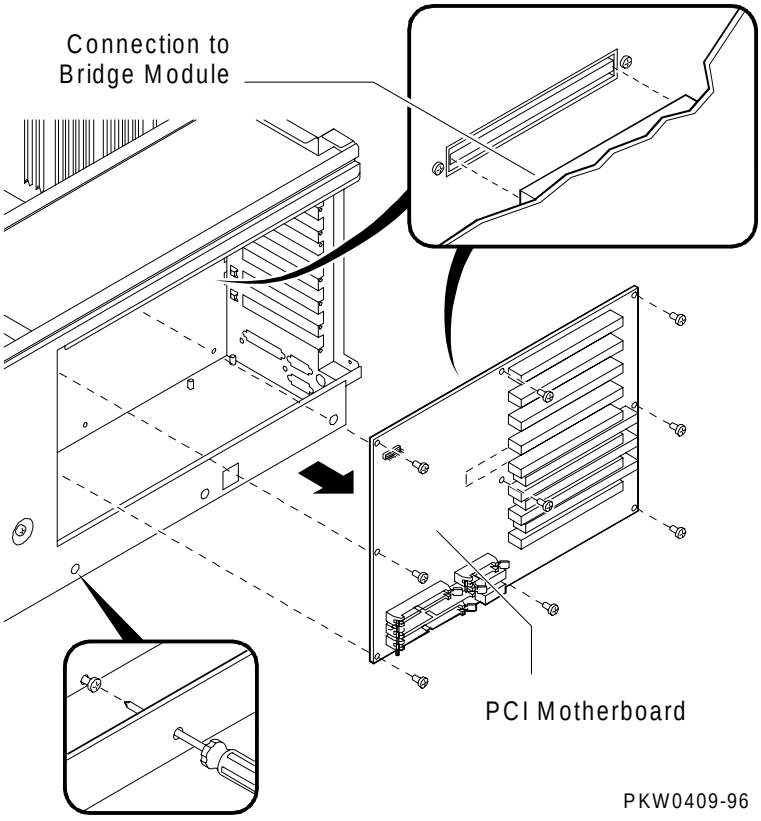
Verification

Power up the system (press the Halt button if necessary to bring up the SRM console) and issue the **show device** command at the console prompt to verify that all system options are seen.

Restore the system serial number by issuing the **set sys_serial_num** command at the SRM console prompt.

PCI/EISA Motherboard (B3050/B3052) Removal and Replacement

Figure 6-11 Replacing PCI/EISA Motherboard



Removal

The PCI motherboard contains an NVRAM with ECU data and customized console environment variables. Therefore, if the console runs, execute a **show *** command at the console prompt and, if you have not done so earlier, record the settings for the **sys_model_number** and **sys_type** environment variables. These environment variables are used to display the system model number and type, and they compute certain information passed to the operating system. When you replace the PCI motherboard, these environment variables are lost. You must restore them after the module swap.

Removal and Replacement

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the PCI bus card cage. Remove three Phillips head screws holding the cover in place and slide it off the drawer.
4. Remove all PCI and EISA options.
5. Disconnect all cables connected to the PCI motherboard.
6. Remove the server control module.
7. Unscrew the two screws holding the system bus to PCI bus bridge module in the system bus card cage to the PCI motherboard.
8. Remove the nine Phillips head screws that hold the motherboard in place. To reach the screws on the bottom of the board, thread your screwdriver through the three holes in the sheet metal.
9. Carefully pry the motherboard loose from the system bus to PCI bus bridge module on the other side of the sheet metal separating the system bus card cage from the PCI card cage.
10. Remove the motherboard from the card cage.

Replacement

Reverse the steps in the Removal procedure.

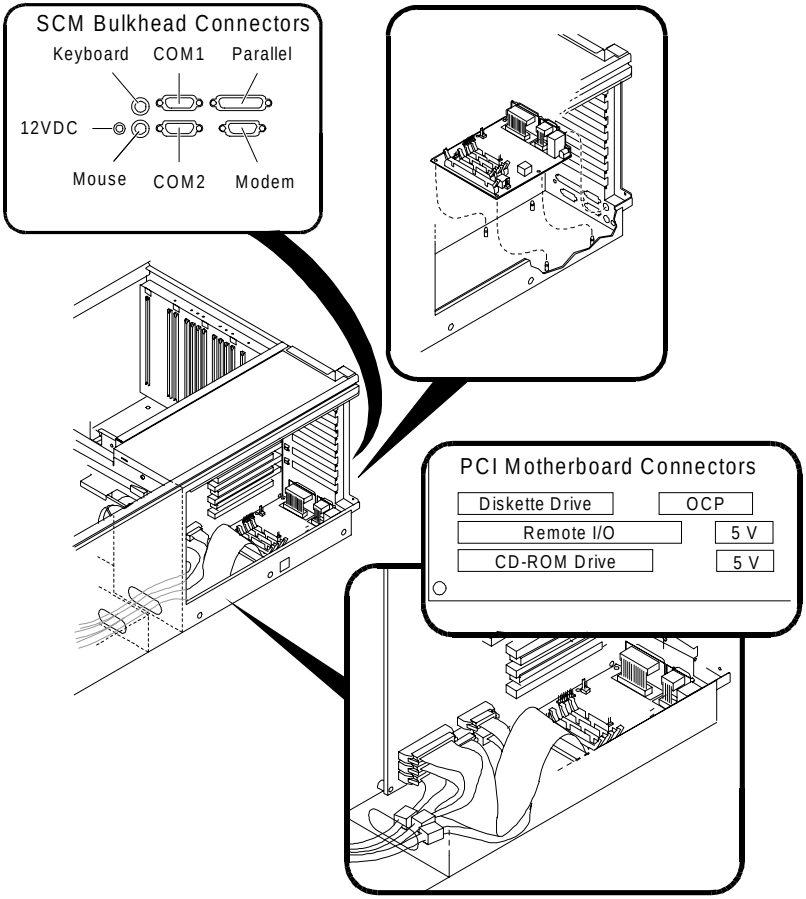
Verification

Power up the system (press the Halt button if necessary to bring up the SRM console) and issue the **show device** command at the console prompt to verify that the system sees all options.

Restore the **sys_model_num**, **sys_type,** and other customized environment variables to their previous settings. Run the ECU to restore EISA configuration data. This must be done regardless of whether there is an EISA option in the EISA slot on PCI 0.

Server Control Module Removal and Replacement

Figure 6-12 Removing Server Control Module



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the PCI bus card cage. Remove three Phillips head screws holding the cover in place and slide it off the drawer.
4. Disconnect the cables connected at the bulkhead to the server control module.
5. If necessary, remove several PCI and EISA options from the bottom of the PCI card cage up until you can access the server control module.
6. Disconnect the two cables connected to the PCI motherboard at the server control module end.
7. Disconnect the twisted pair power cable from the module.
8. Place a credit card or a piece of cardboard between the edge of the SCM module and the B3050/B3052 module to protect the delicate pins of the ASICs located in the lower right corner of the B3050/B3052 module.
9. The server control module is held in place by four stud snaps. Using a flathead screwdriver gently pry the SCM module off the snaps and remove it. *Make sure you do not hit the pins of the ASICs on the B3050/B3052.*

Replacement

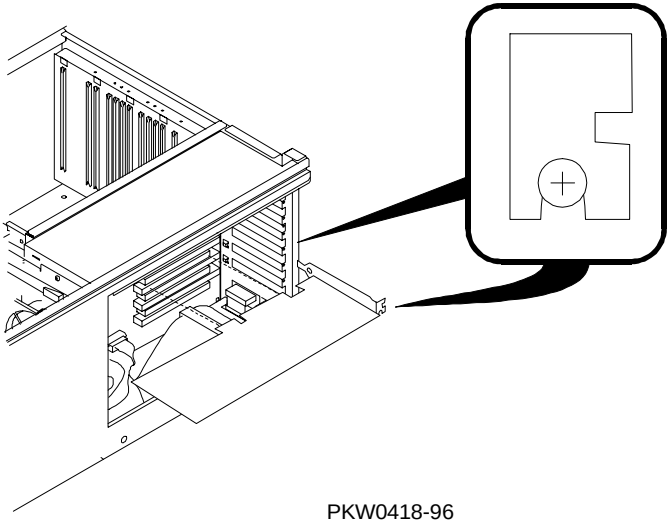
Reverse the steps in the Removal procedure.

Verification

Verify console output on COM1.

PCI/EISA Option Removal and Replacement

Figure 6-13 Removing PCI/EISA Option



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WARNING: To prevent fire, use only modules with current limited outputs. See National Electrical Code NFPA 70 or Safety of Information Technology Equipment, Including Electrical Business Equipment EN 60 950.

Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the PCI bus card cage. Remove three Phillips head screws holding the cover in place and slide it off the drawer.
4. Remove the faulty option. Disconnect cables connected to the option. Unscrew the small Phillips head screw securing the option to the card cage. Slide the option from the card cage.

Replacement

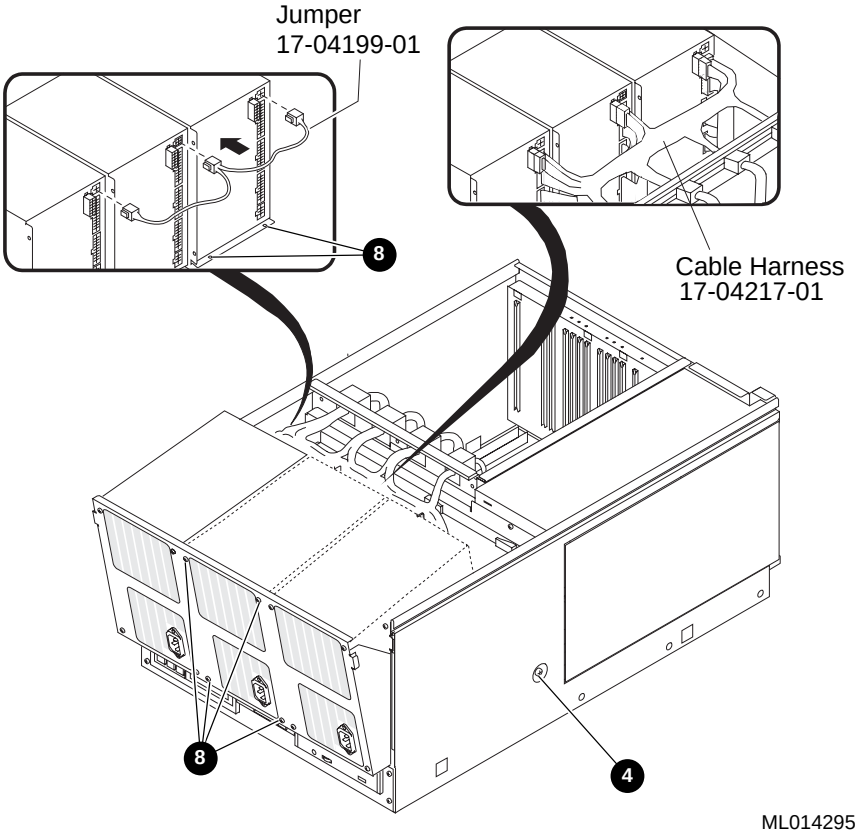
Reverse the steps in the Removal procedure..

Verification

1. Start **AlphaBIOS Setup**, select **Display System Configuration**, and press Enter.
2. Using the arrow keys, select **PCI Configuration** or **EISA Configuration** to determine that the new option is listed.

Power Supply Removal and Replacement

Figure 6-14 Removing Power Supply



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Remove the cover to the power section of the drawer. Remove the two Phillips head screws holding the cover in place and slide it off the drawer.
4. Release the power supply tray by removing the two Phillips head screws on the side of the drawer. See ❹.
5. Lift the power supply tray to release it from the sheet metal and slide it out from the drawer until it locks (about 4 inches).
6. Tilt the tray to allow easier access to the back of the power supplies.
7. Unplug the connectors at the rear of the supply that is being replaced.
8. Unscrew the four Phillips head screws at the front of the tray that hold the power supply in place. Also unscrew the two screws at the back of the power supply. See ❽.
9. Remove the power supply.

Replacement

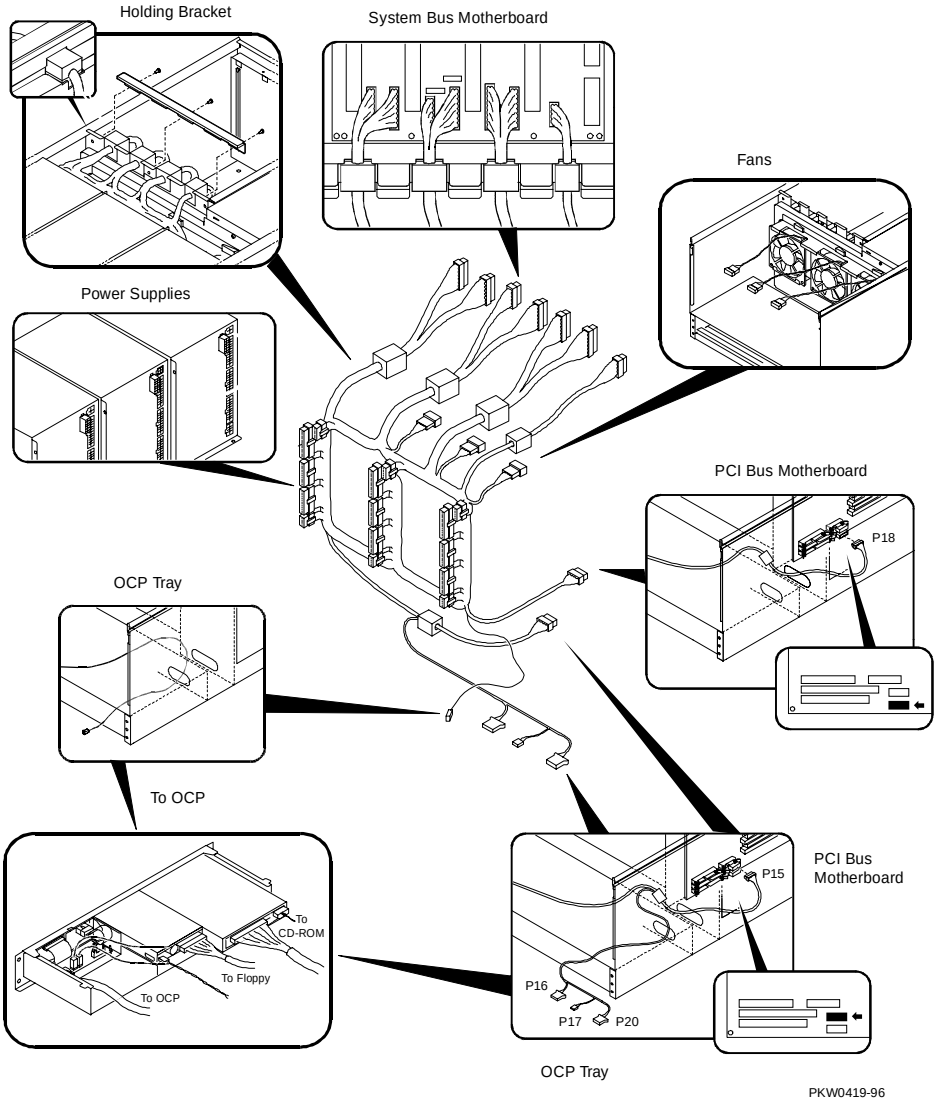
Reverse the steps in the Removal procedure.

Verification

Power up the system. If the system has redundant power, the system will power up regardless of whether the replaced power supply is faulty. In this case look at the PCM LEDs to determine that the power supply is functioning properly. If the system does not have redundant power, it will not power up.

Power Harness Removal and Replacement

Figure 6-15 Removing Power Harness



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the power, system card cage, and PCI/EISA sections of the drawer by removing all covers. Unscrew the Phillips head screws holding each cover in place and slide the covers off the drawer.
4. Release the power supply tray by removing the two Phillips head screws on the side of the drawer.
5. Lift the power supply tray to release it from the sheet metal and slide it out from the drawer until it locks.
6. Tilt the tray to allow easier access to the fans.
7. Remove the bracket holding the power harness as it passes from the power section to the system card cage section of the drawer. Remove the three Phillips head screws holding the bracket in place.
8. Disconnect the power harness from the system motherboard and fold the harness back over the power supplies.

   CAUTION: Secure the power harness connectors in the system card cage to ensure that they cannot damage the pins in the CPU connectors.

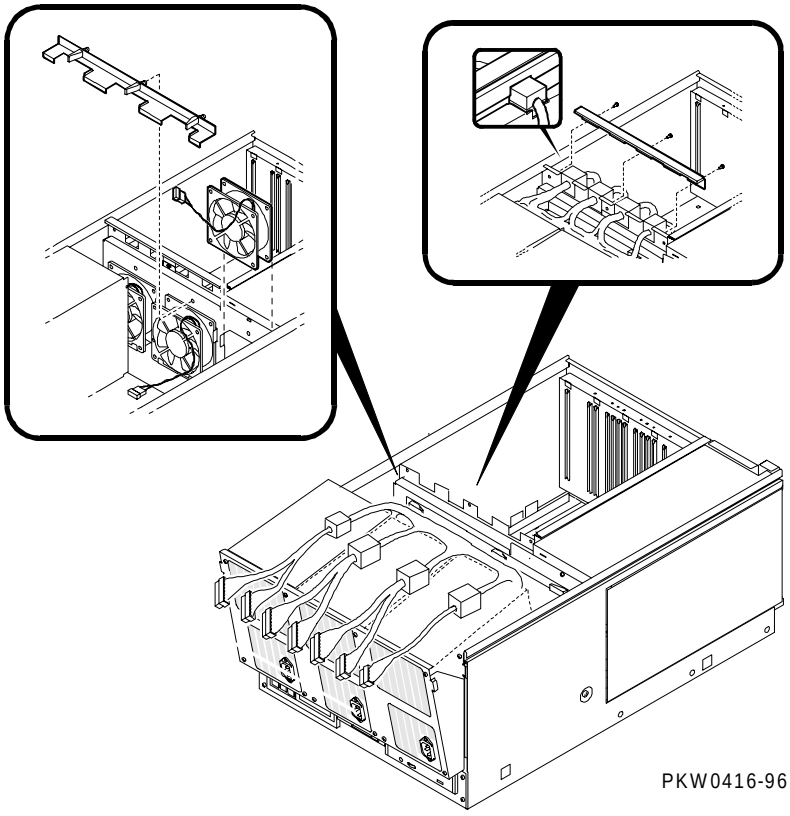
9. Disconnect the two power connectors from the PCI/ESIA motherboard. Push the power cable through the hole from the PCI/EISA section into the power section.
10. Disconnect the fan power cables from the power harness.
11. Remove the four Phillips head screws holding the OCP tray to the drawer.
12. Slide the tray from the drawer far enough to disconnect the power cables attached to the OCP (cabinet only), the floppy, and the CD-ROM.
13. As you remove the tray from the system, push the power cables through the hole at the back of the tray into the power section of the drawer.
14. Disconnect the power harness from the power supplies. Remove the harness from the system.

Replacement

Reverse the steps in the Removal procedure.

System Drawer Fan Removal and Replacement

Figure 6-16 Removing System Drawer Fan



Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Expose the power system, the system card cage, and the PCI card cage sections of the drawer by removing all three covers. Unscrew the two Phillips head screws holding each cover on top of the drawer in place and slide them off the drawer. Release the two lever latches holding the PCI card cage cover in place and slide it off.

Removal and Replacement

4. Release the power supply tray by removing the two Phillips head screws on the side of the drawer.
5. Lift the power supply tray to release it from the sheet metal and slide it out from the drawer.
6. Tilt the tray to allow easier access to the fans.
7. Remove the bracket holding the power harness as it passes from the power section to the system card cage section of the drawer. Remove the three Phillips head screws holding the bracket in place.
8. Disconnect the power harness from the system motherboard and fold the harness back over the power supplies. Remove any modules that prevent you from disconnecting the harness from the system motherboard.

   CAUTION: Secure the power harness connectors in the system card cage to ensure that they cannot damage the pins in the CPU connectors.

9. Disconnect the three power connectors from the PCI motherboard and pass them through the hole from the PCI card cage to the power section of the drawer.
10. Disconnect the fan power cables from the power harness.
11. Remove the four Phillips head screws holding the OCP tray to the system drawer. Slide the tray out of the system drawer far enough to disconnect power cables attached to the OCP, the floppy, and the CD-ROM drive.
12. Remove the tray from the system.
13. Release the three lever latches on the bracket holding all three fans in place.
14. Disconnect the broken fan's power cable from the power harness and lift the fan from the drawer.

Replacement

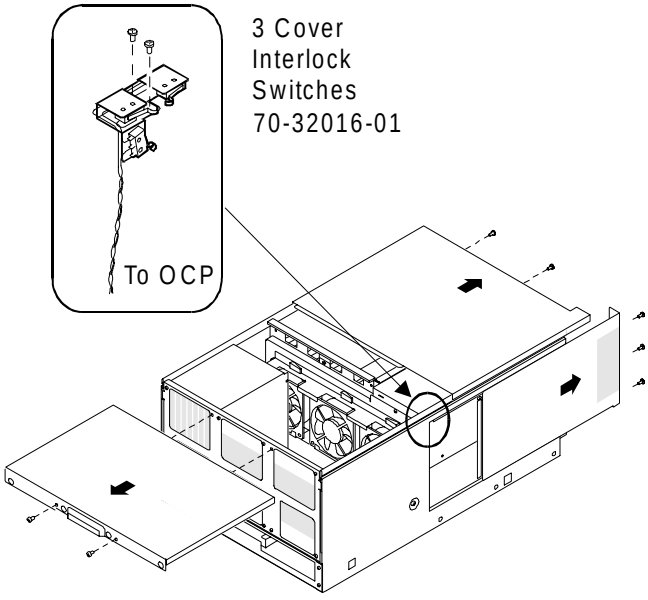
Reverse the steps in the Removal procedure.

Verification

Power up the system. If the fan you installed is faulty, the system will not power up. Look at the PCM LEDs to determine that the fan you replaced is functioning properly.

Cover Interlock Removal and Replacement

Figure 6-17 Removing Cover Interlocks



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Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Remove all three section covers to expose the interlock switch assembly.
4. Remove the two screws holding the interlock in place.
5. Push the interlock toward the opposite side of the system drawer (be sure not to twist it) and tilt it so that the switches affected by the power and system card cage covers clear the openings in the side of the drawer. Slide it toward the front of the drawer and remove it, letting it hang loosely over the side of the drawer.
6. If you are working on a pedestal system, disconnect the switch connection from the tray bulkhead and remove the interlock switch assembly.
7. If you are working on a system drawer in a cabinet, unscrew the four screws holding the OCP tray assembly in place beneath the drawer in front.
8. Slide the tray out and remove it from the system.
9. Pull the interlock switch connection to the OCP back through the access hole and remove the entire switch assembly.

Replacement

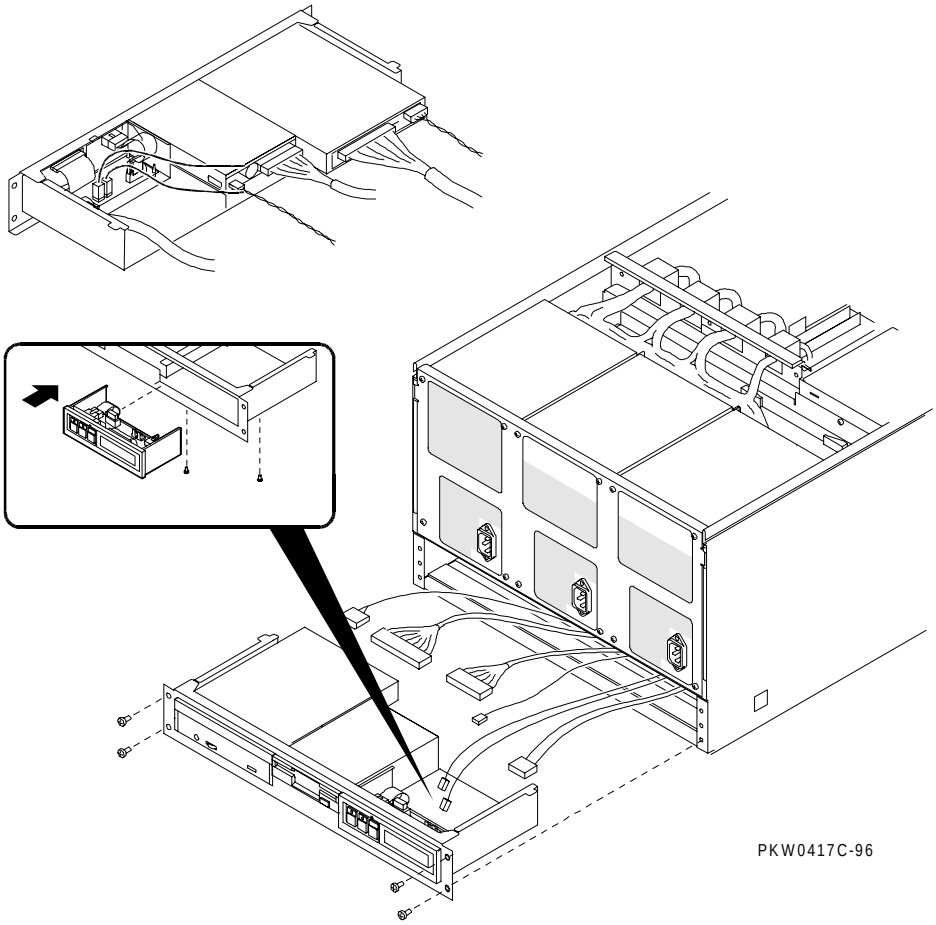
Reverse the steps in the Removal procedure.

Verification

Power up the system. If the switch you installed is faulty, the system will not power up.

Operator Control Panel Removal and Replacement (Cabinet)

Figure 6-18 Removing OCP (Cabinet)



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.

   While you need not remove the tray containing the OCP, you do need to slide it forward to access the OCP retaining screws under the tray. The tray is attached to the power system section cover. To slide the tray forward:

   Remove the tray cover by loosening the retaining screws at the back of the tray and sliding it toward the back of the system.

   Disconnect the cables from the OCP, and any optional SCSI device in the tray from the bulkhead at the rear right of the tray.

   Unscrew the Phillips head retaining screw holding the bulkhead to the tray.

   Unscrew the two Phillips head retaining screws at the front of the system drawer and slide the tray forward.
3. Remove the white power interconnect wire and the signal ribbon cable from the OCP.
4. Remove the two Phillips head screws holding the OCP in place and remove it from the tray.

Replacement

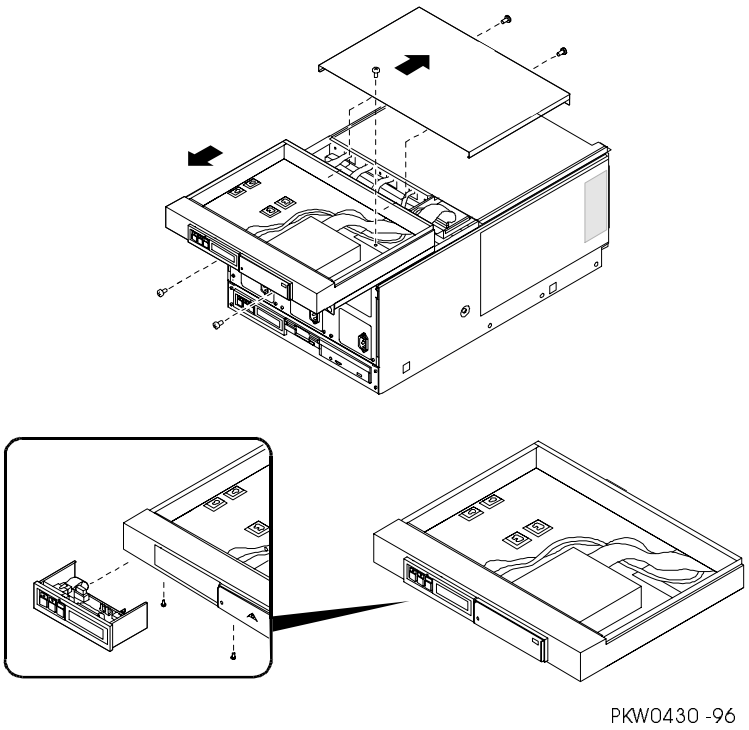
Reverse the steps in the Removal procedure.

Verification

Power up the system. If the OCP you installed is faulty, the system will not power up.

Operator Control Panel Removal and Replacement (Pedestal)

Figure 6-19 Removing OCP (Pedestal)



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Remove the four Phillips head screws holding the OCP tray to the system drawer.
4. Slide the tray out of the system drawer far enough to disconnect cables attached to the OCP, the floppy, and the CD-ROM drive.
5. Remove the tray from the system.
6. Move the tray to some handy work surface. Hold the tray vertically and remove the two Phillips head screws that hold the OCP in place from the bottom of the tray and remove the OCP assembly from the tray.

Replacement

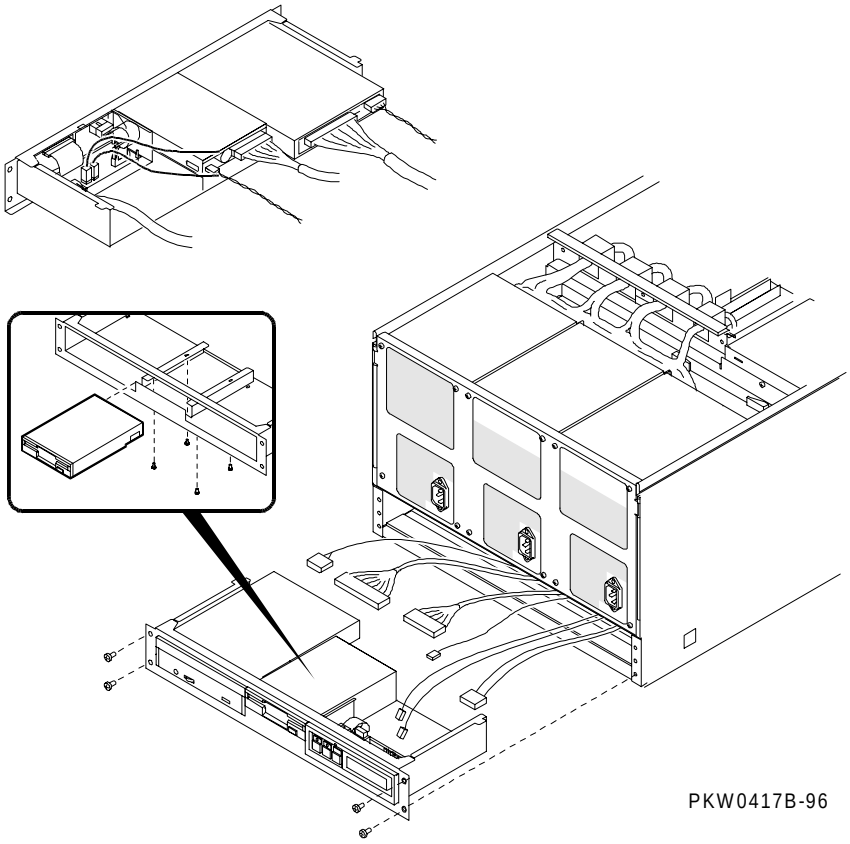
Reverse the steps in the Removal procedure. As you replace the tray in the drawer, be sure that the slides on the sides of the tray are placed on the rails in the drawer.

Verification

Power up the system. If the OCP you installed is faulty, the system will not power up or you will not see messages on the OCP display.

Floppy Removal and Replacement

Figure 6-20 Removing Floppy Drive



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Remove the four Phillips head screws holding the OCP tray to the system drawer.
4. Slide the tray out of the system drawer and disconnect cables attached to the OCP (unnecessary on a pedestal system), the floppy, and the CD-ROM drive. (In the pedestal system the OCP is in the tray above the power supplies.)
5. Move the tray to some handy work surface. Hold the tray vertically and from the bottom of the tray remove the four Phillips head screws that hold the floppy in place and remove it from the tray.

Replacement

Reverse the steps in the Removal procedure. As you replace the tray in the drawer, be sure that the slides on the sides of the tray are placed on the rails in the drawer.

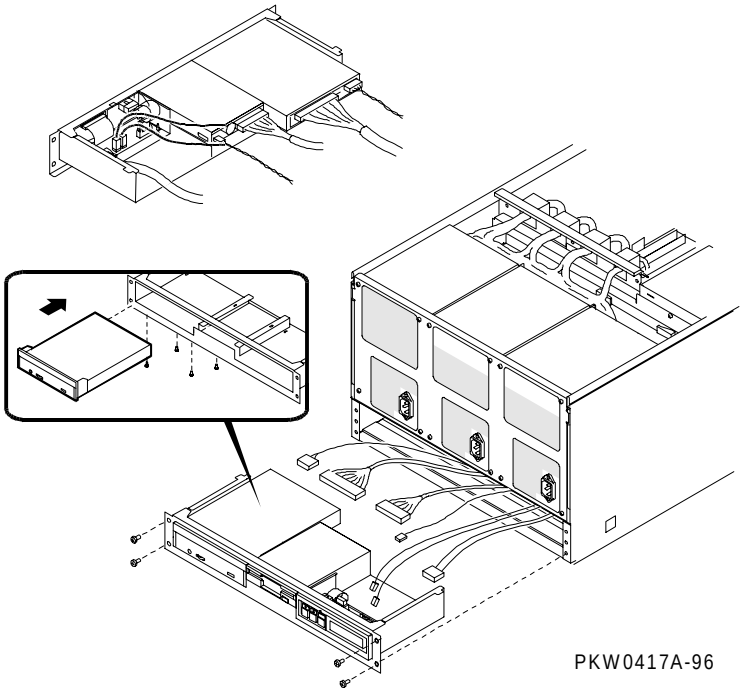
Verification

Power up the system. Use the following SRM console commands to test the floppy:

```
P00>>> show dev floppy
P00>>> HD buf/dva0
```

CD-ROM Removal and Replacement

Figure 6-21 Removing CD-ROM



Removal and Replacement

Removal

1. Shut down the operating system and power down the system.
2. Expose the system drawer.
3. Remove the four Phillips head screws holding the OCP tray to the system drawer.
4. Slide the tray out of the system drawer and disconnect cables attached to the OCP (unnecessary on a pedestal system), the floppy, and the CD-ROM drive. (In the pedestal system the OCP is in the pedestal tray above the power supplies.)
5. Move the tray to some handy work surface. Hold the tray vertically and from the bottom of the tray remove the four Phillips head screws that hold the floppy in place and remove it from the tray.

Replacement

Reverse the steps in the Removal procedure. As you replace the tray in the drawer, be sure that the slides on the sides of the tray are placed on the rails in the drawer.

Verification

Power up the system (press the Halt button if necessary to bring up the SRM console). Use the following SRM console commands to test the CD-ROM:

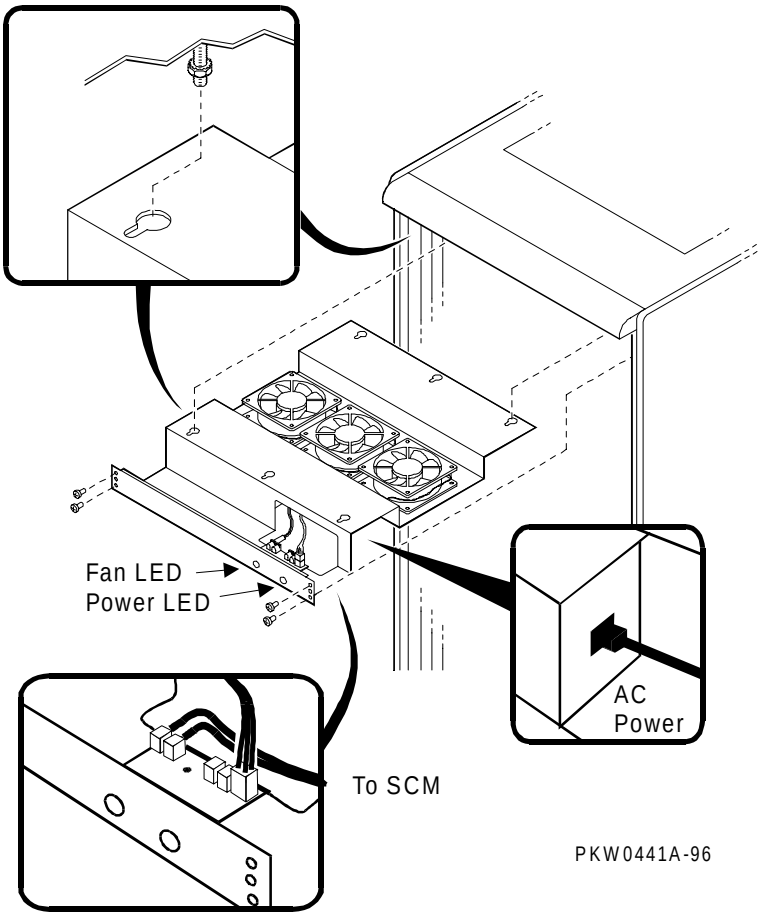
```
P00>>> show dev ncr0
```

```
P00>>> HD buf/dka nnn
```

where *nnn* is the device number; for example, dka500.

Cabinet Fan Tray Removal and Replacement

Figure 6-22 Removing Cabinet Fan Tray



Removal and Replacement

Removal

1. Shut down the operating system and power down the system. Unplug the AC power cable from the cabinet tray power supply.
2. If present, unplug any power cables going to the server control modules at the back of system drawers.
3. Unscrew the four Phillips head screws securing the fan tray to the top of the cabinet.
4. Loosen the four hex nuts that hold the tray to the top of the cabinet.
5. Holding the bottom of the tray, slide it out so that the holes in the tray frame slip over the loosened hex nuts.
6. Move the tray to a work surface to remove whatever component is being replaced.

Replacement

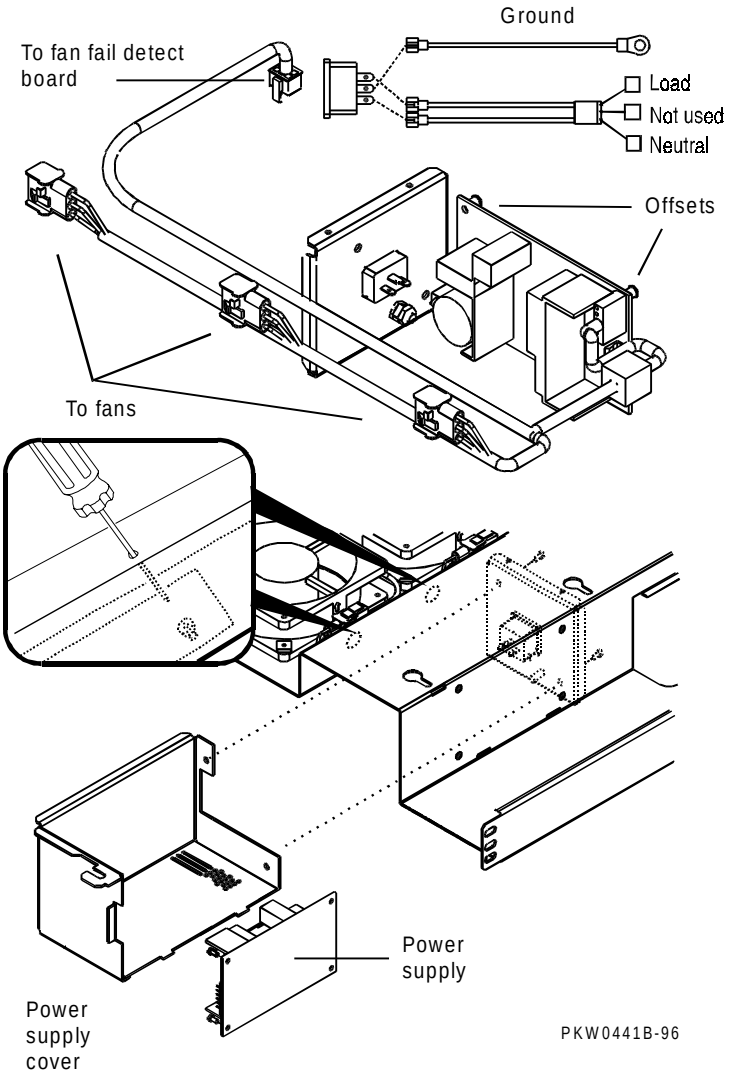
Reverse the steps in the Removal procedure.

Verification

Power up the system. If the green power LED comes on, and the fan LED is off, the cabinet fan tray is verified.

Cabinet Fan Tray Power Supply Removal and Replacement

Figure 6-23 Removing Cabinet Fan Tray Power Supply



Removal and Replacement

Removal

1. Remove the cabinet fan tray.
2. Disconnect the power harness from the fan fail detect module and each fan.
3. Remove the power supply cover. It is held in place by two screws that go through the AC bulkhead spot welded to the tray weldment.
4. Remove the power harness from the tray by disconnecting it from the power supply.
5. Disconnect the neutral and load leads from the power supply.
6. Remove the four screws holding the power supply to the tray. Keep track of the standoffs that provide space between the power supply and weldment. You will need them during replacement.

Replacement

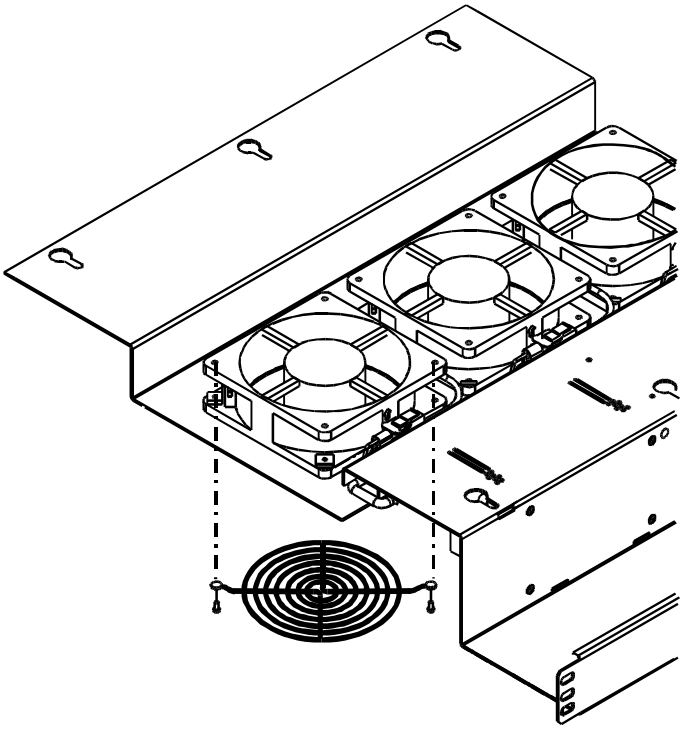
1. Reverse the steps in the Removal procedure.
2. Place the fan tray back in the cabinet.

Verification

Power up the system. If the green power LED comes on, and the fan LED is off, the cabinet fan tray power supply is verified.

Cabinet Fan Tray Fan Removal and Replacement

Figure 6-24 Removing Cabinet Fan Tray Fan



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Removal and Replacement

Removal

1. Remove the cabinet fan tray.
2. Disconnect the power harness from the fan you wish to replace.
3. Remove the fan finger guard.
4. Remove the two remaining screws holding the fan to the tray and remove the fan.
5. If the new fan does not have clip nuts, remove them from the fan.

Replacement

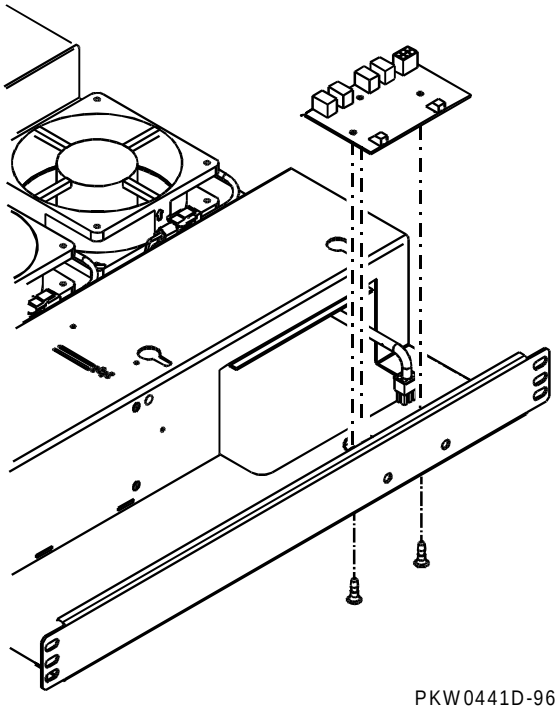
1. Reverse the Removal procedure, taking care to orient the fan so that the connection to the power harness is dressed nicely.
2. Place the fan tray back in the cabinet.

Verification

Power up the system. If the green power LED comes on, and the fan LED is off, the cabinet fan tray fan is verified.

Cabinet Fan Tray Fan Fail Detect Module Removal and Replacement

Figure 6-25 Removing Fan Tray Fan Fail Detect Module



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Removal and Replacement

Removal

1. Remove the cabinet fan tray.
2. Disconnect the power harness from the fan fail detect module.
3. Remove the fan fail detect module. In early systems, the module is held in place by three screws that go through the weldment, through three standoffs, through the module to nuts. In later systems, the module snaps in place.

Replacement

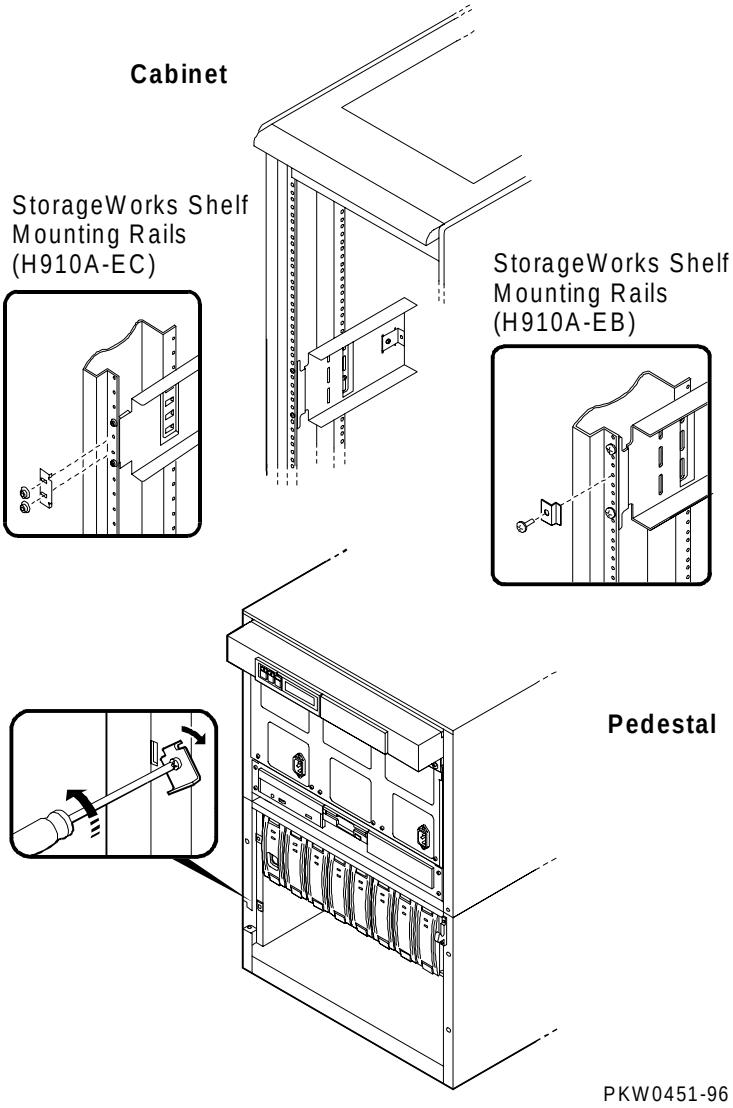
1. Reverse the steps in the Removal procedure.
2. Place the fan tray back in the cabinet.

Verification

Power up the system. If the green power LED comes on, and the fan LED is off, the cabinet fan fail detect module is verified.

StorageWorks Shelf Removal and Replacement

Figure 6-26 Removing StorageWorks Shelf



Removal

1. Shut down the operating system and power down the system.
2. Remove the power cord and signal cord(s) from the StorageWorks shelf.
3. Remove the two retaining brackets holding the shelf in the mounting rail by removing the Phillips head screws holding the brackets in place.
4. Slide the shelf out of the system.

Replacement

Reverse the steps in the Removal procedure.

Verification

Power up the system. Use the **show device console** command to verify that the StorageWorks shelf is configured into the system.

7
Running Utilities

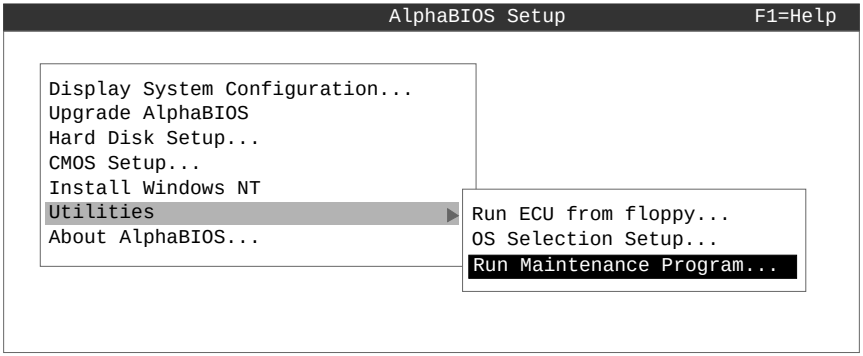
This chapter provides a brief overview of how to load and run utilities. The following topics are covered:

- Selecting Utilities from the AlphaBIOS Menu
- Running Utilities from a Serial Terminal
- Running the EISA Configuration Utility
- Running RAID Standalone Configuration Utility
- Updating Firmware

Selecting Utilities from the AlphaBIOS Menu

Start AlphaBIOS and select Utilities from the menu. The next selection depends on the utility to be run. For example, to run ECU, select Run ECU from floppy. To run RCU, select Run Maintenance Program.

Figure 7-1 Running a Utility from a Graphics Monitor



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Running Utilities from a Serial Terminal

Utilities are run from a serial terminal in the same way as from a graphics monitor. The menus are the same; but, some keys are different.

Table 7-1 AlphaBIOS Option Key Mapping

AlphaBIOS Key	VTxxx Key
F1	Ctrl/A
F2	Ctrl/B
F3	Ctrl/C
F4	Ctrl/D
F5	Ctrl/E
F6	Ctrl/F
F7	Ctrl/P
F8	Ctrl/R
F9	Ctrl/T
F10	Ctrl/U
Insert	Ctrl/V
Delete	Ctrl/W
Backspace	Ctrl/H
Escape	Ctrl/[

Running the EISA Configuration Utility

The EISA Configuration Utility (ECU) is used to configure EISA options on DIGITAL Server systems. The ECU is run from a graphics monitor.

1. Start **AlphaBIOS Setup**. If the system is in the SRM console, issue the command **alphabios**. (You can also set the SRM **console** environment variable to **graphics**.)
2. From **AlphaBIOS Setup**, select **Utilities**.
3. When you see the **Utilities** screen, select **Run ECU from floppy…** and press Enter.

   NOTE: The EISA Configuration Utility is supplied on a Microsoft Windows NT diskette shipped with the system.

4. Insert the correct ECU diskette for the operating system.
5. Press Enter to run the ECU software on the diskette.

The ECU main menu displays the following options:

```
EISA Configuration Utility
Steps in configuring your computer

STEP 1:  Important EISA configuration information
STEP 2:  Add or remove boards
STEP 3:  View or edit details
STEP 4:  Examine required details
STEP 5:  Save and exit
```

NOTE: Step 1 of the ECU provides online help. It is recommended that you select this step and become familiar with the utility before proceeding.

Running RAID Standalone Configuration Utility

The RAID Standalone Configuration Utility is used to set up RAID disk drives and logical units. The Standalone Utility is run from the AlphaBIOS Utility menu.

The DIGITAL Server 7300/7300R series system supports the KZPSC-*xx* PCI RAID controller (SWXCR). The KZPSC-*xx* kit includes the controller, RAID Array 230 Subsystems software, and documentation.

1. Start **AlphaBIOS Setup**. If the system is in the SRM console, issue the command **alphabios**. (You can also set the SRM **console** environment variable to **graphics**.)
2. From **AlphaBIOS Setup**, select **Utilities**.
3. When you see the **Utilities** screen, select **Run Maintenance Program**. Press Enter.
4. In the **Run Maintenance Program** dialog box, type **swxcrmgr** in the Program Name: field. Press Enter to execute the program.

The Main menu displays the following options:

```
[01.View/Update Configuration]
 02.Automatic Configuration
 03.New Configuration
 04.Initialize Logical Drive
 05.Parity Check
 06.Rebuild
 07.Tools
 08.Select SWXCR
 09.Controller Setup
 10.Diagnostics
```

Refer to the RAID Array Subsystems documentation for information on using the Standalone Configuration Utility to set up RAID drives.

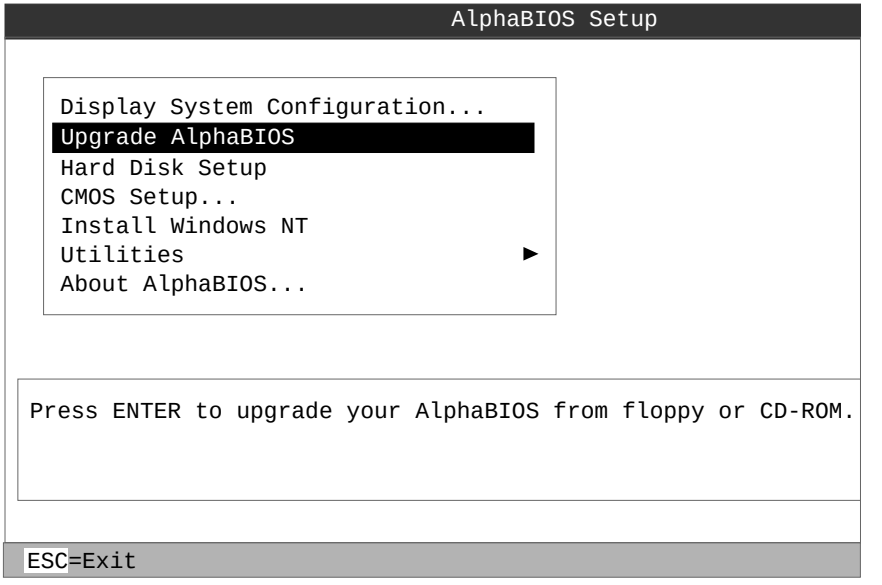
Updating Firmware

Use the Loadable Firmware Update (LFU) utility to update system firmware from an earlier version of AlphaBIOS.

NOTE: If jumper J50 is removed, make sure it is reinserted before you start the upgrade procedure. Otherwise the firmware will not be upgraded.

1. Insert the diskette or CD-ROM containing the AlphaBIOS upgrade.
2. If you are not already running **AlphaBIOS Setup**, start it by restarting your system and pressing F2 when the **Boot** screen is displayed.
3. In the main **AlphaBIOS Setup** screen, select **Upgrade AlphaBIOS** and press Enter as shown in the following figure. The system is reset and the Loadable Firmware Update (LFU) utility is started.

Figure 7-2 Starting LFU from the AlphaBIOS Console



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4. When the upgrade is complete, issue the LFU exit command. The system is reset and you return to AlphaBIOS. If you press the Reset button instead of issuing the LFU exit command, the system is reset and you are returned to LFU

The sections that follow show examples of updating firmware from the local CD-ROM, the local floppy, and a network device. Following these sections is an LFU command reference.

Updating Firmware from the Internal CD-ROM

1. Insert the CD-ROM with the updated firmware and select **Upgrade AlphaBIOS** from the main **AlphaBIOS Setup** screen. Use the Loadable Firmware Update (LFU) utility to perform the update.
2. Select the device from which firmware will be loaded. In this case, the choice is the internal CD-ROM.
3. Select the file that has the firmware update, or press Enter to select the default file. The file options are:

   AS4X00FW (default) - SRM console, AlphaBIOS console, and I/O adapter firmware

   AS4X00CP - SRM console and AlphaBIOS console firmware only

   AS4X00IO - I/O adapter firmware only

   The LFU function table and prompt (UPD>) display.
4. Use the LFU **list** command to determine the revision of firmware in a device and the most recent revision of that firmware available in the selected file.
5. Use the **update** command to update the device specified or all devices.
6. For each device, you are asked to confirm that you want to update the firmware. The default is no. Once the update begins, do not abort the operation. Doing so will corrupt the firmware on the module.
7. Use the **exit** command to return to AlphaBIOS.

Updating Firmware from the Internal Floppy Disk

Creating firmware from a floppy disk requires two steps:

- Creating the diskettes
- Performing the update

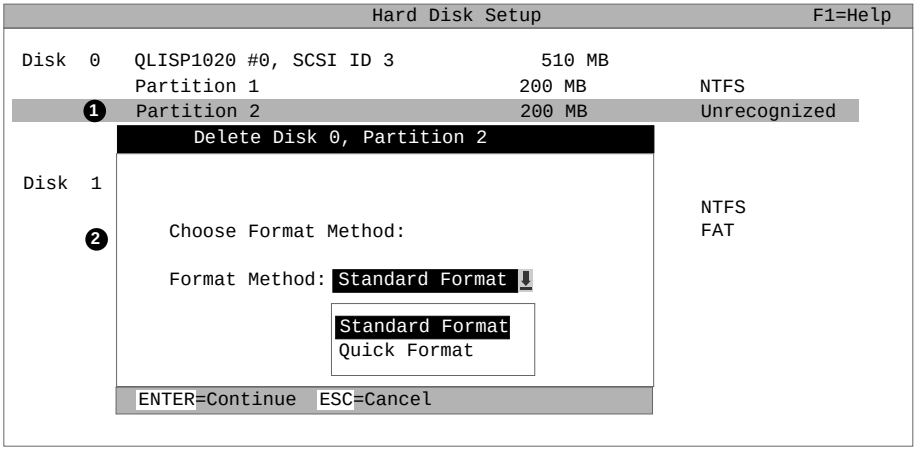
Creating the Diskettes

To update system firmware from floppy disk, you first must create the firmware update diskettes. You will need to create two diskettes: one for console updates, and one for I/O. Both of these must be FAT-formatted diskettes.

Download the update files from the Internet. (See the Preface of this book for the address.)

1. Start AlphaBIOS and select **Hard Disk Setup.** Press Enter.
2. Select the partition to be formatted, as shown in the following figure:

Figure 7-3 Formatting a FAT Partition



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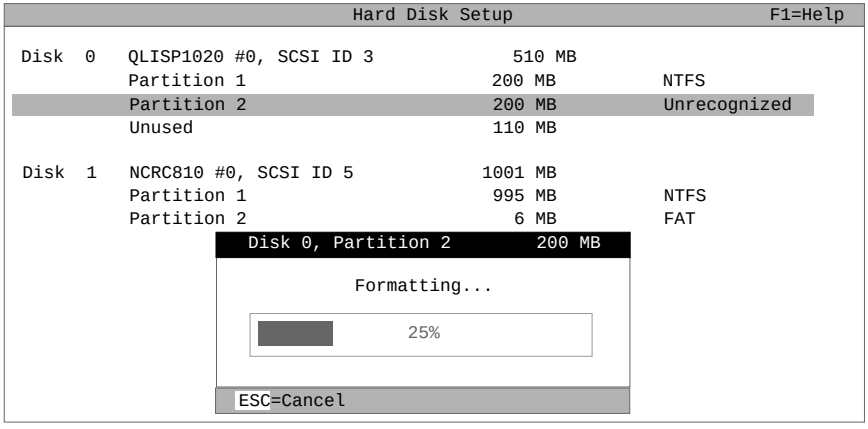
3. Press F6. A dialog box displays, asking whether to perform a quick or standard format (see ❷ in Figure 7-3). If you select **Quick Format**, the formatting is completed immediately, but no bad sectors are mapped. If you select **Standard Format**, a dialog box similar to that in Figure 7-4 displays while the drive is formatted, showing the progress of the formatting. Standard formatting maps bad sectors.
4. Select a format method, and press Enter. Figure 7-4 shows standard formatting.

Figure 7-4 Standard Formatting



PK-0736-96

Table 7-2 File Locations for Creating Update Diskettes on a PC

Console Update Diskette	I/O Update Diskette
AS4X00FW.TXT	AS4X00IO.TXT
AS4X00CP.TXT	RHREADME.SYS
RHREADME.SYS	CIPCA214.SYS
RHSRMROM.SYS	DFPAA246.SYS
RHARCROM.SYS	KZPAAA10.SYS

Updating Firmware from the Internal Floppy Disk — Performing the Update

1. Insert an update diskette you created into the internal floppy drive.
2. Select **Upgrade AlphaBIOS** from the main **AlphaBIOS Setup** screen to start LFU and select the internal floppy as the load device.

3. Select the file that has the firmware update you want, or press Enter to select the default file. When the internal floppy disk is the load device, the file options are:

   AS4X00CP (default) - SRM console and AlphaBIOS console firmware only

   AS4X00IO - I/O adapter firmware only

   AS4X00FW is not available, since the file is too large to fit on a 1.44 MB diskette. This means that when a floppy disk is the load device, you can update either console firmware or I/O adapter firmware, but not both in the same LFU session.

4. Use the LFU **list** command to determine the revision of firmware in a device and the most recent revision of that firmware available in the selected file.
5. Use the **update** command to update the device specified or all devices.
6. For each device, you are asked to confirm that you want to update the firmware. The default is no. Once the update begins, do not abort the operation. Doing so will corrupt the firmware on the module
7. If you need to update both, after finishing the first update, restart LFU with the **lfu** command and insert the floppy disk with the other file.
8. Use the **exit** command to return to the AlphaBIOS console.

Updating Firmware from a Network Device

The basic process of loading file from a network device is to:

1. Copy files to the local MOP server's MOP load area.
2. Start LFU.
3. Select ewa0 as the load device.

Before starting LFU, download the update files from the Internet (see the Preface of this document for the Internet address). You will need the files with the extension .SYS. Copy these files to your local MOP server's MOP load area. Then, take the following steps:

1. Select **Upgrade AlphaBIOS** from the main **AlphaBIOS Setup** screen to start LFU.
2. Select the device from which firmware will be loaded; in this case, a network device
3. Select the file that has the firmware update, or press Enter to select the default file. The file options are:

   AS4X00FW (default) - SRM console, AlphaBIOS console, and I/O adapter firmware

   AS4X00CP - SRM console and AlphaBIOS console firmware only

   AS4X00IO - I/O adapter firmware only

4. Use the LFU **list** command to determine the revision of firmware in a device and the most recent revision of that firmware available in the selected file.
5. Use the **update** command to update the device specified or all devices.
6. Use the **exit** command to return to the AlphaBIOS console.

LFU Commands

You can use the commands summarized in Table 7-3 to update system firmware.

Table 7-3 LFU Command Summary

Command	Function
display	Shows the system physical configuration.
exit	Terminates the LFU program.
help	Displays the LFU command list.
lfu	Restarts the LFU program.
list	Displays the inventory of update firmware on the selected device.
readme	Lists release notes for the LFU program.
update	Writes new firmware to the module.
verify	Reads the firmware from the module into memory and compares it with the update firmware.

These commands are described in the following pages.

display

The **display** command shows the system physical configuration. **Display** is equivalent to issuing the SRM console command **show configuration**. Because it shows the slot for each module, **display** can help you identify the location of a device.

exit

The **exit** command terminates the LFU program, causes system initialization and testing, and returns the system to the console from which LFU was called.

help

The **help** (or **?**) command displays the LFU command list, shown below.

```
------------------------------------------------------------------
 Function    Description
------------------------------------------------------------------
 Display     Displays the system's configuration table.
 Exit        Done exit LFU (reset).
 List        Lists the device, revision, firmware name, and update
             revision.
 Lfu         Restarts LFU.
 Readme      Lists important release information.
 Update      Replaces current firmware with loadable data image.
 Verify      Compares loadable and hardware images.
 ? or Help   Scrolls this function table.
------------------------------------------------------------------
```

lfu

The **lfu** command restarts the LFU program. This command is used when the update files are on a floppy disk. The files for updating both console firmware and I/O firmware are too large to fit on a 1.44 MB disk, so only one type of firmware can be updated at a time. Restarting LFU enables you to specify another update file.

list

The **list** command displays the inventory of update firmware on the CD-ROM, network, or floppy. Only the devices listed at your terminal are supported for firmware updates.

The **list** command shows three pieces of information for each device:

- Current Revision — The revision of the device's current firmware
- Filename — The name of the file used to update that firmware
- Update revision — The revision of the firmware update image

readme

The **readme** command lists release notes for the LFU program.

update

The **update** command writes new firmware to the module. Then LFU automatically verifies the update by reading the new firmware image from the module into memory and comparing it with the source image.

To update more than one device, you may use a wildcard but not a list. For example, **update k*** updates all devices with names beginning with k, and **update *** updates all devices. When you do not specify a device name, LFU tries to update all devices; it lists the selected devices to update and prompts before devices are updated. (The default is no.) The **-all** option removes the update confirmation requests, enabling the update to proceed without operator intervention.

*CAUTION: Never abort an **update** operation. Aborting corrupts the firmware on the module.*

verify

The **verify** command reads the firmware from the module into memory and compares it with the update firmware. If a module already verified successfully when you updated it, but later failed tests, you can use **verify** to tell whether the firmware has become corrupted.

8

SRM Console Commands and Environment Variables

This chapter provides a summary of the SRM console commands and environment variables. It includes the following topics:

- Summary of SRM Console Commands
- Summary of SRM Environment Variables
- Recording Environment Variables

The **test** command is described in Chapter 3 of this document. For complete reference information on the other SRM commands and environment variables, see the *DIGITAL Server 7300/7300R Series System Drawer User's Guide.*

NOTE: It is recommended that you keep a list of the environment variable settings for systems that you service, because you will need to restore certain environment variable settings after swapping modules. Refer to Table 8-3 for a convenient worksheet.

Summary of SRM Console Commands

The SRM console commands are used to examine or modify the system state.

Table 8-1 Summary of SRM Console Commands

Command	Function
alphabios	Loads and starts the AlphaBIOS console.
boot	Loads and starts firmware upgrades.
clear *envar*	Resets an environment variable to its default value.
deposit	Writes data to the specified address.
edit	Invokes the console line editor on a RAM file or on the nvram file (power-up script).
examine	Displays the contents of a memory location, register, or device.
halt	Halts the specified processor. (Same as **stop**.)
help	Displays information about the specified console command.
info *num*	Displays various types of information about the system:
	Info shows a list describing the **num** qualifier.
	Info 3 reads the impure area that contains the state of the CPU before it entered PAL mode.
	Info 5 reads the PAL built logout area that contains the data used by the operating system to create the error entry.
	Info 8 reads the IOD and IOD1 registers.
initialize	Resets the system.
lfu	Runs the Loadable Firmware Update Utility.

Continued

Table 8-1 Summary of SRM Console Commands (Continued)

Command	Function
man	Displays information about the specified console command.
more	Displays a file one screen at a time.
prcache	Initializes and displays status of the PCI NVRAM.
set *envar*	Sets or modifies the value of an environment variable.
set rcm_dialout	Sets a modem dialout string.
show *envar*	Displays the state of the specified environment variable.
show config	Displays the configuration at the last system initialization.
show cpu	Displays the state of each processor in the system.
show device	Displays a list of controllers and their devices in the system.
show fru	Displays the serial number and revision level of system bus options.
show memory	Displays memory module information.
show network	Displays the state of network devices in the system.
show pal	Displays the version of the privileged architecture library code (PALcode).
show power	Displays information about the power supplies, system fans, CPU fans, and temperature.
show rcm_dialout	Displays the modem dialout string.
show version	Displays the version of the console program.
start	Starts a program that was previously loaded on the processor specified.
stop	Halts the specified processor. (Same as **halt**.)
test	Runs firmware diagnostics for the system.

Summary of SRM Environment Variables

Environment variables pass configuration information between the console and the operating system. Their settings determine how the system powers up, boots the operating system, and operates. Environment variables are set or changed with the set *envar* command and returned to their default values with the clear *envar* command. Their values are viewed with the show *envar* command. The SRM environment variables are specific to the SRM console.

Table 8-2 Environment Variable Summary

Environment Variable	Function
com2_baud	Changes the default baud rate of the COM2 serial port.
console	Specifies the device on which power-up output is displayed (serial terminal or graphics monitor).
cpu_enabled	Enables or disables a specific secondary CPU.
ew*0_mode	Specifies the connection type of the default Ethernet controller.
ew*0_protocols	Specifies network protocols for booting over the Ethernet controller.
kbd_hardware_type	Specifies the default console keyboard type.
kzpsa*_host_id	Specifies the default value for the KZPSA host SCSI bus node ID.
language	Specifies the console keyboard layout.

Continued

Table 8-2 Environment Variable Summary (Continued)

Environment Variable	Function
ocp_text	Overrides the default OCP display text with specified text.
os_type	Specifies the operating system and sets the appropriate console interface. Should always be set to **nt**.
pci_parity	Disables or enables parity checking on the PCI bus.
pk*0_fast	Enables fast SCSI mode.
pk*0_host_id	Specifies the default value for a controller host bus node ID.
pk*0_soft_term	Enables or disables SCSI terminators on systems that use the QLogic ISP1020 SCSI controller.
sys_model_num	Displays the system model number and computes certain information passed to the operating system. Must be restored after a PCI motherboard is replaced.
sys_serial_num	Restores the system serial number. Must be set if the system motherboard is replaced.
sys_type	Displays the system type and computes certain information passed to the operating system. Must be restored after a PCI motherboard is replaced.
tga_sync_green	Specifies the location of the SYNC signal generated by the DIGITAL ZLXp-E PCI graphics accelerator option.
tt_allow_login	Enables or disables login to the SRM console firmware on other console ports.

Recording Environment Variables

You can make copies of the table below to record environment variable settings for specific systems. Write the system name in the column provided. Enter the **show*** command to list the system settings.

Table 8-3 Environment Variables Worksheet

Environment Variable	System Name	System Name	System Name
com2_baud			
console			
cpu_enabled			
ew*0_mode			
ew*0_protocols			
kbd_hardware_ type			
kzpsa*_host_id			
language			
ocp_text			
os_type			
pci_parity			
pk*0_fast			
pk*0_host_id			
pk*0_soft_term			

Continued

Table 8-3 Environment Variables Worksheet (Continued)

Environment Variable	System Name	System Name	System Name
pk*0_soft_term			
sys_model_num			
sys_serial_num			
sys_type			
tga_sync_green			
tt_allow_login			

9

Operating the System Remotely

This chapter describes how to use the remote console monitor (RCM) to monitor and control the system remotely. It includes the following topics:

- RCM Console Overview
- Modem Usage
- Entering and Leaving Command Mode
- RCM Commands
- Dial-Out Alerts
- Resetting the RCM to Factory Defaults
- Troubleshooting Guide
- Modem Dialog Details

RCM Console Overview

You use the remote console monitor (RCM) to monitor and control the system remotely. The RCM resides on the server control module and allows the system administrator to connect remotely to a managed system through a modem, using a serial terminal or terminal emulator.

The RCM has special console firmware that is used to control a DIGITAL Server system remotely. The RCM firmware resides on an independent microprocessor. It is not part of the SRM console that resides in the flash ROM.

The RCM firmware has its own command interface that allows the user to perform the tasks that can usually be done from the system's serial console terminal. You use the RCM console commands to reset, halt, and power the system on or off, regardless of the operating system or hardware state. You can also use the RCM console commands to monitor the power supplies, temperature, and fans.

You can enter the RCM console either remotely or through the local serial console terminal. Once in command mode, you can enter commands to control and monitor the system.

To enter the RCM console remotely, you dial in through a modem, enter a password, and then type a special escape sequence that invokes RCM command mode. You must set up the modem before you can dial in remotely. See the section “Modem Usage.”

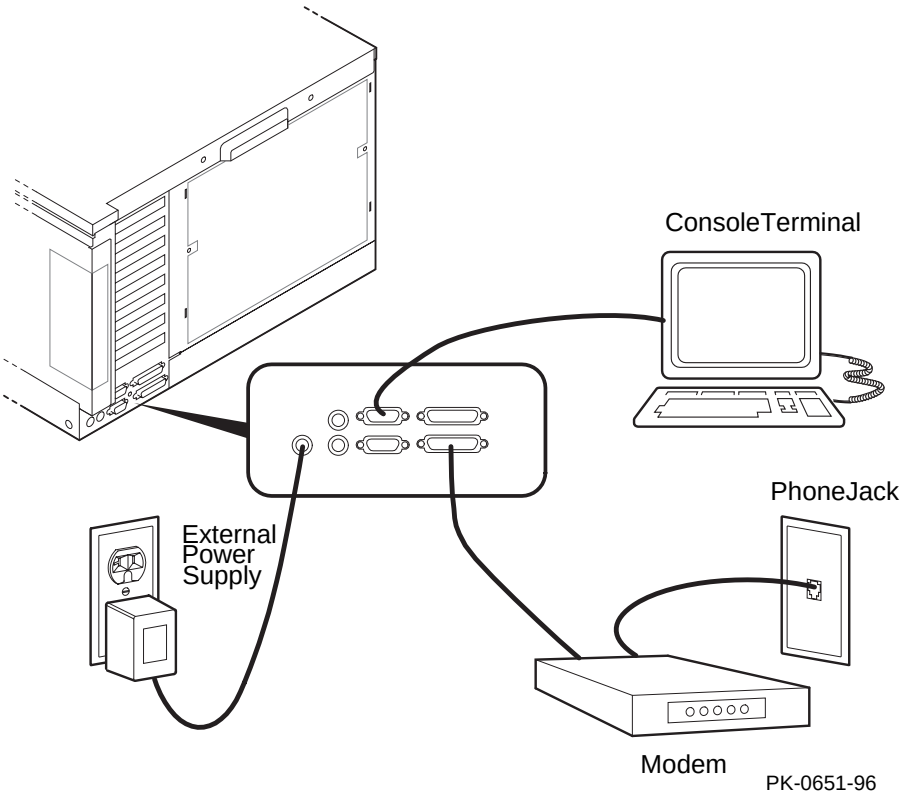
To enter the RCM console locally, you type the escape sequence at the SRM console prompt on the local serial console terminal.

The RCM also provides an autonomous dial-out capability when it detects a power failure within the system. When triggered, the RCM dials a paging service at 30-minute intervals until the administrator clears the alert within the RCM.

Modem Usage

To use the RCM to monitor a system remotely, first make the connections to the server control module, as shown below. Then configure the modem port for dial-in.

Figure 9-1 RCM Connections



Modem Selection

The RCM requires a Hayes-compatible modem. The controls that the RCM sends to the modem have been selected to be acceptable to a wide selection of modems. The modems that have been tested and qualified include:

- Motorola LifeStyle Series 28.8
- AT&T DATAPORT 14.4/FAX
- Zoom Model 360

The U.S. Robotics Sportster DATA/FAX MODEM is also supported, but requires some modification of the modem initialization and answer strings. See the section “RCM Commands.”

Modem Configuration Procedure

1. Connect a Hayes-compatible modem to the RCM as shown in Figure 9-1, and power up the modem.
2. From the local serial console terminal, enter the RCM firmware console by typing the following escape sequence:

   ```
   ^]^]rcm
   ```

   You create the character “^” by simultaneously holding down the Ctrl key and pressing the] key (right square bracket). The firmware prompt, RCM>, should now be displayed.
3. Enter a modem password with the **setpass** command. See the section “RCM Commands.”
4. Enable the modem port with the **enable** command. See the section “RCM Commands.”
5. Enter the **quit** command to leave the RCM console.
6. You are now ready to dial in remotely.

Dialing In to the RCM Modem Port

1. Dial the modem connected to the server control module. The RCM answers the call and after a few seconds prompts for a password with a "#" character.
2. Enter the password that was loaded using the **setpass** command. You have three tries to correctly enter the password. On the third unsuccessful attempt, the connection is terminated, and as a security precaution, the modem is not answered again for 5 minutes.

   On successful entry of the password, the RCM banner message "RCM V1.0" is displayed, and you are connected to the system COM1 port. At this point the local terminal keyboard is disabled except for entering the RCM console firmware. The local terminal displays all the terminal traffic going out to the modem.
3. To connect to the RCM firmware console, type the RCM escape sequence.

Refer to Example 9-1 for an example of the modem dial-in procedure.

Example 9-1 Sample Remote Dial-In Dialog

`ATQ0V1E1S0=0`
`OK`
`ATDT30167`
`CONNECT 9600`
	When modem dial-in connection is made, a screen display similar to this appears.

`#`	Enter password at this prompt.
`RCM V1.0`	RCM banner is displayed.
`^]^]rcm`	Enter the escape sequence after the banner is displayed. The escape sequence is not echoed on the terminal.
`RCM>`	RCM prompt is displayed. Commands to control and monitor the system can be entered.

Terminating a Modem Session

Terminate the modem session by executing a **hangup** command from the RCM console firmware. This will cleanly terminate the modem connection.

If the modem connection is terminated without using the **hangup** command, or if the line is dropped due to phone line problems, the RCM will detect carrier loss and initiate an internal **hangup** command. This process can take a minute or more, and the local terminal will be locked out until the auto hangup process completes.

If the modem link is idle for more than 20 minutes, the RCM initiates an auto hangup.

Entering and Leaving Command Mode

Use the default escape sequence to enter RCM command mode for the first time. You can enter RCM command mode from the SRM console level, the operating-system level, or an application. The RCM quit command reconnects the terminal to the system console port.

Example 9-2 Entering and Leaving RCM Command Mode

```
^]^]rcm                ❶
RCM>


RCM> quit              ❷
Focus returned to COM port
```

Entering the RCM Firmware Console

To enter the RCM firmware console, enter the RCM escape sequence. See ❶ in Example 9-2 for the default sequence.

The escape sequence is not echoed on the terminal or sent to the system. Once in the RCM firmware console, the user is in RCM command mode and can enter RCM console commands.

Leaving Command Mode

To leave RCM command mode and reconnect to the system console port, enter the **quit** command, then press Return to get a prompt from the operating system or system console. (See ❷ in Example 9-2.)

RCM Commands

The RCM commands summarized below are used to control and monitor a system remotely.

Table 9-1 RCM Command Summary

Command	Function
alert_clr	Clears alert flag, stopping dial-out alert cycle
alert_dis	Disables the dial-out alert function
alert_ena	Enables the dial-out alert function
disable	Disables remote access to the modem port
enable	Enables remote access to the modem port
hangup	Terminates the modem connection
halt	Halts server
help or **?**	Displays the list of commands
poweroff	Turns off power to server
poweron	Turns on power to server
quit	Exits console mode and returns to system console port
reset	Resets the server
setesc	Changes the escape sequence for entering command mode
setpass	Changes the modem access password
status	Displays server's status and sensors

Command Conventions

- The commands are not case sensitive.
- A command must be entered in full.
- If a command is entered that is not valid, the command fails with the message:

```
*** ERROR - unknown command ***
```

  Enter a valid command.

The RCM commands are described on the following pages.

alert_clr

The **alert_clr** command clears an alert condition within the RCM. The alert enable condition remains active, and the RCM will again enter the alert condition when it detects a system power failure.

```
RCM>alert_clr
```

alert_dis

The **alert_dis** command disables RCM dial-out capability. It also clears any outstanding alerts. The alert disable state is nonvolatile. Dial-out capability remains disabled until the **alert_enable** command is issued.

```
RCM>alert_dis
```

alert_ena

The **alert_ena** command enables the RCM to automatically dial out when it detects a power failure within the system. The RCM repeats the dial-out alert at 30-minute intervals until the alert is cleared. The alert enable state is nonvolatile. Dial-out capability remains enabled until the **alert_disable** command is issued.

```
RCM>alert_ena
```

In order for the **alert_enable** command to work, two conditions must be met:

A modem dial-out string must be entered with the system console.

Remote access to the RCM modem port must be enabled with the **enable** command.

If the **alert_enable** command is entered when remote access is disabled, the following message is returned:

```
*** error ***
```

disable

The **disable** command disables remote access to the RCM modem port.

```
RCM>disable
```

The module's remote access default state is DISABLED. The modem enable state is nonvolatile. When the modem is disabled, it remains disabled until the **enable** command is issued. If a modem connection is in progress, entering the **disable** command terminates it.

enable

The **enable** command enables remote access to the RCM modem port. It can take up to 10 seconds for the **enable** command to be executed.

```
RCM>enable
```

The module's remote access default state is DISABLED.

The modem enable state is nonvolatile. When the modem is enabled, it remains enabled until the **disable** command is issued.

The **enable** command can fail for two reasons:

- There is no modem access password configured.
- The modem is not connected or is not working properly.

If the **enable** command fails, the following message is displayed:

```
*** ERROR - enable failed ***
```

hangup

The **hangup** command terminates the modem session. When this command is issued, the remote user is disconnected from the server. This command can be issued from either the local or remote console.

```
RCM>hangup
```

halt

The **halt** command attempts to halt the managed system. It is functionally equivalent to pressing the Halt button on the system operator control panel to the "in" position and then releasing it to the "out" position. The RCM console firmware exits command mode and reconnects the user's terminal to the server's COM1 serial port.

```
RCM>halt
Focus returned to COM port
```

NOTE: Pressing the Halt button has no effect on systems running Windows NT.

help or ?

The **help** or **?** command displays the RCM firmware command set.

poweroff

The **poweroff** command requests the RCM module to power off the system. It is functionally equivalent to turning off the system power from the operator control panel.

```
RCM>poweroff
```

If the system is already powered off, this command has no effect.

The external power to the RCM must be connected in order to power off the system from the RCM firmware console. If the external power supply is not connected, the command will not power the system down, and displays the message:

```
*** ERROR ***
```

poweron

The **poweron** command requests the RCM module to power on the system. For the system power to come on, the following conditions must be met:

- AC power must be present at the power supply inputs.
- The DC On/Off button must be in the "on" position.
- All system interlocks must be set correctly.

The RCM firmware console exits command mode and reconnects the user's terminal to the system console port.

```
RCM>poweron
Focus returned to COM port
```

NOTE: If the system is powered off with the DC On/Off button, the system will not power up. The RCM will not override the

"off" state of the DC On/Off button. If the system is already powered on, the poweron command has no effect.

quit

The **quit** command exits the user from command mode and reconnects the user's terminal to the system console port. The following message is displayed:

```
Focus returned to COM port
```

The next display depends on what the system was doing when the RCM was invoked. For example, if the RCM was invoked from the SRM console prompt, the console prompt will be displayed when you enter a carriage return. Or, if the RCM was invoked from the operating system prompt, the operating system prompt will be displayed when you enter a carriage return.

reset

The **reset** command requests the RCM module to perform a hardware reset. It is functionally equivalent to pressing the Reset button on the system operator control panel.

```
RCM>reset
Focus returned to COM port
```

The following events occur when the **reset** command is executed:

- The system restarts and the system console firmware reinitializes.
- The console exits RCM command mode and reconnects the user's terminal to the server's COM1 serial port.
- The power-up messages are displayed, and then the console prompt is displayed or the operating system boot messages are displayed, depending on the state of the Halt button.

setesc

The **setesc** command allows the user to reset the default escape sequence for entering console mode. The escape sequence can be any character string. A typical sequence consists of 2 or more characters, to a maximum of 15 characters. The escape sequence is stored in the module's on-board NVRAM.

NOTE: If you change the escape sequence, be sure to record the new sequence. Although the module factory defaults can be restored if the user has forgotten the escape sequence, this involves accessing the server control module and moving a jumper.

The following sample escape sequence consists of five iterations of the Ctrl key and the letter “o”.

```
RCM>setesc
^o^o^o^o^o
RCM>
```

If the escape sequence entered exceeds 15 characters, the command fails with the message:

```
*** ERROR ***
```

When changing the default escape sequence, avoid using special characters that are used by the system’s terminal emulator or applications.

Control characters are not echoed when entering the escape sequence. To verify the complete escape sequence, use the **status** command.

setpass

The **setpass** command allows the user to change the modem access password that is prompted for at the beginning of a modem session. The password is stored in the module’s on-board NVRAM.

```
RCM>setpass
new pass>*********
RCM>
```

The maximum password length is 15 characters. If the password entered exceeds 15 characters, the command fails with the message:

```
***  ERROR ***
```

The minimum password length is one character, followed by a carriage return. If only a carriage return is entered, the command fails with the message:

```
*** ERROR - illegal password ***
```

If you have forgotten the password, you can now enter a new password.

status

The **status** command displays the current state of the server's sensors, as well as the current escape sequence and alarm information.

```
RCM>status

Firmware Rev: V1.0
Escape Sequence: ^]^]RCM
Remote Access: ENABLE/DISABLE
Alerts: ENABLE/DISABLE
Alert Pending: YES/NO (C)
Temp (C): 26.0
RCM Power Control: ON/OFF
External Power: ON
Server Power: OFF

RCM>
```

The status fields are explained in Table 9-2.

Table 9-2 RCM Status Command Fields

Item	Description
Firmware Rev:	Revision of RCM firmware.
Escape Sequence:	Current escape sequence to enter RCM firmware console.
Remote Access:	Modem remote access state. (ENABLE/DISABLE)
Alerts:	Alert dial-out state. (ENABLE/DISABLE)
Alert Pending:	Alert condition triggered. (YES/NO)
Temp (C):	Current system temperature in degrees Celsius.
RCM Power Control:	Current state of RCM system power control. (ON/OFF)
External Power:	Current state of power from external power supply to server control module. (ON/OFF)
Server Power:	Current state of system power. (ON/OFF)

Dial-Out Alerts

The RCM can be configured to automatically dial out through the modem (usually to a paging service) when it detects a power failure within the system. When a dial-out alert is triggered, the RCM initializes the modem for dial-out, sends the dial-out string, hangs up the modem, and reconfigures the modem for dial-in. The RCM and modem must continue to be powered, and the phone line must remain active, for the dial-out alert function to operate.

Example 9-3 Configuring the Modem for Dial-Out Alerts

```
P00>>> set rcm_dialout "ATDTstring#;"  ❶


RCM>enable
RCM>status
.
.
Remote Access:  ENABLE                 ❷
.
RCM>alert_ena                          ❸
```

Example 9-5 Typical RCM Dial-Out Command

```
P00>>> set rcm_dialout "ATXDT9,15085553333,,,,,,5085553332#;"
```

Use the **show** command to verify the RCM dial-out string:

```
P00>>> show rcm_dialout
rcm_dialout       ATXDT9,15085553333,,,,,,5085553332#;
```

Enabling the Dial-Out Alert Function:

1. Enter the **set rcm_dialout** command, followed by a dial-out alert string, from the SRM console (see ❶ in **Error! Reference source not found.**).
2. The *string* is a modem dial-out character string, not to exceed 47 characters, that is used by the RCM when dialing out through the modem. See the next topic for details on composing the modem dial-out string.
3. Enter the RCM firmware console and enter the **enable** command to enable remote access dial-in. The RCM firmware **status** command should display "Remote Access: ENABLE." (See ❷.)
4. Enter the RCM firmware **alert_ena** command to enable outgoing alerts. (See ❸.)

Composing a Modem Dial-Out String

The modem dial-out string emulates a user dialing an automatic paging service. Typically, the user dials the pager phone number, waits for a tone, and then enters a series of numbers.

The RCM dial-out string (Example 9-5) has the following requirements:

- The entire string following the **set rcm_dialout** command must be enclosed by quotation marks.
- The characters ATDT must be entered after the opening quotation marks. Do not mix case. Enter the characters either in all uppercase or all lowercase.
- Enter the character X if the line to be used also carries voice mail. Refer to the example that follows.
- The valid characters for the dial-out string are the characters on a phone keypad: 0–9, *, and #. In addition, a comma (,) requests that the modem pause for 2 seconds, and a semicolon (;) is required to terminate the string.

Elements of the Dial-Out String

`ATXDT`	AT = Attention X = Forces the modem to dial "blindly" (not look for a dial tone). Enter this character if the dial-out line modifies its dial tone when used for services such as voice mail. D = Dial T = Tone (for touch-tone) , = Pause for 2 seconds.
`9,`	In the example, "9" gets an outside line. Enter the number for an outside line if your system requires it.
`15085553333`	Dial the paging service.
`,,,,,,`	Pause for 12 seconds for paging service to answer.
`5085553332#`	"Message," usually a call-back number for the paging service.
`;`	Return to console command mode. Must be entered at end of string.

Resetting the RCM to Factory Defaults

If the escape sequence has been forgotten, you can reset the controller to factory settings.

Reset Procedure

1. Power down the DIGITAL Server system and access the server control module, as follows:

   Expose the PCI bus card cage. Remove three Phillips head screws holding the cover in place and slide it off the drawer. If necessary, remove several PCI and EISA options from the bottom of the PCI card cage until you have enough space to access the server control module.

2. Unplug the external power supply to the server control module.

   Locate the password and option reset jumper. The jumper number, which is etched on the board, depends on the revision of the server control module.

   NOTE: If the RCM section of the server control module does not have an orange relay, the jumper number is J6. If the RCM section of the server control module has an orange relay, the jumper number is J7.

3. Move the jumper so that it is sitting on both pins.

4. Replace any panels or covers as necessary so you can power up the system. Press the Halt button and then power up the system to the SRM console prompt.

5. Powering up with the password and option reset jumper in place resets the escape sequence, password, and modem enable states to the factory default.

6. When the console prompt is displayed, power down the system and move the password and option reset jumper back onto the single pin.

7. Replace any PCI or EISA modules you removed and replace the PCI bus card cage cover.

8. Power up the system to the SRM console prompt and type the default escape sequence to enter RCM command mode:

   ```
   ^]^]RCM
   ```

9. Configure the module as desired. You must reset the password and modem enable states in order to enable remote access.

Troubleshooting Guide

Table 9-3 lists a number of possible causes and suggested solutions for symptoms you might see.

Table 9-3 RCM Troubleshooting

Symptom	Possible Cause	Suggested Solution
The local terminal will not communicate with the system or the RCM.	System and terminal baud rate set incorrectly.	Set the system and terminal baud rates to 9600 baud.
	Cables not correctly installed.	Review external cable installation.
RCM will not answer when the modem is called.	Modem cables may be incorrectly installed.	Check modem phone lines and connections.
	RCM remote access is disabled.	Enable remote access.
	RCM does not have a valid password set.	Set password and enable remote access.
	The local terminal is currently in the RCM console firmware.	Issue a **quit** command on the local terminal.
	On power-up, the RCM defers initializing the modem for 30 seconds to allow the modem to complete its internal diagnostics and initialization.	Wait 30 seconds after powering up the system and RCM before attempting to dial in.
	Modem may have had power cycled since last being initialized or modem is not set up correctly.	Enter **enable** command from RCM console.

Continued

Table 9-3 RCM Troubleshooting (Continued)

Symptom	Possible Cause	Suggested Solution
After the system and RCM are powered up, the COM port seems to hang and then starts working after a few seconds.	This delay is normal behavior.	Wait a few seconds for the COM port to start working.
RCM installation is complete, but system will not power up.	RCM Power Control: is set to DISABLE.	Enter RCM console and issue the **poweron** command.
New password, escape sequence, and modem enable state are forgotten when system and RCM module are powered down.	The password and option reset jumper is still installed. If the RCM section of the server control module does not have an orange relay, the jumper number is J6. If it does have an orange relay, the number is J7.	After resetting RCM to factory defaults, move the jumper so that it is sitting on only one pin.
The remote user sees a "+++" string on the screen.	The modem is confirming whether the modem has really lost carrier. This occurs when the modem sees an idle time, followed by a "3," followed by a carriage return, with no subsequent traffic. If the modem is still connected, it will remain so.	This is normal behavior.
The message "unknown command" is displayed when the user enters a carriage return by itself.	The terminal or terminal emulator is including a linefeed character with the carriage return.	Change the terminal or terminal emulator setting so that "new line" is not selected.

Continued

Table 9-3 RCM Troubleshooting (Continued)

Symptom	Possible Cause	Suggested Solution
Cannot enable modem or modem will not answer.	The modem is not configured correctly to work with the RCM.	Modify the modem initialization and/or answer string.

Modem Dialog Details

This section provides further details on the dialog between the RCM and the modem and is intended to help you reprogram your modem if necessary.

Phases of Modem Operation

The RCM is programmed to expect specific responses from the modem during four phases of operation:

- Initialization
- Ring detection
- Answer
- Hang-up

The initialization and answer command strings are stored in the RCM NVRAM. The factory default strings are:

Initialization string: `AT&F0EVS0=0S12=50<cr>`

Answer string `ATXA<cr>`

NOTE: All modem commands must be terminated with a <cr> character (0x0d hex).

Initialization

The RCM initializes the modem to the following configuration:

Factory defaults (`&F0`)

No Echo (`E`)

Numeric response codes (`V`)

No Auto Answer (`S0=0`)

Guard-band = 1 second (`S12=50`)

Fixed modem-to-RCM baud rate

Connect at highest possible reliability and speed

The RCM expects to receive a "**`0<cr>`**" (OK) in response to the initialization string. If it does not, the **enable** command will fail.

This default initialization string works on a wide variety of modems. If your modem does not configure itself to these parameters, the initialization string will need to be modified. See the topic in this section entitled Modifying Initialization and Answer Strings.

Ring Detection

The RCM expects to be informed of an in-bound call by the modem signaling the RCM with the string, "2<cr>" (RING).

Answer

When the RCM receives the ring message from the modem, it responds with the answer string. The "X" command modifier used in the default answer string forces the modem to report simple connect, rather than connect at *xxxx*. The RCM expects a simple connect message, "1<cr>" (CONNECTED). If the modem responds with anything else, the RCM forces a hang-up and initializes the modem.

The default answer string is formatted to request the modem to provide only basic status. If your modem does not provide the basic response, the answer string, and/or initialization string will need to be modified. See the topic in this section entitled Modifying Initialization and Answer Strings.

After receiving the "connect" status, the modem waits for 6 seconds and then prompts the user for a password.

Hangup

When the RCM is requested to hang up the modem, it forces the modem into command mode and issues the **hangup** command to the modem. This is done by pausing for a minimum of the guard time, sending the modem "+++". When the modem responds with "0<cr>" (OK), the hang-up command string is sent. The modem should respond with "3<cr>" (NO CARRIER). After this interchange, the modem is reinitialized in preparation for the next dial-in session.

RCM/Modem Interchange Overview

Table 9-4 summarizes the actions between the RCM and the modem from initialization to hangup.

Table 9-4 RCM/Modem Interchange Summary

Action	Data to Modem	Data from Modem
Initialization command	AT&F0EVS0=0S12=50<cr>	
Initialization successful		0<cr>
Phone line ringing		2<cr>
RCM answering	ATXA<cr>	
Modem successfully connected		1<cr>
Force modem into command mode	<guard_band>+++	
Modem in command mode		0<cr>
Hangup	ATH<cr>	
Successful hangup		3<cr>

Modifying Initialization and Answer Strings

The initialization and answer strings are stored in the RCM's NVRAM. They come pre-programmed to support a wide selection of modems. In the circumstance where the default initialization and answer strings do not set the modem into the desired mode, the following SRM **set** and **show** commands are provided to enable the user to define and examine the initialization and answer strings.

To replace the initialization string:

```
P00>>> set rcm_init "new_init_string"
```

To replace the answer string:

```
P00>>> set rcm_answer "new_answer_string"
```

To display all the RCM user settable strings:

```
P00>>> show rcm*
rcm_answer  ATXA
rcm_dialout
rcm_init    AT&F0EVS0=0S12=50
P00>>>
```

Initialization and Answer String Substitutions

The RCM default initialization and answer strings are as follows:

Initialization String: "AT&F0EVS0=0S12=50"

Answer String: "ATXA"

The following modem requires a modified answer string.

	Initialization String	Answer String
USRobotics Sportster 28,800 Data/Fax Modem	RCM default	"ATX0&B1&A0A"

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