Digital AlphaStation 200/400 Series

Technical Information

Part Number: EK-PCDSA-TI. A01

Digital Equipment Corporation
Maynard, Massachusetts

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Preface

Intended Audience

This information is intended for VARs (value-added resellers), ISVs, and other system users or service providers who are configuring their own systems or adding features to existing AlphaStation 200/400 Series systems.

Document Contents

This information covers the following general topics (see the Table of Contents for a detailed listing of the material mentioned here):

- Distinctive system features of the Digital AlphaStation 200 Series and 400 Series systems
- Steps in system configuration
- Addressing
- I/O programming
- Direct memory access (DMA)
- Hardware exceptions and interrupts
- System power-up and initialization
- AlphaStation firmware
- Errors and machine checks
- Connector and cable information
- Console commands
- Registers

Associated Documents

For additional information on the Digital AlphaStation 200/400 Series systems, refer to the following information sources:

- *Digital AlphaStation 400 Series User Information* (EK-PCDSA-UI)
- *Digital AlphaStation 400 Series Installation Information* (EK-PCDSA-II)
- *Digital AlphaStation 200 Series User Information* (EK-PCDTA-UI)
- *Digital AlphaStation 200 Series Installation Information* (EK-PCDTA-II)

Refer to the following additional sources for technical information:

- *System I/O (SIO) 82378IB chip*, Intel
- *PC87332 (Super I/O III) chip*, National Semiconductor
- *Alpha Architecture Handbook* (EC-H1689-10), Digital Equipment Corporation
- *DECchip 21064 and DECchip 21064A Microprocessor Hardware Reference Manual*, order number EC-Q9ZUA-TE, Digital Equipment Corporation
- *DECchip 2107/21072 Core Chip Sets Data Sheet*, order number EC-N0648-72, Digital Equipment Corporation
- *DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual* (EC-N0752-72), Digital Equipment Corporation
- *53C810 SCSI I/O Processor Data Manual*, NCR
- *53C720 SCSI I/O Processor Programmer's Guide*, NCR
- *BQ4285 Time-of-Year/NVR chip (TOY)*, Brooktree
- *PCI Local Bus Specification, Revision 2.0*, PCI Special Interest Grove, Order Number 281446-001
- *ISA Bus Specification*, IEEE Standards Office
- *8242 Keyboard Controller Specification*, Intel, PHOENIX Technologies, Ltd.

For information on the error logger within operating systems, write to Intel Corporation, Literature Sales, P.O. Box 7641, Mt. Prospect, Il 60056-7641. Request the following item: *82420/82430 PCIset ISA and EISA Bridges*, Order Number 290483-001.

Conventions

This document uses the following conventions:

Convention Example	Description
[Enter]	Square brackets around text represent a key on the keyboard.
`c:\windows`	`Monospaced` text indicates file names, path names, addresses, directories, or screen text. Each operating system has its own specific syntax.
bold text	**Bold** text is used occasionally to set off material.
italicized text	*Italicized* text is used for commands that you enter, buttons that you press, and so forth. *Italic* type is used occasionally for emphasis as well.
Addresses	1 A000 0020 Addresses are formatted with spaces (for example, 1 A000 0020h) rather than with commas.

Abbreviations

This information uses the following, commonly used abbreviations:

Abbreviation	Meaning
ASIC	application-specific integrated circuit
KByte	kilobyte
MByte	megabyte
AUI	adapter or attachment unit interface, thickwire Ethernet connection
CAS	column address strobe
CPU	central processing unit
DRAM	dynamic RAM
D-stream	data stream
ECC	error correction code
EIA	Electronics Industry Association
EID	Ethernet identification
FDC	floppy disk controller
I/O	input/output

(continued)

ISA	industry-standard architecture
I-stream	instruction stream
kbits	1024 bits
Kbytes	1000 bytes for storage; 1024 bytes for memory
kHz	kiloHertz, 1000 cycles per second
MAU	media adapter unit
Mbits	1,048,576 bits
MBytes	1,000,000 bytes for storage; 1,048,576 bytes for memory
MHz	megaHertz, 1,000,000 cycles per second
NVRAM	nonvolatile RAM
PCI	peripheral component interconnect
PLL	phase-locked loop
RAM	random access memory
RAS	row address strobe
RISC	reduced instruction set computer
ROM	read-only memory
SCSI	small computer system interconnect
SIMM	single in-line memory module
SIO	System I/O chip, Intel 87378IB PCI-ISA bridge chip *or* super I/O chip (parallel port, SLU...) NCR 97332
SRAM	static RAM
TOY	time-of-year clock chip
VCO	voltage-controlled oscillator
ZIF	zero insertion force

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Digital AlphaStation System Descriptions

Overview

Digital AlphaStation 200 Series and 400 Series systems are state-of-the-art workstations that incorporate some of the fastest microprocessors available on the market today. This chapter covers the following general topics:

- System features
- System architecture

System Features

The Digital AlphaStation 200 Series and 400 Series systems share the following characteristics:

- DECchip 21064 or 21064A Alpha architecture CPU
- DECchip 21071-AA (core logic chipset) consisting of:
  - — Cache/memory controller (one 21071-CA chip)
  - — PCI interface (one 21071-DA chip)
  - — Data path (two 21071-BA chips)
- 512 Kbytes of on-board secondary cache (15 ns SRAM)
- From 8 to 384 MBytes of RAM (70 ns DRAM), in three pairs of 128-MByte SIMM sockets
- One MByte of erasable/rewriteable nonvolatile memory (flashROM)
- 8 Kbytes of NVRAM
- Keyboard and mouse ports
- Two serial ports

- Bi-directional enhanced parallel port
- TOY clock
- Fast SCSI-2 controller for internal and external devices
- FDC for floppies and tapes
- PCI and ISA expansion slots

Table 1-1 outlines several distinctions between the AlphaStation 200 and 400 Series systems.

Table 1-1. Distinctive Features of the Digital AlphaStation 200 and 400 Series Systems

Feature	AlphaStation 200 Series System	AlphaStation 400 Series System
Enclosure	Slimline desktop	Mini-tower deskside
PCI-only slots	1	2
ISA-only slots	1 (half-height options only)	3
PCI/ISA combination slots	1*	1
Drive bays: • 3.5-inch expansion • 5.25-inch expansion	 3 (one nonaccessible) 1	 2 (one nonaccessible) 3
Ethernet LAN controller (embedded)	Yes (on riser with a socketed EID ROM)	No
Logic to support dynamic power management	Yes	No
Dedicated custom slot for 16-bit stereo audio	Yes	No

* Some versions of the AlphaStation 200 Series systems have two PCI/ISA slots.

System Unit

AlphaStation 200 Series System

Desktop Enclosure

The Digital AlphaStation 200 Series system's corporate slimline desktop low-profile enclosure houses the motherboard, I/O riser card, power supply, audio, and Ethernet options and internal peripherals.

Controls, Indicators, and Connectors

The front of the system enclosure has a small control panel featuring a reset button and two status LEDs. The reset button causes either a CPU halt or a system reset, depending on the system module jumper's (J3) setting. The status LEDs indicate power-on and disk activity.

Figures 1-1 and 1-2 and Tables 1-2 and 1-3 show and describe the front and rear views, respectively, of the Digital AlphaStation 200 Series system.

The motherboard includes eight diagnostic LEDs, which are visible through ports at the rear of the system. (These viewing ports are intended for diagnostic use by manufacturing, service personnel, and repair sites.) A stake-pin connector on the motherboard provides for an internal speaker. When a sound card is present, the internal speaker is connected to it.

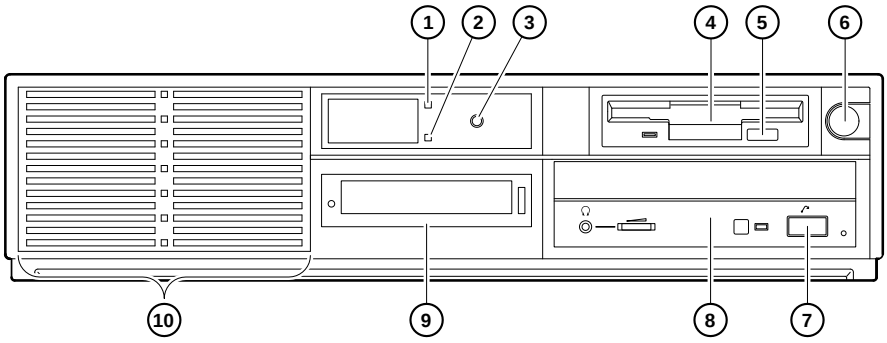


Figure 1-1. AlphaStation 200 Series Control and Indicators

Table 1-2. AlphaStation 200 Series Front Controls and Indicators

Figure Legend	Control or Indicator	Function
1	Power indicator	Power. Lights when the system is on.
2	Disk activity indicator	Hard disk drive. Lights when a hard disk drive is in use.
3	Reset button	This button resets the system and causes the self test to run.
4	Floppy drive	Location of 3.5-inch diskette drive.
5	Floppy eject button	Push to eject the floppy disk.
6	Power on/off button	Turns AC power on and off.
7	CD-ROM eject button	Opens the CD loading drawer.
8	CD drive (optional)	5.25-inch half-height front-accessible drive bay.
9	HDD drive	3.5-inch low-profile front-accessible drive bay.
10	Louvered air intake	Passageway for cooling air to enter the system. *(Do not block air intake.)*

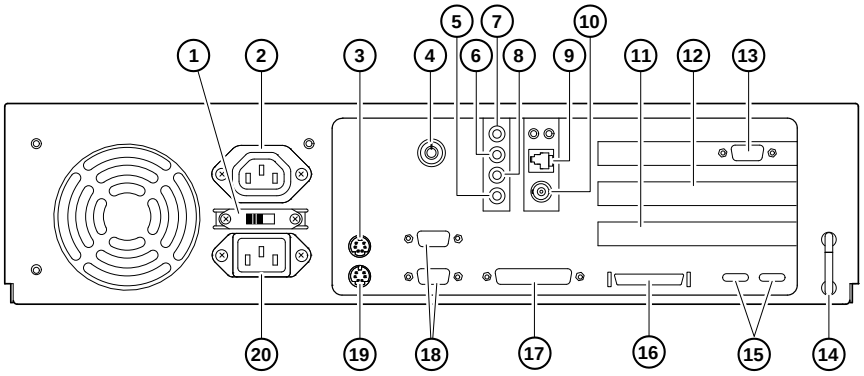


Figure 1-2. AlphaStation 200 Series Rear Connectors

Table 1-3. AlphaStation 200 Series Rear Connectors

Figure Legend	Connector	Function
1	Voltage selector switch	Allows you to set your system to work with 115-Volt or 230-Volt AC power.
2	Monitor power connector	Use to connect a monitor to AC power. *If your monitor consumes more than 2 Amps at 115 Volts(1 Amp at 230 Volts), connect it directly to your wall outlet.* This connector may be missing from future versions of the system.
3	Keyboard connector	Use to connect a 101- or 102-key keyboard.
4	System (chassis) lock	Locks top cover.
5	Sound card line in connector	Brings audio signals into the card (for example, from a stereo amplifier).
6	Sound card line out connector	Routes audio signals to an external amplifier.
7	Sound card headphone jack	Connector for the headphones or amplified speakers.
8	Sound card microphone jack	Connector for the microphone.
9	Twisted pair connector	Connection to the embedded Ethernet controller .
10	ThinWire connector	Connection to the embedded Ethernet controller .

Table 1-3. AlphaStation 200 Series Rear Connectors *(continued)*

11	ISA expansion slot	Used for half-size ISA expansion options only.
12	PCI/ISA expansion slot	Either a PCI or ISA option can use this slot.
13	PCI expansion slot	Used for PCI expansion options. (In earlier systems, this slot was a PCI/ISA combo slot. The slot was changed to PCI only to support two-board PCI options.) In this example, a PCI graphics adapter is in the slot.
14	Security loop	Attaches padlock and security cable.
15	LED viewing ports	Ports for viewing diagnostic LED indicators.
16	SCSI port	Provides the interface between the system unit and external SCSI devices.
17	Enhanced bidirectional parallel port	Connects an industry-standard parallel printer or other parallel device.
18	Serial port connectors	Connects serial devices.
19	Mouse connector	Connects a PS/2-compatible mouse.
20	AC power connector	Connects the system to AC power.

AlphaStation 400 Series System

Deskside Enclosure

The Digital AlphaStation 400 Series system is a workstation system packaged in a mini-tower deskside enclosure.

Controls Indicators, and Connectors

The front of the enclosure has a small control panel featuring a reset button and three status LEDs. The reset button causes a system reset. The top two status LEDs indicate power-on and disk activity. The lowermost status LED is unused in this system.

Figures 1-3 and 1-4 and Tables 1-4 and 1-5 show and describe the front and rear views, respectively, of the Digital AlphaStation 400 Series system.

The CPU module contains eight diagnostic LEDs. (These are not visible during normal system operation and are intended for diagnostic use only by manufacturing, service personnel, and repair sites.) A stake-pin connector on the motherboard provides for an internal speaker.

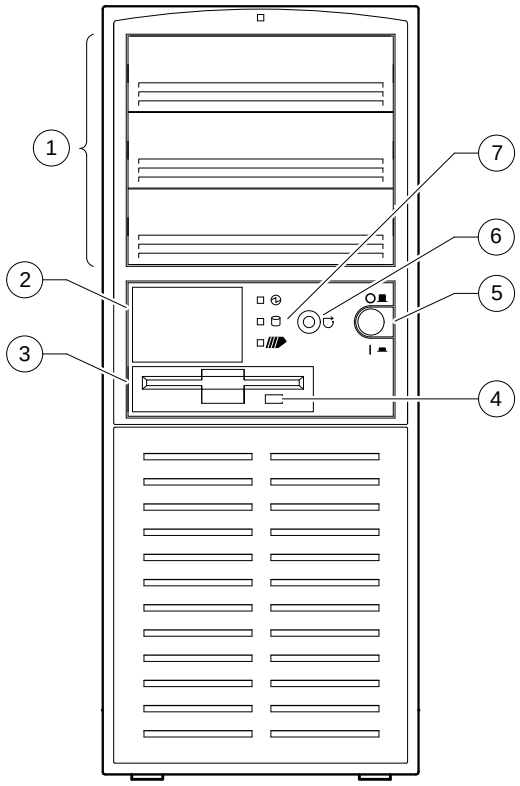


Figure 1-3. AlphaStation 400 Series Control and Indicators

Table 1-4. AlphaStation 400 Series Controls and Indicators

Figure Legend	Control or Indicator	Function
1	Drive bays	Location of three upper 5.25-inch drive bays.
2	Hard drive	Location of hidden 3.5-inch drive bay.
3	Floppy drive	Location of 3.5-inch diskette drive.
4	Floppy eject button	Releases a 3.25-inch diskette from the floppy diskette drive.
5	Power On/Off button	Turns AC power on and off.
6	Halt/Reset button	When set to Halt, this button is operating-system-specific. See your operating system documentation. When set to Reset (default), this button resets the system and causes the self test to run.
7	Indicators	Indicators from top to bottom are as follows: • Power. Lights when the system is on. • Hard disk drive. Lights when a hard disk drive is in use. • The lower indicator is not used.

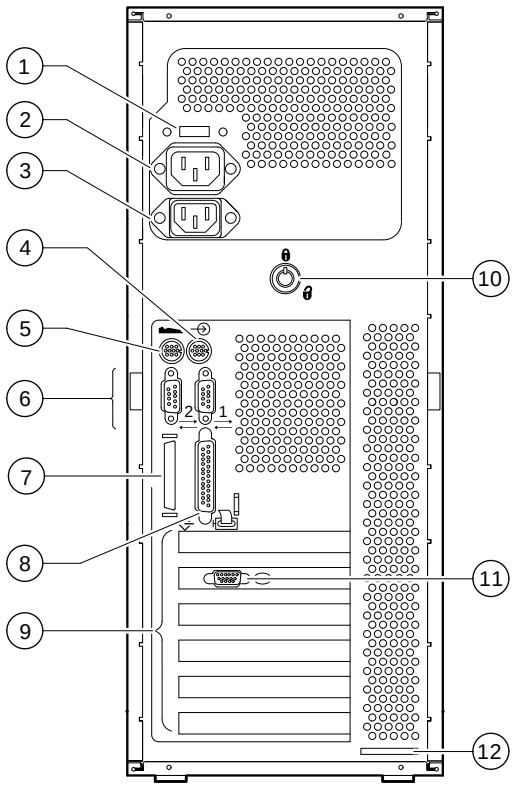


Figure 1-4. AlphaStation 400 Series Rear Connectors

Table 1-5. AlphaStation 400 Series Rear Connectors

Figure Legend	Connector	Function
1	Voltage selector switch	Allows you to set your system to work with 115-Volt or 230-Volt AC power.
2	Monitor power connector	Use to connect a monitor to AC power. *If your monitor consumes more than 2 Amps at 115 Volts(1 Amp at 230 Volts), connect it directly to your wall outlet.*
3	AC power connector	Use to connect the system to AC power.
4	Mouse connector	Use to connect a PS/2-compatible mouse.
5	Keyboard connector	Use to connect a 101- or 102-key keyboard.
6	Serial port connectors	Use to connect serial devices.
7	SCSI connector	Provides the interface between the system unit and external SCSI devices.
8	Parallel port connector	Allows you to connect an industry-standard parallel printer.
9	Expansion board slots	Allow you install up to two full-size PCI, up to three full-size ISA, and one additional PCI or ISA expansion boards.
10	System (chassis) lock	Locks outside panels.
11	Video port (on option module)	Interface between video/graphics expansion module (option) and supported monitor.
12	Security loop	Attachment point for security lock or cable.

System Architecture

Features

The DECchip 21064 (or DECchip 21064A) CPU and the 21071-AA (core logic) chipset form the core of the Digital AlphaStation 200 and 400 Series systems. A 512-Kbyte secondary cache supplements the two on-chip primary caches: one for I-stream, one for D-stream), and up to three banks of DRAM memory. The flashbus provides access to various low-speed devices such as flashROM, DROM, NVRAM, and diagnostic LEDs. An SROM bus loads power-on code from the SROM into the CPU's on-chip I-cache. The PCI bridge connects to the I/O section. Peripheral devices, including SCSI, Ethernet controllers, and an ISA bridge chip provide access to the usual set of devices (for example, audio, parallel port, two serial lines, floppy port, keyboard and mouse controller, and TOY chip).

I/O controllers connect either directly to the PCI bus or to the ISA and utility busses spawned by the PCI-ISA bridge chip. The bridge chip itself has many internal registers accessible from the PCI bus. CPU accesses to the PCI bus may be either to I/O space or to memory space. These two spaces are specified by different dedicated address spaces within the CPU's total address space and are separately decoded on the PCI bus using different values of the multifunction C/BE lines.

Figure 1-5 shows the overall system architecture for the Digital AlphaStation 200 Series system. Figure 1-6 illustrates the overall system architecture for the Digital AlphaStation 400 Series system.

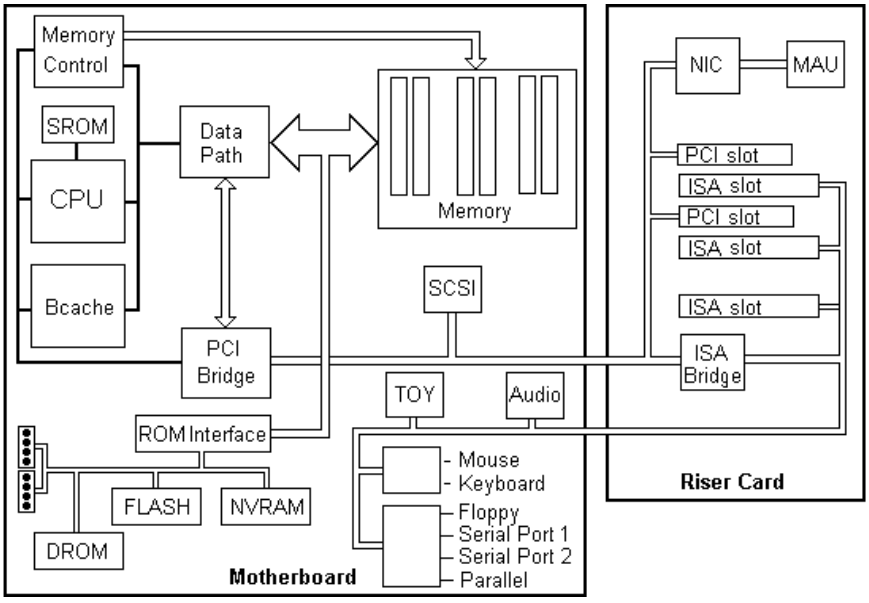


Figure 1-5. AlphaStation 200 Series System Architecture

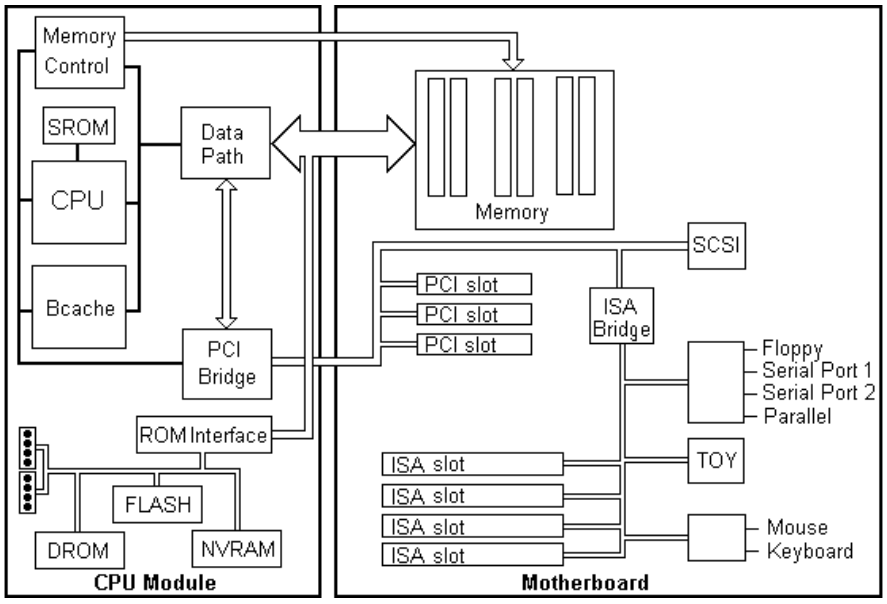


Figure 1-6. AlphaStation 400 Series System Architecture

CPU

The AlphaStation 200 Series system is designed for future variations, which you can accomplish by replacing the CPU with different, pin-compatible chips from the EV4 series and using new firmware and an IRQ PALchip to accommodate the timing changes.

The modular design of the AlphaStation 400 Series system allows for a replacement of the CPU module to increase the CPU speed and the size of the backup cache.

Depending on which Digital AlphaStation system you purchased, your system has either a DECchip 21064 or a DEChip 21064A CPU. The DECchip 21064A includes double the amount of on-chip ICache and DCache (16 KBytes each). In addition, the DECchip 21064A has a greater peak instruction execution rate. The CPU has a fully pipelined, dual-issue, 64-bit RISC architecture. Its on-chip pipelined floating point unit supports IEEE and digital formats. Forty-four translation buffers speed execution of memory-management operations. The memory data path (to the secondary cache) is 128 bits wide, with an additional 4 bits of parity.

The clock supplied to the CPU varies according to the particular system. In the 4/166 version of the Digital AlphaStation 200 Series system, the clock runs at 333 MHz; the

CPU has divide-by-two logic that converts this external clock to 166 MHz internally. This relationship is also true for the other speed variations.

Core Logic

The supporting core logic provides a cache and memory controller, data path, and a PCI bus bridge.

Cache and Memory Control

The cache and memory control (DECchip 21071-CA chip) portion of the core logic:

- Provides control for filling the Bcache and extracting victims on CPU-initiated transactions.
- Provides control for probing the Bcache on DMA transactions and invalidating the Bcache on DMA write hits.
- Provides arbitration between the CPU and the DECchip 21071-DA chip for control of the sysBus.
- Stores addresses for the four-cache-line memory write buffer.
- Controls the loading of the I/O write buffer and the DMA read buffer.
- Uses fast-page mode on the DRAMs to improve performance on DMA burst reads and memory writes.
- Controls the movement of data to and from the memory banks.
- Arbitrates between CPU requests and PCI bridge requests.
- Supports Bcache during CPU cache miss and DMA transactions.

The memory controller has control and error status registers used for reporting errors.

☞ For more information on registers, see Chapter 11, Registers.

For the Digital AlphaStation 200 and 400 Series systems, only banks zero, one, and two are used for selection of DRAM memory; bank eight is used to select the flashbus. Memory timing and addressing is determined by the values in registers in the memory control chip. Each memory bank has its own base address register, configuration register, timing register A, and timing register B.

Data Path

The data path portion of the core logic provides the path from the CPU to main memory and I/O. Two DECchip 21071-BA chips provide a 64-bit path to main memory. Included in the data path are:

- Error checking/generation on DMA-initiated transactions.
- Memory write buffer. Four entries of 32 bytes each that will be written to main memory.
- Memory read buffer. One 32-byte (a cache line) buffer used to hold data read from memory by a CPU or DMA request.
- Merge and I/O read buffer. The merge and I/O read buffer is a one-cache-line (32 Bytes), termporary holding buffer used to store data written by the CPU on memory writes or to store data read from the PCI bus on CPU reads from I/O space.
- I/O write buffer. The I/O write buffer has two entries: One entry acts as a write buffer for CPU I/O writes to the DECchip 21071-BA chip or PCI bus; the other acts as a holding buffer.
- DMA read buffer. The DMA read buffer stores data that is being read from the memory by a device on the PCI bus. This buffer is two cache lines deep and is spread across the DECchip 21071-BA chips in the system.
- DMA write buffer. The DMA write buffer stores four cache lines of PCI memory write data. Each entry is transferred to the memory write buffer after the necessary cache-coherency checks have been performed.

PCI Bridge

The PCI bridge (DECchip 21071-DA) portion of the core logic functions as the bridge between the PCI and CPU, its Bcache, and memory. The PCI bridge interface protocol is compliant with the PCI local bus. With the exception of a few pipeline registers and the parity tree, all the data path functions required to support the PCI reside in the PCI bridge.

The following list describes the major features of the PCI bridge:

- Scatter/gather mapping from the 32-bit PCI address to the 34-bit physical address, with on-chip, 8-entry translation lookaside buffer (TLB) for fast address translations. To reduce cost, the scatter/gather tables are stored in memory and are read automatically by the PCI bridge when a translation misses in the TLB.
- Supports a maximum PCI burst length of 16 longwords on PCI memory reads and writes.
- Supports two types of addressing regions on CPU-initiated transactions to PCI space.

  - Sparse space for accesses with byte and word granularities and a maximum burst length of 2.
  - Dense space for burst lengths from 1 to 8 longwords on writes and a burst length of 2 longwords on reads. This region can be used for memory-like structures such as frame buffers, which require high bandwidth accesses.
- Stores address information for the DMA write buffer and controls the loading of the DMA write buffer and I/O read buffer.
- Stores address information for the I/O write buffer and controls the unloading of the I/O write buffer and DMA read buffer.

Secondary Cache (Bcache)

The Digital AlphaStation 200 and 400 Series systems have a secondary cache to augment the CPU's primary cache. The cache has a capacity of 512 Kbytes and is organized as single-set, direct-mapped, write-back, allocate on read and, optionally, on write. The cache line size is 132 bits wide (128 data bits plus four parity bits).

The cache is not directly accessible through any special address ranges or diagnostic access modes.

Memory System

The memory system of the Digital AlphaStation 200 and 400 Series systems consists of main memory, ROM interface, NVRAM, flashROM memory, and DROM.

Main Memory

The Digital AlphaStation 200 and 400 Series main memory systems provide for up to 192 MBytes of DRAM. Additional devices on an auxiliary bus (called the "flashbus") consist of one MByte of flashROM, a 64-Kbyte DROM, an 8-Kbyte NVRAM, and jumpers.

Six industry-standard 72-pin SIMM sockets allow 70 ns DRAM memory to be added to the motherboard. When upgrading memory, you must add *pairs* of SIMMs, to make up to three banks of two SIMMs each. The SIMM sockets must be populated in pairs because the CPU memory bus width is 66 bits (64 bits of data plus two bits of parity). Each SIMM in a pair must be identical.

The Digital AlphaStation 200 and 400 Series systems support several SIMM sizes (including 33-bit versions), thereby allowing memory configurations from 8 MBytes/bank to 128 MBytes/bank, allowing maximum memory of up to 384 MBytes. Banks of different sizes may be used together, and there is no restriction on physical ordering of the SIMM pairs.

ROM Interface

The ROM interface ties the memory data bus to the flashbus. The flashbus is an auxiliary bus that supports several slower components whose access is not time critical: flashROM, NVRAM, LEDs, DROM, and two configuration jumpers. The flashbus uses two addresses in memory bank eight: one for an index register, which is used to set the offset within the flashbus address range and another for a data register used to pass information back and forth.

☞ For detailed information, see Chapter 4, I/O Programming.

The 8-bit bus allows access to 1 MByte of flashROM for console, PALcode, and diagnostics; an 8-Kbyte nonvolatile RAM (NVRAM); 8 LEDs for diagnostic display; a 64-Kbyte read-only memory (ROM) for additional diagnostic code; and 2 read-only jumpers.

NVRAM

The system provides an additional 8 Kbytes of NVRAM. The system firmware uses NVRAM to store configuration and environment variable information.

FlashROM Memory

Normally, flashROM memory is used as read-only storage for the system firmware, which is copied to main memory for execution. Under certain conditions, you can write or erase the flashROM.

There are up to four flashROM devices in the Digital AlphaStation 200 and 400 Series system module, each of which is 256 Kbytes. The SRM console and the ARC console firmware occupy the flashROM.

The contents of the flashROM devices are only changeable when the write enable jumper has been set to the flashROM write enable position.

DROM

A 64-Kbyte DROM stores power-on self test and diagnostic code. The DROM code tests concentrate on the I/O portion of the system. When the tests complete successfully, the DROM code loads the appropriate console firmware from the flashROMs. The DROM code also can load an image from a floppy diskette.

Diagnostic LEDs

Both the Digital AlphaStation 200 and 400 Series systems have 8 diagnostic LEDs. The LEDs provide an indication of initialization and POST firmware progress and errors.

In the Digital AlphaStation 200 Series system, the LEDs are mounted on the motherboard and are visible through slots in the back of the system enclosure.

In the Digital AlphaStation 400 Series system, the LEDs are mounted on the CPU module and are visible only when the left side panel is removed. Since airflow patterns required

for proper cooling are disrupted when the box is open, do not run the machine for an extended period with the side panel off.

PCI

The PCI, a 33-MHz, 32-bit-wide multiplexed address/data bus, logically connects to all the I/O devices of the Digital AlphaStation 200 and 400 Series systems. I/O controllers connect either directly to the PCI bus or to the ISA and utility busses spawned by the ISA bridge chip. The PCI interface clock speed is fixed at 33.33 MHz for a 30-ns cycle time. The theoretical maximum instantaneous burst data rate is 132 MBytes/sec.

I/O controllers connect either directly to the PCI bus or to the ISA and utility busses spawned by the ISA bridge chip. The bridge chip itself has many internal registers accessible from the PCI bus. CPU accesses to the PCI bus may be either to I/O space or to memory space. These two spaces are specified by different dedicated address spaces within the CPU's total address space and are separately decoded on the PCI bus using different values of the multifunction C/BE lines.

The PCI bridge chip (part of the core logic) acts as a bridge between the PCI bus and memory. This chip also can become a PCI bus master. It can generate all types of PCI cycles and responds to cycles initiated by devices requiring access to memory. Also, it performs translation of addresses supplied by other PCI devices acting as bus masters.

The AlphaStation 200 Series system has one PCI slot and one PCI/ISA combination slot located on the riser card. The AlphaStation 400 Series system has two PCI slots and one PCI/ISA combination slot. Combination slots can be used by either PCI or ISA options.

SCSI

Integral to the Digital AlphaStation 200 and 400 Series systems module is a fast SCSI-2 controller (NCR 53C810 controller chip). This chip connects directly to the on-board PCI bus and supports 8-bit, single-ended SCSI devices running at up to 10 MByte per second (fast SCSI). The chip offloads the CPU by executing a "Script" of commands, stored in system memory and retrieved by the SCSI controller as required.

The NCR 53C810 SCSI controller chip connects to the PCI bus.

Ethernet LAN Controller (DECchip 21040)

The AlphaStation 200 Series system has a DECchip 21040 embedded on the riser card. The chip is a single-chip master DMA Ethernet LAN controller with a direct interface to the PCI local bus. It supports full duplex, and its unique design optimally reduces the use of the host bus. A 32-byte Ethernet ID serial ROM (EID SROM) supplies the Ethernet address for the base network interface controller. The EID ROM is located on the riser card.

The DECchip 21040 is attached to through a ribbon cable to the media adapter unit (MAU). The MAU supports twisted-pair (10BASE-T) and ThinWire (10BASE2) network connections.

ISA Bridge

The ISA bridge chip (an Intel 82378IB system I/O chip, also known as the SIO) connects to the PCI bus but does not obey the normal PCI configuration rules. On power-on, it responds to PCI I/O space addresses in the range 0 to 0000.FFFFh (first 64 Kbytes) and to PCI memory space addresses 0 to 00FF.FFFFh (first 16 MBytes). Some of these addresses are decoded for use within the bridge chip, and some are for use on the ISA bus.

The ISA bridge chip (located on the riser card in the AlphaStation 200 Series system and on the motherboard in the AlphaStation 400 Series system) provides connection for the embedded ISA peripheral controllers and the ISA option slots, as well as a dedicated utility bus.

ISA Bus

The Digital AlphaStation 200 Series system has one combination PCI/ISA option slot and one ISA-only slot on the riser card. The PCI and PCI/ISA combination slots are full size; the bottom ISA-only slot is limited to half-size options. The Digital AlphaStation 400 Series system has one PCI/ISA combination slot and three ISA-only slots on the motherboard. A National 87332 Super I/O chip connects to the ISA bus to provide a floppy disk interface, two serial lines, and a parallel port.

Serial I/O

The Digital AlphaStation 200 and 400 Series system includes two asynchronous serial lines, both of which support modem control. The maximum speed is 56 kBaud. These are provided as a part of the functionality of the super I/O chip that connects to the ISA bus spawned by the ISA bridge chip. The serial ports are labeled COM1 and COM2 . You can access them by ISA addresses 3F8h through 3FFh and 2F8 through 2FFh.

Keyboard/Mouse

The Digital AlphaStation 200 Series and 400 Series systems include a standard Intel 8242 keyboard and mouse controller. The controller is accessed through the ISA bridge chip using addresses 060h and 064h.

TOY Clock

The TOY chip is the source of a periodic interrupt for the CPU. It connects to IRQ4 on the CPU chip, bypassing the bridge chip's interrupt controller.

The TOY chip also has 114 bytes of battery-supported RAM. The chip is addressed as a device on the utility bus spawned by the ISA bridge chip. It is accessed at ISA addresses 070h and 071h.

Floppy Disk Controller (FDC)

The FDC controls one or two drives; it is another section of the National PC87332 super I/O chip. You can access it through ISA addresses 3F0h through 3F7h. The floppy drive in both the Digital AlphaStation 200 and 400 Series systems consists of a low-profile 3.5-inch device.

You can connect an optional tape drive to the floppy disk bus.

NOTE

SCSI tape drives must be attached to the SCSI bus, *not* to the FDC bus.

Sound Card: Digital AlphaStation 200 Series System

The Digital AlphaStation 200 Series system has a dedicated sound card, compatible with the Microsoft Windows Sound System. The sound card is connected to the ISA bus on a private connector. Neither the connector nor the sound card is ISA-standard.

There are four user-accessible connectors available at the rear of the system enclosure. When you install a headphone jack, the internal speaker is muted for sounds originating on the sound card; the beeps and bloops from the motherboard will still go to the speaker if the TCE jumper on the sound card is installed.

The sound card also accepts audio from the CD-ROM drive. A four-pin header is provided to connect the sound card to the CD-ROM drive.

The sound card has a four-pin header where you can connect the internal speaker. Alternatively, you can plug the speaker into the motherboard connector at J15.

The sound card I/O base address is selected by use of jumpers SW1 and SW2 on the sound card (default is 530h). *Always* use ISA addresses 388h through 38Bh for the synthesizer chip.

2

Configuring Your AlphaStation System

Overview

This chapter describes how to configure the Digital AlphaStation 200 and 400 Series systems, including the following topics:

- System configurations
- Memory
- Mass storage expansion
- PCI expansion
- ISA expansion
- Jumpers

System Configurations

You can configure your Digital AlphaStation 200 or 400 Series system in various ways. Graphics are supported with a PCI or ISA option card, and you can choose from several monitors. SCSI and FDC peripherals provide mass storage and backup; *four* drive bays are provided for the AlphaStation 200 Series system; *five* drive bays are included for the AlphaStation 400 Series system. SIMM sockets allow memory configurations up to 192 MBytes.

Packaged system building blocks for both the AlphaStation 200 and 400 Series systems typically include the features shown in Table 2-1.

Table 2-1. Typical Digital AlphaStation System Configurations

System Feature	Description
Sound card	16-bit audio with headphones and microphone
Memory	32 MBytes (expandable to 192 MBytes)
SCSI disk	1.05-GByte hard drive and CD-ROM drive
Graphics option	8-plane, 2 Mpixel PCI (1280x1024 72 Hz)
Monitor	15-inch color (optional in some packages)
Ethernet	Embedded in the AlphaStation 200 Series system, DE435-AA in the AlphaStation 400 Series system
Floppy drive	1.44-MByte
Keyboard and mouse	Standard
Operating system software	Digital UNIX® and OpenVMS systems factory-installed, Windows NT Workstation ships on CD-ROM media

Memory

The AlphaStation 200 and 400 Series memory systems support up to 192 MBytes of DRAM (or 384 MBytes when 64-MByte SIMMs are available). Six industry-standard 72-pin SIMM sockets hold 70 ns DRAM memory.

Memory is added in pairs of SIMMs because of the 66-bit width of the CPU memory data bus. Each SIMM in a pair must be identical.

The use of longword parity allows the AlphaStation 200 and 400 Series systems to use either 33-bit SIMMs *or* 36-bit SIMMs.

Several SIMM sizes are supported, which allow memory configurations from 8 MBytes to 384 MBytes. If banks of different sizes are used together, there is no restriction on physical ordering of the SIMM pairs. The larger banks are initialized by the power-on code to occupy the lower addresses because the base address of each bank must be naturally aligned with its size.

Two kinds of SIMMs are supported: those with a single RAS line and those with two RAS lines. SIMMs that have two RAS lines are addressed as though they have two separate memories (that is, split bank).

The number of address lines used (RAS/CAS) varies according to the size of the SIMM. For example, Table 2-2 shows that one 1 Mx33 SIMM contains 4 MBytes. A bank with a pair of these SIMMs contains 8 MBytes, with the SIMM having one RAS line (that is, it is not a split bank).

Table 2-2. Supported SIMMs for the Digital AlphaStation

SIMM	SIMM Size	Bank Size	Split Bank (Two RAS Lines)
1 Mx33 (or 36)	4 MBytes	8 MBytes	No
2 Mx33 (or 36)	8 MBytes	16 MBytes	Yes
4 Mx33 (or 36)	16 MBytes	32 MBytes	No
8 Mx33 (or 36)	32 MBytes	64 MBytes	Yes
16 Mx33 (or 36)	64 MBytes	128 MBytes	No

Mass Storage Expansion

Internal Bay Availability: AlphaStation 200 Series Systems

The Digital AlphaStation 200 Series system enclosure has four internal mass storage bays, as Figure 2-1 and Table 2-3 show. Notice that the floppy drive is connected to the FDC, not to the SCSI bus. The system can use either an FDC or SCSI tape drive.

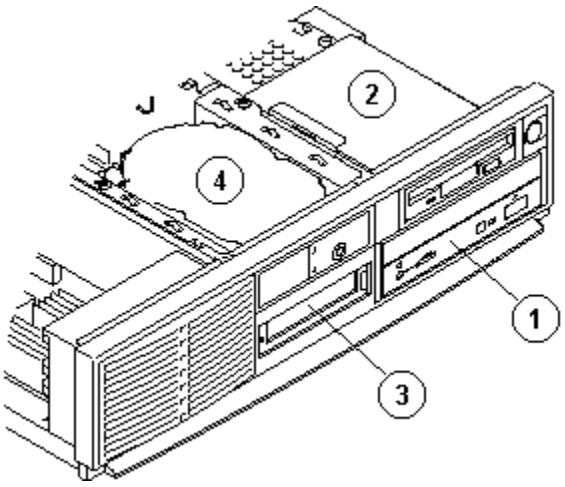


Figure 2-1. Internal Bays: AlphaStation 200 Series System

Table 2-3. Description of the AlphaStation 200 Series Internal Bays

Bay	Description
1	The outer-bay lower area can hold one 5.25-inch half-height, front-accessible or nonaccessible, storage device. Typically, this bay is used for CD drives or tape drives. Because of thermal characteristics, Digital does not support the use of hard drives in this bay.
2	The outer-bay upper area may contain the optional 3.5-inch 1.44-MByte floppy drive. The floppy disk is controlled by the floppy disk controller (FDC). The FDC controls up to two drives. You can add an FDC device, such as a tape-backup drive.
3	The inner-bay lower area can hold a 3.5-inch front-accessible or nonaccessible device. This bay would be a likely spot to place a second HDD drive.
4	The inner-bay upper area can contain a 3.5-inch nonaccessible device. Normally, the first hard disk is located here.

Internal Bay Availability: AlphaStation 400 Series Systems

The Digital AlphaStation 400 Series system enclosure has five internal mass storage bays in two areas. The Digital AlphaStation 400 Series system supports up to four SCSI devices inside the system enclosure. Figure 2-2 shows and Table 2-4 describes the internal bays.

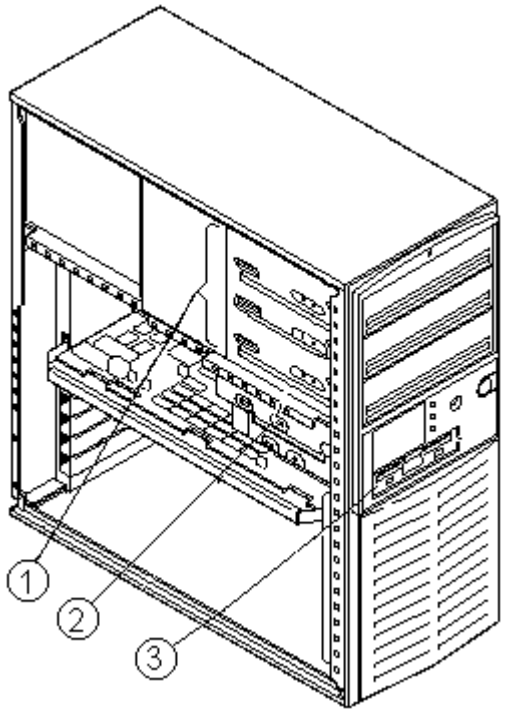


Figure 2-2. Internal Bays - AlphaStation 400 Series Systems

Table 2-4. Description of the AlphaStation 400 Series System Internal Bays

Bay	Description
1	The upper-bay area can hold three 5.25-inch half-height, front-accessible or nonaccessible storage devices.
2	The lower-bay area can hold two 3.5-inch storage devices. One is nonaccessible from the front and typically contains the first hard disk.
3	The second drive in the lower-bay area is the standard 1.44-MByte, 3.5-inch floppy diskette drive. The floppy disk is controlled by the floppy disk controller (FDC). The FDC controls up to two drives. You can add another FDC device, such as a tape-backup drive.

External SCSI Bus Expansion

A connector at the rear of the system enclosure allows for the addition of external devices. A second connector mounted on the system module allows for connection to devices internal to the system enclosure. There may be up to seven peripheral devices, which is the limit of the SCSI bus.

The total bus length, including internal cables and etch as well as the external cables between enclosures and any cables inside expansion boxes, cannot exceed 3 meters (9.8 feet) for fast SCSI operation or 4 meters (13.1 feet) for slow SCSI operation (5 Mbytes/sec).

The amount of bus length inside the Digital AlphaStation 200 Series system is 1.4 meters (4.6 feet), which leaves 1.6 meters (5.25 feet) for external cabling and wiring in expansion enclosures if the bus is used in fast mode.

The amount of bus length inside the Digital AlphaStation 400 Series system is 1.5 meters (4.9 feet), which leaves 1.5 meters (4.9 feet) for external cabling and wiring in expansion enclosures if the bus is used in fast mode.

SCSI Termination

For both systems, the SCSI bus must be terminated at both physical ends. Inside the system enclosure, the SCSI bus runs from the external SCSI connector to the SCSI controller chip and then to a connector for the internal drives. Given this, one terminator is located inside the system enclosure at the last internal drive. The other is an active terminator located on the motherboard adjacent to the external SCSI connector. The active terminator is used when no external drives are present.

NOTE

Before powering on the system box, power on all external SCSI devices.

AlphaStation 200 Series System SCSI Termination

When you add external devices, the active terminator is automatically disabled (by sensing a conductor, on external connector pin 36, grounded by the external cable). You must insert a terminator in the expansion connector of the last expansion device. (A jumper, J21, is provided for manual override.) The act of plugging the cable into the rear SCSI connector – not the presence of SCSI devices – disables the terminator.

CAUTION

Take care that no other devices added externally have their own internal terminators; there must never be more than the pair of terminators in a system, one at each physical end of the bus.

AlphaStation 400 Series System SCSI Termination

When you add external devices, you must configure the system for external termination through the console firmware. If the system is running the ARC console, go to the `Machine specific setup menu...` and select `set SCSI termination to external`. If you remove all the external SCSI devices, select `set SCSI termination to internal`. If the system is running the SRM console, type `>>>set control_scsi_term external` (or `internal` when all external SCSI devices are removed).

When external SCSI devices are attached, the last SCSI device must provide termination.

CAUTION

Take care that no other devices added externally have their own internal terminators; there must never be more than the pair of terminators in a system, one at each physical end of the bus.

SCSI IDs

The SCSI controller chip is normally assigned to device ID 7. SCSI devices should have the default ID assignments shown in Table 2-5.

Table 2-5. AlphaStation 200 /400 Series System SCSI ID Assignments

ID	Device
0	First hard disk
1	Second hard disk
4	CD-ROM
5	Tape drive
7	Host adapter

PCI Expansion

The AlphaStation 200 Series system has one PCI slot, one combination PCI/ISA slot, and one ISA slot on the riser card. The AlphaStation 400 Series system has two PCI slot, one PCI/ISA combination slot, and three ISA slots. PCI devices are automatically configured by the AlphaStation 200 and 400 Series system console firmware. Typically, the console firmware performs the tasks shown in Table 2-6.

Table 2-6. AlphaStation PCI Expansion Tasks

Task	Firmware Action
Determine what PCI devices are present.	Try to read the ID registers.
When a device is located, determine its address space requirements.	All 1's are written to its base address register. Device returns the address bits it uses set to 1's, all others are 0's.
Initialize the base registers.	Set up all base address registers in order from largest to smallest.
Determine interrupt assignments.	The SRM console uses the configuration database to first identify ISA bus IRQ assignments. It then assigns open IRQs to the PCI devices. The ARC console assigns IRQs to the PCI devices as follows: 200 Series / 400 Series IRQ10: Ethernet / PCI slot 1 IRQ15: PCI slot 1 / PCI slot 2 IRQ9: PCI slor 2 / PCI slot 3 IRQ11: SCSI / SCSI

PCI IDSEL Assignments

Embedded PCI devices and the PCI expansion slots have hardwired IDSEL assignments. The PCI controller is responsible for generating the cycles necessary to configure the PCI bus. These cycles, called *configuration cycles* (accesses to CPU addresses `1 e000.0000` through `1 fff.ff80`), must be performed after power-on because PCI devices power on with no built-in knowledge of the address ranges to which they should respond.

The first step in configuration is deciding which devices are connected to the PCI bus. Because the devices have no allotted address range at this point, they use a special mechanism for this purpose. Each device on the PCI bus has its own select input (IDSEL), each one of these is connected to a different one of PCI AD lines <31:11>, that is, a maximum of 21 devices. As part of the configuration sequence, the CPU asserts each one of these address lines in sequence looking for a DEVSEL response.

NOTE

Only a single IDSEL can be asserted in the configuration space address.

Table 2-7 shows the relationship of the IDSEL bit, PCI base address, and CPU base address in the AlphaStation 200 Series and the AlphaStation 400 Series systems.

Table 2-7. PCI AD <n> to IDSEL# Assignments

Device	IDSEL Bit	PCI Base Address	CPU Base Address
Both AlphaStation Series Systems			
SCSI	AD[17]	0002.0000	1 E006.0000
ISA Bridge	AD[18]	0004.0000	1 E007.0000
AlphaStation 200 Series System Only			
Ethernet (embedded)	AD[22]	0040.0000	1 E00B.0000
PCI Bus Slot #1	AD[23]	0080.0000	1 E00C.0000
PCI Bus Slot #2	AD[24]	0100.0000	1 E00D.0000
AlphaStation 400 Series System Only			
PCI Bus Slot #1	AD[22]	0040.0000	1 E00B.0000
PCI Bus Slot #2	AD[23]	0080.0000	1 E00C.0000
PCI Bus Slot #3	AD[24]	0100.0000	1 E00D.0000

CPU base address <20:16> represents the encoded value of the IDSEL bit to be asserted (IDSEL bits range from PCI AD<31:11>). For example, in a CPU base address of 1.e006.0000, the encoded IDSEL value is 06. Starting at PCI AD<11> and counting up 7 bits (0-6), points to PCI AD<17>, which is hardwired as an IDSEL line to the SCSI controller.

When a device is addressed using its IDSEL signal, the low eight bits of the PCI physical address generated by the CPU select one of 256 possible byte-wide registers within the device. Of these, 64 are pre-defined as a "header" region whose format is fixed for all PCI devices; the remaining 192 bytes are device-specific. Figure 2-3 shows the layout of the 64-byte header region.

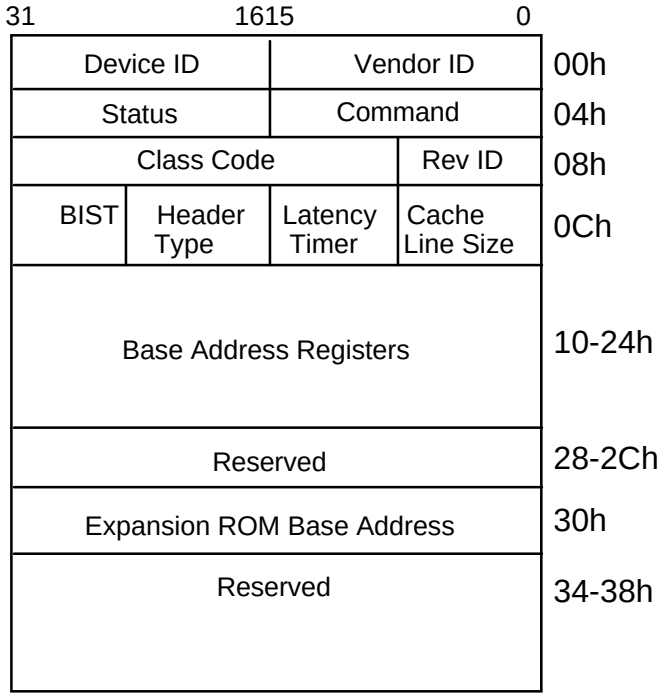


Figure 2-3. PCI Configuration Header Region

Ethernet LAN Controller Chip

The Digital DC21040 Ethernet LAN controller chip is mounted on the AlphaStation 200 Series system riser card. This chip connects to the PCI bus and allows for either a 10Base2 (Thinwire, BNC) or 10Base-T (Twisted Pair, RJ45) connection. At the rear of the system enclosure, mounted on a media adapter unit (MAU) card, are both a BNC and an RJ45 connector. (The MAU is, however, required for network connection.) The default active port is the 10Base2, a register within the Ethernet controller that allows you to select either using one of the following commands:

SRM: `set ewa0_mode twisted-pair`

- or -

`set ewa0_mode AUI`

Ethernet Identification SROM

A 32-byte EID SROM supplies the Ethernet address for the base network interface controller. Its data is accessed through the Ethernet controller. Writing to register CSR9 resets the pointer. Successive reads from CSR9 each return a byte of data in the low byte and increment the ROM pointer. Bit <31> of the returned data becomes a zero to indicate the serial transfer has taken place and that data is valid. This chip is socketed so that you can keep the same Ethernet ID when you upgrade or replace the riser card.

ISA Expansion

The AlphaStation 400 Series system has a built-in ISA device as well as slots for up to four additional ISA options. The built-in device is a Super I/O chip (National PC87332) which provides controllers for the floppy disk bus, two serial lines, and the bi-directional enhanced parallel port.

The ARC console preassigns IRQ9, 10, 11, and 15 to PCI devices for Windows NT systems. The SRM console provides the Digital UNIX and OpenVMS operating systems with an ISA configuration database. The ISACFG command maintains the database.

To avoid operating system hangs, before you add ISA options to an OpenVMS or Digital UNIX system, use ISACFG to add the new options to the configuration database. If you add an option to the system without updating the database and you boot the operating system, you could cause the system to stall. The SRM console uses the configuration database to determine PCI IRQ assignments.

NOTE

The OpenVMS operating system uses a VMS configuration file also: ISA_CONFIG.DAT. Check the OpenVMS operating system documentation for information about maintaining the contents of this file. If the SRM console does not know about an ISA option, a PCI option might inadvertently be assigned the same IRQ as the ISA option, which could result in a stalled operating system.

Use the procedure shown in Table 2-8 when adding ISA options:

Table 2-8. Procedure for Adding ISA Options

Action	Result or Next Step
1. Perform operating system configuration tasks, if any. Refer to your operating system installation guide and release notes.	The operating system is prepared for the ISA option.
2. Shut down the system.	The system is at the console prompt (>>>).
3. `>>>isacfg` *options*	Adds the new ISA option to the SRM console configuration table using the appropriate command options.
4. `>>>init`	Typing `init` incorporates the changes into the configuration database.
5. Configure the ISA option.	Use the manual that came with the ISA option to set the ISA option up to match the configuration database.
6. Turn off the system and install the ISA option.	The option is mounted in the system.
7. Turn on the system and boot.	The operating system boots and sees the new ISA option.

Jumpers

The Digital AlphaStation 200 Series and 400 Series systems use jumpers to control initialization, write enable flashROMs, and determine switch functions, clock speeds, and SCSI termination. This section describes the jumpers and their functions.

AlphaStation 200 Series System

Motherboard

The Digital AlphaStation 200 Series system motherboard has several jumpers. Figure 2-4 and Table 2-9 show and describe the motherboard jumpers.

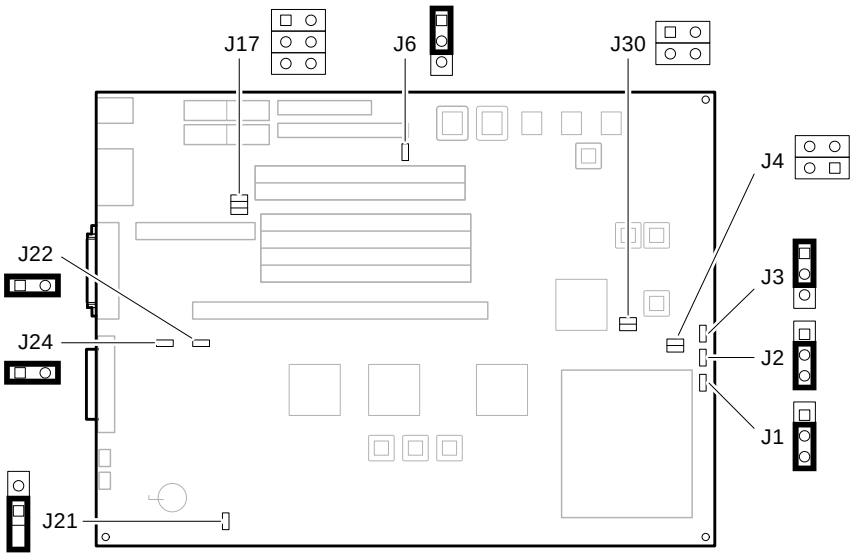


Figure 2-4. AlphaStation 200 Series System Motherboard Jumpers

Table 2-9. AlphaStation 200 Series Motherboard Jumper Locations

Jumper	Setting	Function	Description
J1	(1 to 2) (2 to 3) (D)	Mini-console. Jump to main console.	The position of J1 determines whether the SROM code goes to the SROM mini-console (for manufacturing use) or passes control to the next stage of initialization, the DROM code.
J2	(1 to 2) (2 to 3) (D)	Boot floppy. Normal (flashROM load).	The DROM code uses J2 to determine whether an image from a floppy disk or the flashROM containing the console firmware should be loaded into memory and started.
J3	(1 to 2) (D) (2 to 3)	Reset. Halt Interrupt Request.	The front-panel push button can be set to cause either a Reset or a Halt Interrupt Request.
J4	(1 to 2) and (3 to 4) Not installed (D)	PLL clock source. Oscillator clock source.	This jumper is used to select the clock source. The AlphaStation 200 Series system uses the oscillator as the clock source.
J6	(1 to 2) (D) (2 to 3)	Enables flashROM writes. Disables writes.	The J6 jumper can be used to prevent writes to the flashROMs. Typically, writes are enabled.

Table 2-9. AlphaStation 200 Series Motherboard Jumper Locations *(continued)*

Jumper	Setting	Function	Description
J17	(1 to 2) (3 to 4) (5 to 6)	Keyboard controller inputs.	All are unused.
J21	(1 to 2) Hang Off (D)	Disables sensing for presence of external cable. Enables sensing for the presence of an external SCSI cable.	J21 controls the automatic SCSI bus terminator. If an external SCSI cable is attached to the SCSI connector, the automatic SCSI terminator turns off. The SCSI bus must be terminated at the end of the external bus. When sensing is disabled (J21 1 to 2 installed), an external SCSI terminator is *required*, even if no external SCSI devices are present. If a cable is present, the SCSI bus must be terminated at the end of the external bus.
J22	(1 to 2) (D) Removed	87332 Super I/O chip. 87312 Super I/O chip.	J22 is installed when the 87332 Super I/O chip is used. This chip supports enhanced parallel port operations.
J24	(1 to 2) (D) Removed	87332 Super I/O chip. 87332 Super I/O chip.	J24 is installed when the 87332 Super I/O chip is used. This chip supports enhanced parallel port operations.
J30		To be used for future upgrades.	

(D)= Default setting.

Sound Card

The Digital AlphaStation 200 Series system sound card uses three jumpers to control the motherboard beeps and the I/O address assignment. Figure 2-5 and Table 2-10 show these jumpers and describe their functions.

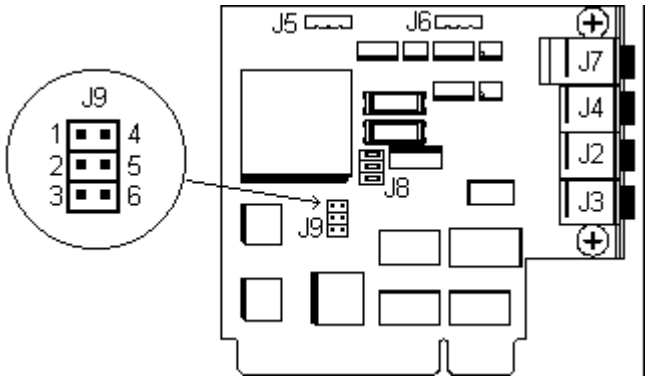


Figure 2-5. AlphaStation 200 Series System Sound Card Jumpers

Table 2-10. AlphaStation 200 Series System Sound Card Jumper Descriptions

Jumper	Setting	Description
J9	1 to 4 IN (D) 1 to 4 OUT	Motherboard beeps sent to speaker. Motherboard beeps ignored.
J9	2 to 5 *and* 3 to 6 OUT OUT OUT IN IN OUT IN IN (D)	Base Address: x604 xF40 xE80 x530

The J9 (1 to 4) jumper, timer counter enable (TCE), connects the timer-counter circuit from the motherboard to the mixer that drives the speaker header. Install this jumper to drive motherboard sound to the speaker connector. The motherboard sound is not mixed into the headphone output or the line out.

AlphaStation 400 Series System

Motherboard

The Digital AlphaStation 400 Series system motherboard has several jumpers, most of which are not used in this system. Figure 2-6 and Table 2-11 show and describe the motherboard jumpers.

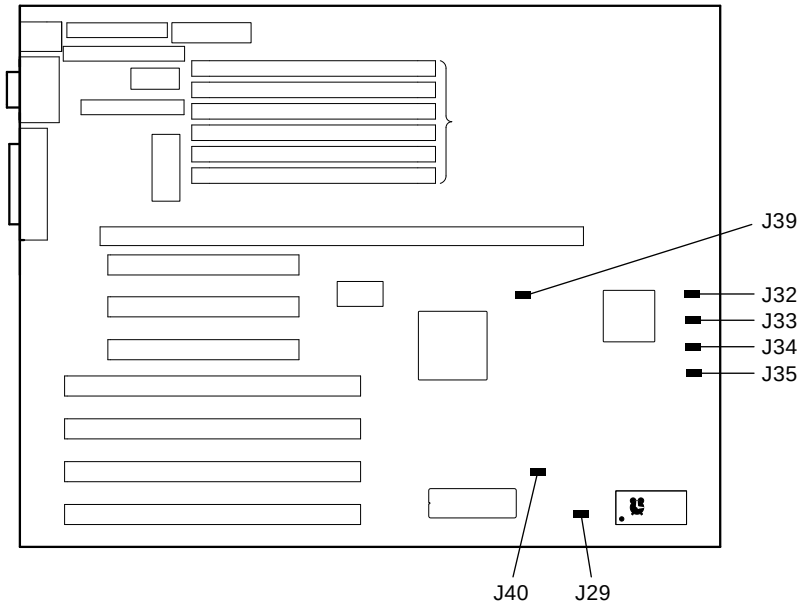


Figure 2-6. AlphaStation 400 Series Motherboard Jumpers

Table 2-11. AlphaStation 400 Series Motherboard Jumpers

Jumper	Setting	Function	Description
J29	1 to 2 2 only (D)	CMOS clear Normal	CMOS clear
J32	1 to 2 2 only (D)	Password clear Normal	Password clear (not used on the AlphaStation 400 system)
J33	1 to 2 2 only (D)	Color Mono	Display type (not used on the AlphaStation 400 system)
J34	1 to 2 2 only (D)	Recovery mode Normal	Recovery mode (not used on the AlphaStation 400 system)
J35	1 to 2 (D) 2 only	Enabled Disabled	BIOS upgrade (not used on the AlphaStation 400 system)
J39	1 to 2 (D) 2 only	Alpha architecture Unsupported	CPU selection
J40	1 to 2 (D) 2 to 3	Disabled Enabled	Reprogram boot block (not used on the AlphaStation 400 system)

(D) = Default position.

CPU Module

The Digital AlphaStation 400 Series system PB50C-BA CPU module contains jumpers that provide firmware-related information and determine the front-panel push-button function. Figure 2-7 and Table 2-12 show and describe the PB50C-BA CPU module jumpers.

Figure 2-7. AlphaStation 400 Series PB50C-BA CPU Module Jumpers

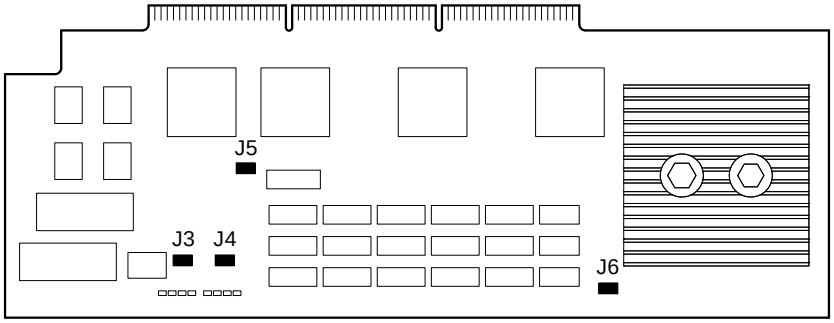


Table 2-12. AlphaStation 400 Series PB50C-BA CPU Module Jumper Descriptions

Jumper	Pins	Function	Description
J3	1 to 2	Mini-console	The position of J3 determines whether the SROM code goes to the SROM mini-console (for manufacturing use) or passes control to the next stage of initialization, the DROM code.
	2 to 3 **(D)**	Jump to main console	
J4	1 to 2 **(D)**	Enables flashROM writes	The J4 jumper can be used to prevent writes to the flashROMs.
	2 to 3	Disables writes	Typically, writes are enabled.
J5	1 to 2	Boot floppy	The DROM code uses J5 to determine whether an image from a floppy disk or the flashROM containing the console firmware should be loaded into the memory and started.
	2 to 3 **(D)**	Normal (flashROM load)	
J6	1 to 2 **(D)**	Reset	The front-panel push button is set to cause a Reset when pressed.
	2 to 3	Not supported	

3
Addressing

Overview

This chapter covers addressing for the Digital AlphaStation 200 and 400 Series systems, including the following topics:

- Address diagram
- Cacheable memory space
- Noncacheable memory space
- PCI sparse memory space
- PCI dense memory space

CPU-initiated accesses to the PCI bus can be either to PCI I/O space or to PCI memory space. These two spaces are specified by different dedicated address spaces within the CPU's total address space and are decoded separately on the PCI bus using different values of the multifunction C/BE lines.

Address Diagram

The Digital AlphaStation 200 and 400 Series system CPUs use 34 bits to address physical address space. The physical address space is divided into the areas shown in Figure 3-1.

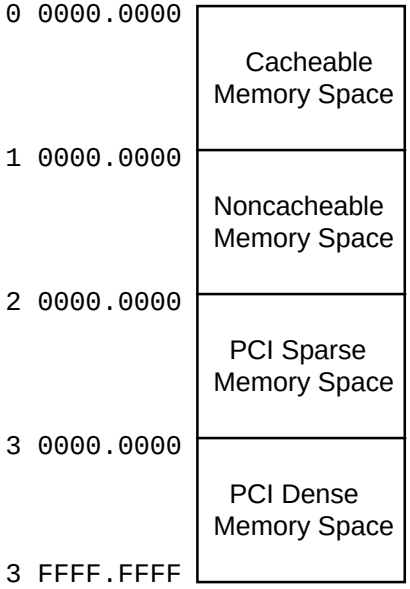


Figure 3-1. Physical Address Space

Cacheable Memory Space: 0 0000.0000-0 FFFF.FFFF

Memory addressing is set up during power-on initialization to start at address 0 0000.0000 and to occupy a contiguous address range. The highest memory address possible on a Digital AlphaStation 200 or 400 Series system is 0 17FF.FFFF (384 MBytes), as Figure 3-2 shows. Currently, the memory system can use up to six 32-MByte SIMMs for a total memory size of 192 MBytes.

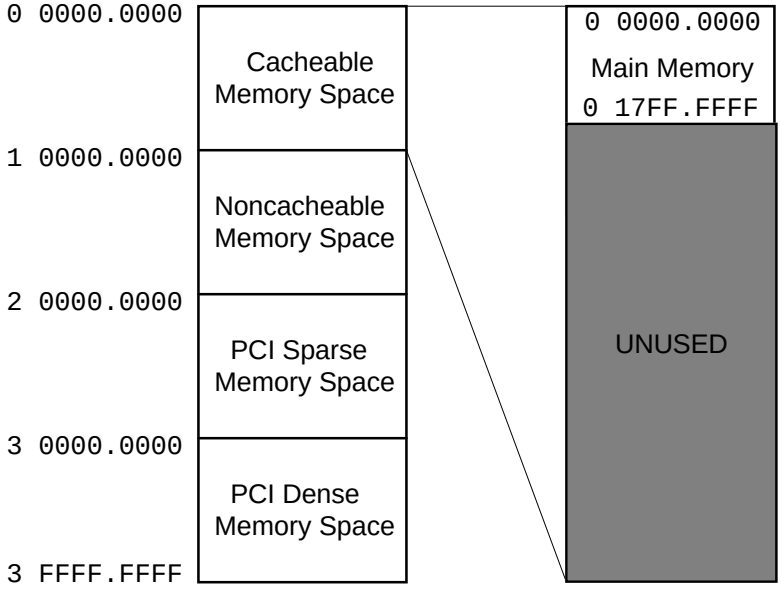


Figure 3-2. Cacheable Memory Space

Noncacheable Memory Space:1 0000.0000-1 FFFF.FFFF

Figure 3-3 shows the major areas of the noncacheable address space. The cache/memory controller responds to read/write accesses in the first two GByte of noncacheable space. (The Bcache is bypassed.) The other two GBytes of space are used for CSRs and PCI functions.

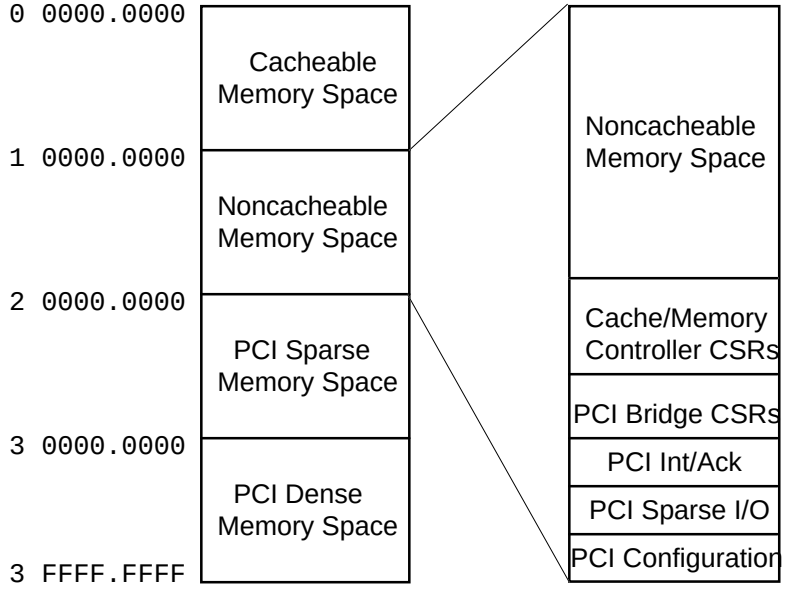


Figure 3-3. Noncacheable Address Space

First Two GBytes of Noncacheable Space

Table 3-1 shows the items located in the first two GBytes of noncacheable space. The flashbus registers are used to create a window through which to access the flashROMs, NVROM, DROM, and LEDs.

Table 3-1. Noncacheable Memory: First Two GBytes

Address	Description
1 0000.0000	Flashbus index register
1 0010.0000	Flashbus data register

Cache/Memory Controller

The cache/memory controller portion of the core logic uses some of the space in the second two GBytes of noncacheable space for its CSRs. Table 3-2 shows the CSR names and addresses.

☞ For more information, refer to *DECchip 21071/21072 Core Chip Sets Data Sheet*, order number EK-N0648-72.

Table 3-2. Cache Memory Controller Registers

Address	Description
1 8000.0000	General control register
1 8000.0040	Error and diagnostic status register
1 8000.0060	Tag enable register
1 8000.0080	Error low address register
1 8000.00A0	Error high address register
1 8000.00C0	LDx_L low address register
1 8000.00E0	LDx_L high address register
1 8000.0200	Global timing register
1 8000.0220	Refresh timing register
1 8000.0240	Video frame pointer register
1 8000.0260	Presence detect low data register
1 8000.0280	Presence detect high data register
1 8000.0800	Bank 0 base address register
1 8000.0820	Bank 1 base address register
1 8000.0840	Bank 2 base address register
1 8000.0860	Bank 3 base address register
1 8000.0880	Bank 4 base address register
1 8000.08A0	Bank 5 base address register
1 8000.08C0	Bank 6 base address register
1 8000.08E0	Bank 7 base address register
1 8000.0900	Bank 8 base address register
1 8000.0A00	Bank 0 configuration register
1 8000.0A20	Bank 1 configuration register
1 8000.0A40	Bank 2 configuration register

Table 3-2. Cache Memory Controller Registers (*continued)*

Address	Description
1 8000.0A60	Bank 3 configuration register
1 8000.0A80	Bank 4 configuration register
1 8000.0AA0	Bank 5 configuration register
1 8000.0AC0	Bank 6 configuration register
1 8000.0AE0	Bank 7 configuration register
1 8000.0B00	Bank 8 configuration register
1 8000.0C00	Bank 0 timing register A
1 8000.0C20	Bank 1 timing register A
1 8000.0C40	Bank 2 timing register A
1 8000.0C60	Bank 3 timing register A
1 8000.0C80	Bank 4 timing register A
1 8000.0CA0	Bank 5 timing register A
1 8000.0CC0	Bank 6 timing register A
1 8000.0CE0	Bank 7 timing register A
1 8000.0D00	Bank 8 timing register A
1 8000.0E00	Bank 0 timing register B
1 8000.0E20	Bank 1 timing register B
1 8000.0E40	Bank 2 timing register B
1 8000.0E60	Bank 3 timing register B
1 8000.0E80	Bank 4 timing register B
1 8000.0EA0	Bank 5 timing register B
1 8000.0EC0	Bank 6 timing register B
1 8000.0EE0	Bank 7 timing register B
1 8000.0F00	Bank 8 timing register B

PCI Bridge Registers

Table 3-3 shows the PCI bridge register addresses that are located in the second half of the noncacheable space.

Table 3-3. PCI Bridge Register Addresses

Address	Description
1 A000.0000	Diagnostic control and status register
1 A000.0020	PCI error address register
1 A000.0040	SysBUS error address register
1 A000.0060	Dummy register 1
1 A000.0080	Dummy register 2
1 A000.00A0	Dummy register 3
1 A000.00C0	Translated base 1 register
1 A000.00E0	Translated base 2 register
1 A000.0100	PCI base 1 register
1 A000.0120	PCI base 2 register
1 A000.0140	PCI mask 1 register
1 A000.0160	PCI mask 2 register
1 A000.0180	Host address extension register 0
1 A000.01A0	Host address extension register 1
1 A000.01C0	Host address extension register 2
1 A000.01E0	PCI master latency timer register
1 A000.0200	TLB tag 0 register
1 A000.0220	TLB tag 1 register
1 A000.0240	TLB tag 2 register
1 A000.0260	TLB tag 3 register
1 A000.0280	TLB tag 4 register
1 A000.02A0	TLB tag 5 register
1 A000.02C0	TLB tag 6 register
1 A000.02E0	TLB tag 7 register
1 A000.0300	TLB data 0 register
1 A000.0320	TLB data 1 register

Table 3-3. PCI Bridge Register Addresses (*continued)*

Address	Description
1 A000.0340	TLB data 2 register
1 A000.0360	TLB data 3 register
1 A000.0380	TLB data 4 register
1 A000.03A0	TLB data 5 register
1 A000.03C0	TLB data 6 register
1 A000.03E0	TLB data 7 register
1 A000.0400	TLB invalidate-all register

PCI Sparse I/O Space

The core logic generates PCI I/O cycles for all accesses in the CPU address range 1 C000.0000 through 1 DFFF.FFFF. The CPU has no addressing modes that permit direct access to bytes or combinations of bytes, other than aligned four-byte entities (longwords) on the PCI bus. Therefore, an encoding scheme of certain low-order address bits is used to allow direct byte, word (two contiguous bytes) and tri-byte (three contiguous bytes) accesses. This is sometimes called *sparse-space addressing*. The PCI byte enables are driven out on the four multifunction PCI bus lines CBE#[3:0].

By using some of the low-order address bits in this way, you cannot generate a full 32-bit PCI address from the CPU address alone: Only 22 bits of CPU-supplied address are available for passing to the PCI bus; CPU address bits A<28:7> generate PCI address bits AD<23:2>. A field within the Host Address Extension (HAXR2) Register allows this address to be extended to a full 32 bits. The 16-MByte region the CPU can access is further subdivided so that accesses to the first 256 Kbytes (CPU address bits A<28:23> = zero) ignore the HAXR2 bits and treat them as all zero. Thus the PCI space accessible is a 256-Kbyte region that always starts at PCI physical address zero, referenced when CPU address bits A<28:23> are zero and a 16-MByte region whose address is formed by concatenating the CPU-supplied 22 bits of address with the 6 bits of the HAXR2 when CPU address bits A<28:23> are nonzero.

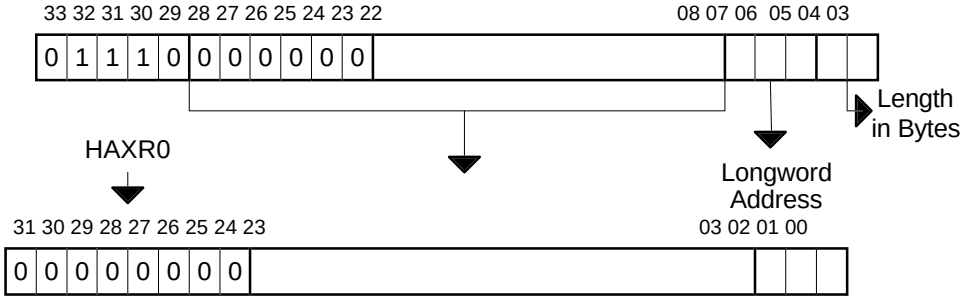


Figure 3-4. PCI Sparse I/O Space Translation (Lower 256 KBytes)

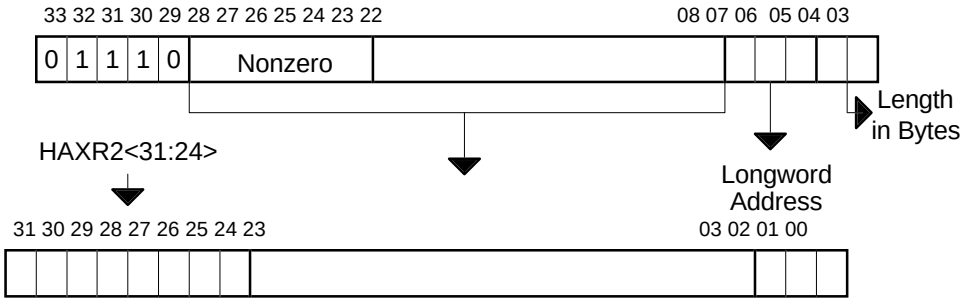


Figure 3-5. PCI Sparse I/O Address Translation (Remaining 16 MBytes)

The address bit encoding for byte selection is shown in Table 3-4.

Table 3-4. PCI Sparse I/O Space Byte Selection

CPU A<6:5>	CPU A<4:3>	PCI CBE#<3:0>	PCI AD<2>	PCI AD<1:0>	Transfer Type
00	00	1110	A<7>	00	Byte
01	00	1101	A<7>	01	Byte
10	00	1011	A<7>	10	Byte
11	00	0111	A<7>	11	Byte
00	01	1100	A<7>	00	Word
01	01	1101	A<7>	01	Word
10	01	0011	A<7>	10	Word
00	10	1000	A<7>	00	Tri-byte
01	10	0001	A<7>	01	Tri-byte
00	11	0000	A<7>	00	Longword
11	11	0000	0	00	Quadword

Figure 3-6 shows some of the devices that are accessed through PCI sparse address space.

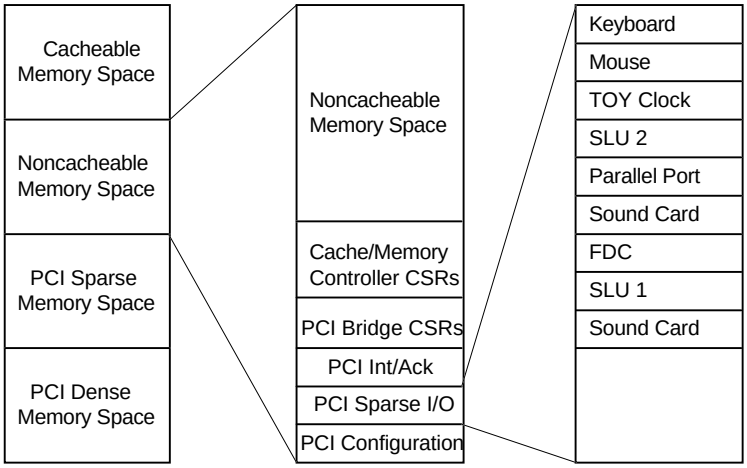


Figure 3-6. PCI Sparse Address Space

Embedded ISA Device Addresses

Table 3-5 shows the ISA device addresses and the equivalent PCI and CPU addresses for the standard embedded ISA devices.

Table 3-5. Embedded ISA Device Addresses

Device/Register	ISA Address	PCI Address	CPU Address
Keyboard	060	0000.0060	1 C000.0C00
Mouse	064	0000.0064	1 C000.0C80
TOY Clock	070	0000.0070	1 C000.0E00
	071	0000.0071	1 C000.0E20
Serial Port 1			
RCVBUFF/XMITHOLD	03F8	0000.03F8	1 C000.7F00
Int Enable	03F9	0000.03F9	1 C000.7F20
Int Ident	03FA	0000.03FA	1 C000.7F40
Line Control	03FB	0000.03FB	1 C000.7F60
Modem Control	03FC	0000.03FC	1 C000.7F80
Line Status	03FD	0000.03FD	1 C000.7FA0
Modem Status	03FE	0000.03FE	1 C000.7FC0
Scratch Pad	03FF	0000.03FF	1 C000.7FE0
Serial Port 2			
RCVBUFF/XMITHOLD	02F8	0000.02F8	1 C000.5F00
Int Enable	02F9	0000.02F9	1 C000.5F20
Int Ident	02FA	0000.02FB	1 C000.5F40
Line Control	02FB	0000.02FC	1 C000.5F60
Modem Control	02FC	0000.02FD	1 C000.5F80
Line Status	02FD	0000.02FA	1 C000.5FA0
Modem Status	02FE	0000.02FE	1 C000.5FC0
Scratch Pad	02FF	0000.02FF	1 C000.5FE0
Parallel Port			
Data Register	0378	0000.0378	1 C000.6F00
Status Register	0379	0000.0379	1 C000.6F20
Control Register	0380	0000.0380	1 C000.7000

Table 3-5. Embedded ISA Device Addresses (*continued*)

Device/Register	ISA Address	PCI Address	CPU Address
FDC			
Digital Output Register	03F2	0000.03F2	1 C000.7E40
Tape Drive Register	03F3	0000.03F3	1 C000.7E60
Main Status Register	03F4	0000.03F4	1 C000.7E80
Data Rate Select	03F4	0000.03F4	1 C000.7E80
FIFO Data Register	03F5	0000.03F5	1 C000.7EA0
Digital Input Register	03F7	0000.03F7	1 C000.7EE0
Configuration Control Register	03F7	0000.03F7	1 C000.7EE0

AlphaStation 200 Series System Sound Card

Jumpers select the sound card I/O base address for the AlphaStation 200 Series system. Table 3-6 shows the four possible sound card I/O address and the PCI and CPU address for each one. The synthesizer portion of the sound card always uses addresses 388h - 38Bh.

Table 3-6. AlphaStation 200 Series System Sound Card I/O Addresses

ISA I/O Base Address	PCI Address	CPU Address
604h	0000.0604	1 C000.C080
F40h	0000.0F40	1 C001.E800
E80h	0000.0E80	1 C001.D000
530h	0000.0530	1 C000.A600

Configuration Cycles

Configuration cycles are generated on the PCI bus when accesses are made to CPU addresses 1 E000.0000 through 1 FFFF.FF80.

The two low-order PCI address bits, AD<1:0>, are supplied from HAXR2<1:0>. The address bit encoding for byte selection is shown in Table 3-7.

NOTE

PCI address bit AD<2> is a copy of the CPU address bit A<7> except for a quadword access, when it is always zero. Values of CPU address bits A<6:3> not shown in Table 3-7 are illegal and produce unpredictable results.

Table 3-7. PCI Configuration Cycle Byte Selection

CPU A<6:5>	CPU A<4:3>	PCI CBE#<3:0>	PCI AD<2>	Transfer Type
00	00	1110	A<7>	Byte
01	00	1101	A<7>	Byte
10	00	1011	A<7>	Byte
11	00	0111	A<7>	Byte
00	01	1100	A<7>	Word
01	01	1001	A<7>	Word
10	01	0011	A<7>	Word
00	10	1000	A<7>	Tri-byte
01	10	0001	A<7>	Tri-byte
00	11	0000	A<7>	Longword
11	11	0000	0	Quadword

PCI Sparse Memory Space

The core logic generates PCI memory cycles for all accesses in the CPU address range 2 0000.0000 through 2 FFFF.FFFF as Figure 3-7 shows.

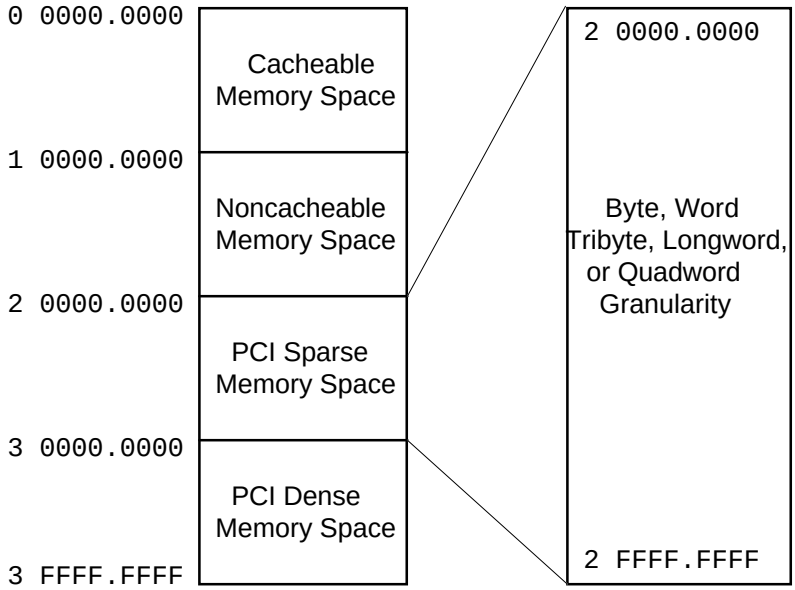


Figure 3-7. PCI Sparse Memory Space

Similar to PCI sparse I/O space, this sparse memory address space uses a complex scheme to derive byte enables from the CPU address. CPU address bits A<2:0> are ignored; A<7:3> are used to create byte masks and a longword offset;A<28:8> become PCI address bits AD<23:3>. (See Table 3-8.) For the low 16 MBytes in this CPU address space (A<31:29> is zero), the high PCI address bits AD<31:24> are zero.

For CPU addresses above the low 16 MBytes in the PCI sparse memory space (A<31:29> nonzero), PCI address bits AD<31:27> are supplied by HAXR1<31:27> and AD<26:24> are copied from CPU address A<31:29>. See Figures 3-8 and 3-9.

Table 3-8. PCI Sparse Memory Space Byte Selection

CPU A<6:5>	CPU A<4:3>	PCI CBE#<3:0>	PCI AD<2>	Transfer Type
00	00	1110	A<7>	Byte
01	00	1101	A<7>	Byte
10	00	1011	A<7>	Byte
11	00	0111	A<7>	Byte
00	01	1100	A<7>	Word
01	01	1001	A<7>	Word
10	01	0011	A<7>	Word
00	10	1000	A<7>	Tri-byte
01	10	0001	A<7>	Tri-byte
00	11	0000	A<7>	Longword
11	11	0000	0	Quadword

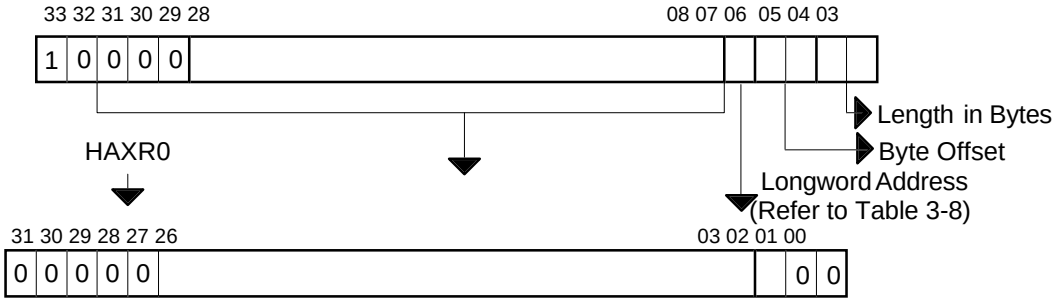


Figure 3-8. PCI Memory Space Address Translation (Lower 16 MBytes)

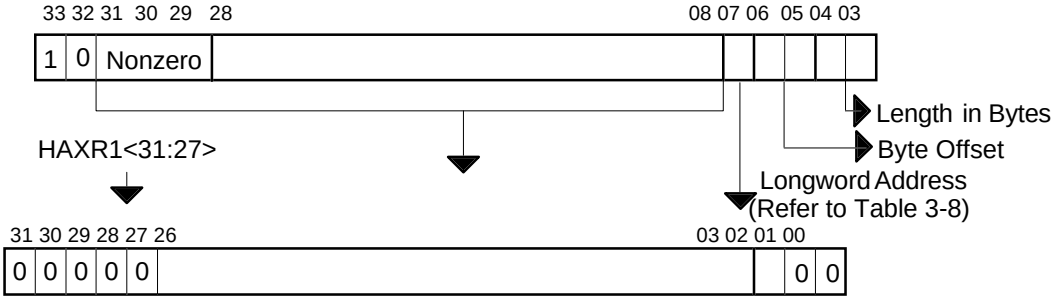


Figure 3-9. PCI Memory Space Address Translation (Remaining 112 MBytes)

PCI Dense Memory Space

To access PCI dense memory space, use addresses 3 0000.0000 though 3 FFFF.FFFF in the CPU's address space, as Figure 3-10 shows.

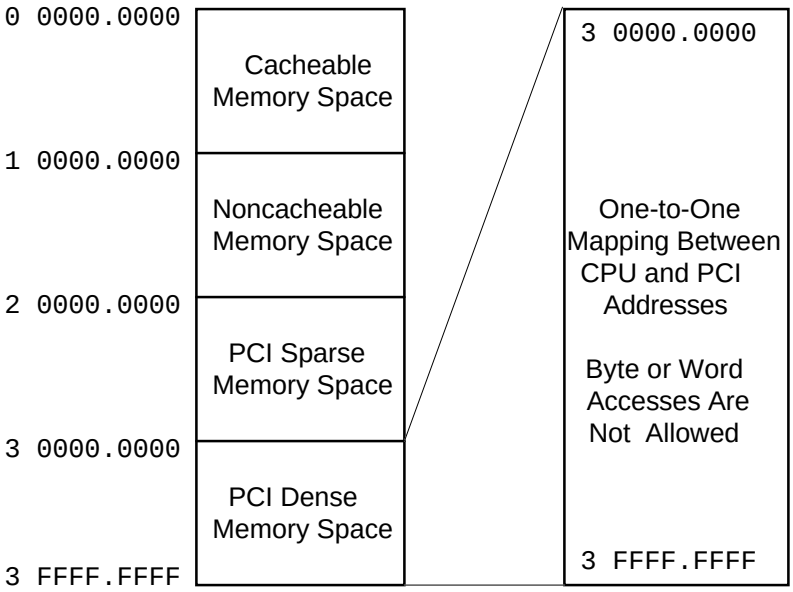


Figure 3-10. PCI Dense Memory Space

PCI dense memory space is typically used for data buffers on the PCI and has the following characteristics:

- There is a one-to-one mapping between CPU addresses and PCI addresses. A longword address from the CPU maps to a longword on the PCI. (This accounts for the the name *dense space*, as opposed to PCI sparse memory space.)
- Byte or word accesses are not allowed in this space. Minimum access granularity is longword. The maximum transfer length implemented by the core logic chipset is a cache line (32 bytes) on writes and a quadword on reads.

- Read prefetching is allowed in this space; extra reads have no side effects. The CPU does not specify a longword address on read transactions; it only specifies a quadword address. Therefore, reads in this space are always done as a quadword read with a burst length of two on the PCI.

Addresses are generated in dense space as follows:

CPU address A<31:5> is directly sent out on PCI address bits AD<31:5>.

On read transactions, PCI address AD<4:3> is generated from cpuCWMask<1:0>, PCI address <2> is always 0.

On write transactions, PCI address <4:2> is generated from cpuCWMask<7:0>. If the lower longword is to be written, PCI address <2> is 0; if the lower longword is masked out and the upper longword is to be written, PCI address <2> is 1. The number of longwords written on the PCI is directly obtained from cpuCWMask<7:0>. Any combination of cpuCWMask<7:0> is allowed by the core logic chipset.

NOTE

If the cache line written by the processor has holes, that is, if some of the longwords have been masked out, the corresponding transfer is still performed on the PCI with disabled byte enables. Downstream bridges must be able to deal with completely disabled byte enables on the PCI during write transactions.

I/O Device View of I/O Space

Figure 3-11 shows address space from the I/O perspective.

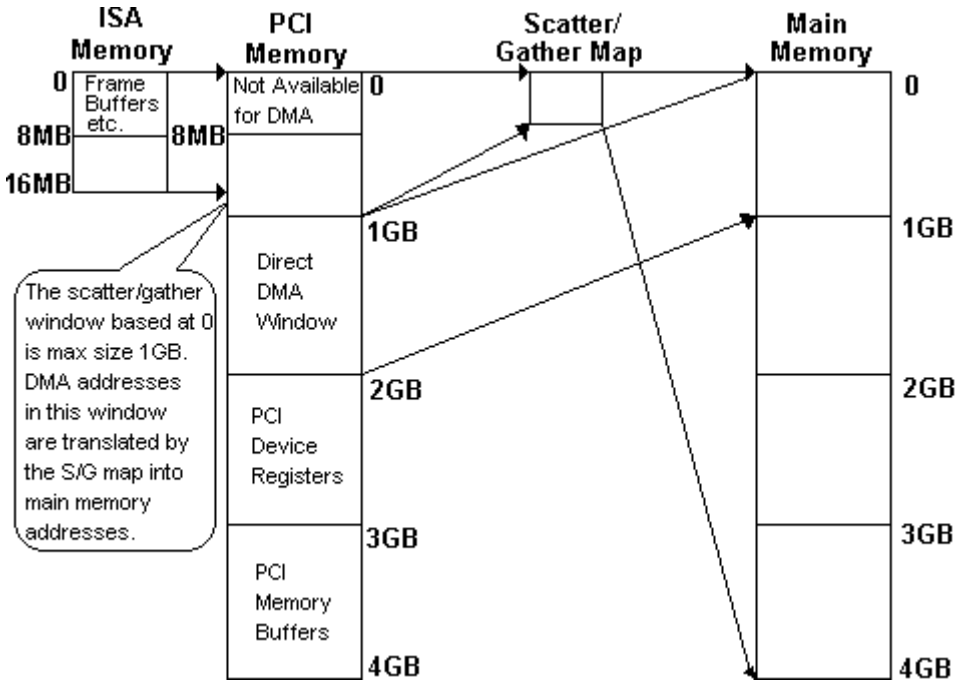


Figure 3-11. Address Space from the I/O Perspective

4

I/O Programming

Overview

This chapter covers unique areas of I/O programming for the Digital AlphaStation 200 and 400 Series systems, including:

- Accessing flashbus devices
- Keyboard and mouse controller
- TOY
- Super I/O chip
- Disabling interrupts

Accessing Flashbus Devices

On the Digital AlphaStation 200 and 400 Series systems, the flashROM, NVRAM, DROM, LEDs, and two jumpers reside on the flashbus. The cache and memory control portion of the core logic does not contain a function specifically for accessing the flashbus; therefore, bank 8 of the memory interface is used. The base of bank 8 is programmed to noncacheable memory space by SROM code.

Two addresses (1 0000.0000 and 1 0010.0000) are used to transfer data to and from devices on the flashbus. Figure 4-1 and Table 4-1 describe the index register, and Figure 4-2 and Table 4-2 describe the data register. The index register is write-only; you must access it as a longword. (The behavior of access to flashbus addresses anywhere other than those shown is undefined.)

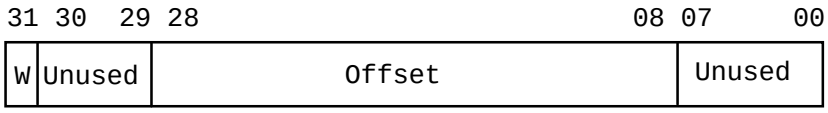


Figure 4-1. Flashbus Index Register

Table 4-1. Flashbus Index Register Bit Descriptions

Bits	Function
<31>	Write harbinger: Set to 1 if flashbus write is intended. Set to 0 is flashbus read is intended.
<30:29>	Unused.
<28:8>	Flashbus device offset address.
<7:0>	Unused.

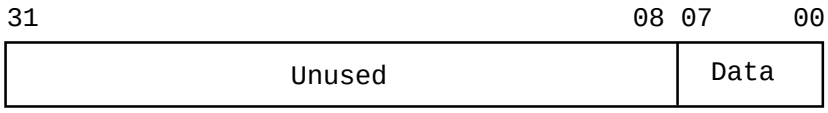


Figure 4-2. Flashbus Data Register

Table 4-2. Flashbus Data Register Bit Descriptions

Bits	Function
<31:8>	Unused
<7:0>	Flashbus device data

Flashbus Offsets

Table 4-3 lists the flashbus offsets for the Digital AlphaStation 200 and 400 Series systems.

Table 4-3. Flashbus Device Offset Addresses

Offset Address	Access	Device
00.0000 - 03.FFFF	r/w	FlashROM 0 *(optional)*
04.0000 - 07.FFFF	r/w	FlashROM 1 *(optional)*
08.0000 - 0B.FFFF	r/w	FlashROM 2 *(optional)*
0C.0000 - 0F.FFFF	r/w	FlashROM 3 *(optional)*
10.0000 - 10.3FFF	r/w	Nonvolatile RAM (NVR)
14.0000	w	LEDs
18.0000 - 18.FFFF	r	Diagnostic ROM (DROM)
1C.0000	r	Jumpers

Each device occupies a quarter-megabyte of the flashbus offset address space. If the device does not require the entire space (for example, the NVRAM uses only 8 Kbytes), then the address wraps and there appear to be multiple copies of the device. This feature is not guaranteed, and software should use only the specified offsets for each device.

Access Procedure

You can use the following procedures for *writing* and *reading* to access flashbus devices.

To write to a flashbus device :

1. Write a longword to the index register, 1 0000.0000, containing the following data: the device offset/address in bits <28:8> and the write harbinger bit <31>.
2. Write a longword to data register, 1 0010.0000, containing a byte of data in bits <7:0> to be transferred to the flashbus device.

For example, to write a 1 into the second location of the NVR, deposit 1000.0100 into the index register and 0000.0001 into the data register. Data register bits <31:8> are ignored.

NOTES

a. The contents of the flashROM devices are changeable only when you have set the Write Enable jumper to the write enable position.

b. When writing the flashROM memory, you must meet specific timing requirements by program delays and procedures. Refer to the appropriate flashROM specification for details.

To read from a flashbus device :

1. Write a longword to index register, 1 0000.0000, containing the device offset in bits <28:8>. Make sure bit <31>, the write harbinger bit is clear.
2. Read a longword from data register. The data from the addressed flashbus device is returned in bits <7:0>. Bits <31:8> are undefined.

For example, to read the second location of the NVR, first deposit 1000.0100 into the index register and then read the data register.

NOTE

To ensure proper sequencing of the accesses to the flashbus index and data registers, which could be merged or performed out of order due to write buffering in the core logic, the index register must be read after it is written. Additionally, on a write operation, the data register must be read after it is written. *The data returned for these extra reads is meaningless.* Ensure, however, that the compiler does not remove them.

Keyboard and Mouse Controller

The keyboard and mouse controller functions as follows:

1. The system writes commands to ISA port 60h and the data associated with the command to port 60h.
2. ISA addresses 60h and 64h map into CPU sparse I/O addresses 1 C000.0C00h and 1 C000.0C80h.
3. The system reads all auxiliary device and keyboard data at port 60h.
4. The system reads the 8042 status at port 64h.
5. Keyboard commands and data are written to port 64h.

6. Auxiliary device commands are written to port 60h after the Write Auxiliary Device command.

The auxiliary device data follows the same procedure.

TOY

The TOY chip is accessed at ISA addresses 070h and 071h, corresponding to CPU sparse I/O addresses 1 C000.0E00h and 1 C000.0E20h. The first address is used to load an address to the chip from bits<7:0>, the second address is then used to read or write data from/to that loaded address to/from data bits <7:0>.

The Digital AlphaStation 200 Series system includes a standard TOY clock that also has 114 bytes of battery-supported RAM. The chip is addressed as a device on the Utility Bus spawned by the ISA bridge chip. It is accessed at ISA addresses 070h and 071h, corresponding to PCI sparse I/O addresses 1 C000.0E00h and 1 C000.0E20h. Use the first address to load an address to the chip from bits<7:0>, then use the second address to read or write data from/to that loaded address to/from data bits <7:0>.

The TOY chip is also the source of a periodic interrupt for the CPU. It connects to IRQ4 on the 21064 CPU chip, bypassing the bridge chip's interrupt controller.

Firmware detects the CPU speed by counting cycles against the TOY clock's fixed period and sets up secondary cache timing appropriately.

Super I/O Chip

You can access the FDC through ISA addresses 3F0h through 3F7h. These addresses map into CPU sparse I/O addresses 1 C000.7E00 through 1 C000.7EE0.

The PC87312 super I/O chip is set to its "PC/AT mode" by tying the IDENT pin high during power-on reset. Status registers A and B at ISA addresses 3F0h and 3F1h are disabled in this mode.

Disabling Interrupts

To disable interrupts on the PCI-embedded controllers, follow these guidelines:

- **For SCSI.** Write zero to interrupt enable registers SIEN0, SIEN1, DIEN; clear any pending interrupts by reading interrupt status registers SIST0, SIST1, DSTAT.
- **For Ethernet controller.** Write zero to the interrupt mask register CSR7.
- **For Bridge chip.** Write ones (FFh) to operation control word 1 register for interrupt controller 1 and 2.

5

DMA

Overview

This chapter includes information on ISA DMA channels for the Digital AlphaStation 200 and 400 Series systems.

ISA DMA Channels

The ISA interface uses eight DMA channels. DMA channel 4 cascades two four-channel DMA controllers, leaving only channels 0-3 and 5-7 available.

Any DMA channel can be programmed for either 8- or 16-bit transfers. (Conventional usage is for channels 0-3 to be 8 bits and for channels 5-7 to be 16 bits.)

Any of the ISA option slots can use DMA channels 0-3 and 5-7.

CAUTION

Take care to avoid conflicts; DMA channel 2 is already spoken for by the super I/O chip, and channel 3 can be used by the parallel port.

The DMA channels are assigned as Figure 5-1 shows.

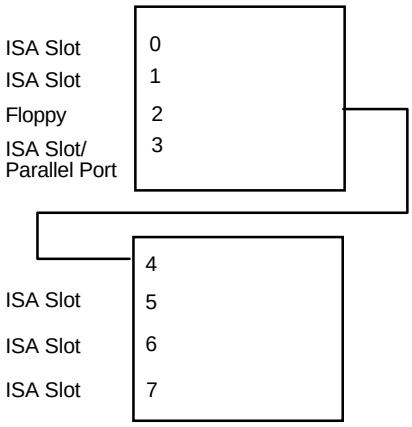


Figure 5-1. DMA Channel Assignments

6

Hardware Interrupts

Overview

This chapter discusses Digital AlphaStation 200 and 400 Series systems' hardware interrupts, including the following topic areas:

- Interrupts
- Sources
- Hardware reaction to errors

Interrupts

Interrupts from the various I/O components of the Digital AlphaStation 200 and 400 Series systems connect to the interrupt-controller section of the ISA bus bridge chip. Some interrupts are hardwired to specific interrupt levels, and some of the PCI interrupts may be programmed to connect to specific interrupt levels (Notice that the term *levels* here is used in the context of the bridge chip, not the CPU.) Figure 6-1 shows a block diagram of the interrupt system.

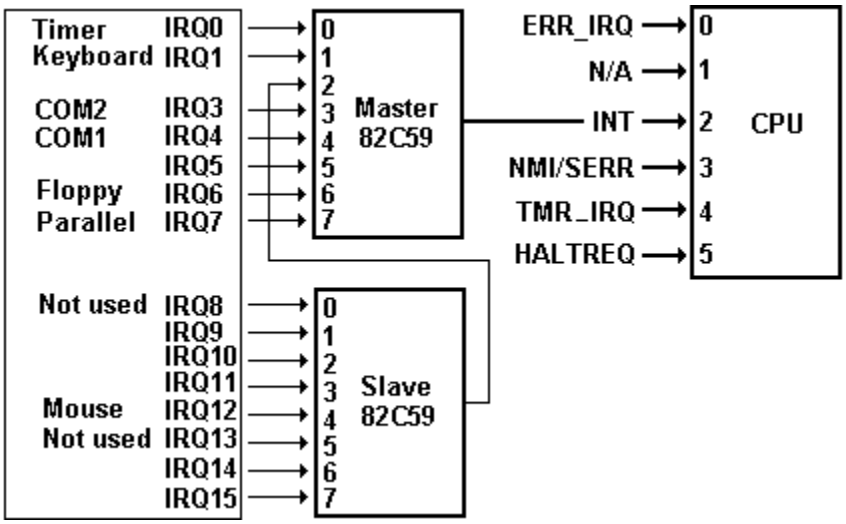


Figure 6-1. Interrupt System Block Diagram

The CPU has six interrupt inputs; five of these are used in the Digital AlphaStation 200 and 400 Series systems. All interrupt handling is performed in PALcode. Interrupt inputs are assigned as Table 6-1 shows.

Table 6-1. CPU Interrupt Inputs and Assignments

Interrupt Input	Interrupt Assignments
IRQ0	CPU bus and parity errors
IRQ1	Not used
IRQ2	Device interrupts (ISA and PCI)
IRQ3	NMI, PCI SERR#
IRQ4	Periodic interval timer interrupt from TOY chip
IRQ5	Halt switch

IRQ0: CPU Bus and Parity Errors

CPU internal errors are reported through the BIU_STAT register. PALcode intercepts the IRQ0 interrupt and builds a machine check logout frame, which is passed to the operating

system by means of an interrupt through system control block (SCB) entry 660h (hexadecimal) or 670h.

IRQ2: Device Interrupts

When a device interrupt has been detected on CPU line IRQ2, the PALcode interrupt dispatcher must generate a PCI INTACK cycle. The PCI-ISA bridge chip sees this cycle and converts it into two cycles that freeze and then read the normal ISA-style interrupt priority encoders within the bridge chip. The bridge chip then returns a vector on data bits <7:0>.

This INTACK cycle does not remove the source of the interrupt; specific code that accesses the device that interrupted must do this. The bridge chip releases its interrupt when the interrupt dispatcher issues an EOI command. This is a cooperative activity performed by some combination of PALcode and the particular operating system.

IRQ3: NMI (Nonmaskable Interrupt)

The PCI-ISA bridge chip generates this NMI (nonmaskable interrupt) when either SERR# or IOCHK# is asserted. The NMI signal connects to IRQ3 on the CPU.

SERR# indicates that an address parity error has been detected on the PCI bus by the bridge chip. The bridge chip takes no action other than reporting the error.

IOCHK# indicates that a parity error has been detected on a memory module plugged into the ISA bus.

You can use the NMISC register in the PCI-ISA bridge chip to distinguish which of the SERR# and IOCHK# conditions caused the interrupt.

IRQ4: Interval Timer Interrupt

You can program the time-of-year (TOY) clock chip to provide an interrupt output, which is connected directly to the IRQ4 input of the EV4S, bypassing the interrupt controller on the PCI-ISA bridge chip.

IRQ5: HALTREQ

You can assert the HALTREQ signal by pressing the front-panel HALT button. A jumper controls the function of this button; it can generate a HALTREQ interrupt or a CPU Reset signal. (Refer to Chapter 2, Configuring Your AlphaStation System, for jumper information on the 200 and 400 Series systems.) The HALTREQ signal is combined logically with KBRST before connecting to IRQ5 on the CPU.

The keyboard reset signal (KBRST) can be generated by the 8242 keyboard controller chip under software control. This line is connected to the P20 pin and is sometimes called *SRESET*.

Interrupt Inputs

The ISA bridge chip allows for 16 interrupt inputs; not all of these are external to then chip. Within the bridge chip, logic for two separate 8259 interrupt controllers are connected, with IRQ2 used to cascade the second controller. The controllers' priority, from highest to lowest, is 0-1, 8-15, 3-7. These interrupts are assigned as Table 6-2 describes, which indicates the various interrupt lines with all possible (p) sources and with the standard (s) or the hardwired (h) use.

Table 6-2. AlphaStation System Interrupt Assignments

IRQ Level ⇨ Device ⇩	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer/counter	h															
Keyboard		h														
COM2				s												
COM1					s											
FDC						s										
Parallel port						p		s								
Mouse													h			
Sound card								p		p	p	p				
ISA slots				p	p	p	p	p		p	p	p	p		p	p

Several interrupt lines are dedicated for specific uses . Additionally, three lines (shaded in the table) are unavailable because of hardware restrictions; IRQ2 is used to cascade the two interrupt controllers in the PCI-ISA bridge chip, and IRQ8 and IRQ13 are not connected. You can logically route the four PCI interrupt lines to ISA IRQs, internal to the PCI-ISA chip.

Because many of the interrupt requests that originate from an ISA slot can be connected to the same IRQ pin ("shared"), you must ensure that the jumpers selecting the actual connection are set up so that no sources are joined together, unless the single interrupt they would generate can be resolved as to its source.

IRQ 5 can be driven by the super I/O chip, as the parallel port interrupt; console firmware uses the more conventional IRQ7 instead.

IRQs 3-7, 9-12, and 14-15 can be driven by ISA slots. You must understand conflicts with interrupt lines used by the system's base logic and other options.

IRQs 7 and 9-11 can be driven by the sound card and are software-selectable.

Ordinarily, IRQ8 is used for an interval timer interrupt but is unconnected in the Digital AlphaStation 200 Series system; the interval timer interrupt is tied directly to the CPU instead.

PCI Interrupts

PCI interrupts from the PCI slots, plus the embedded SCSI and embedded Ethernet (Digital AlphaStation 200 Series system only) controllers are wire-ORed according to Table 6-3 and then brought to the four PCI interrupt inputs of the ISA bridge chip. These are logically routed to ISA IRQ lines.

Table 6-3. PCI Interrupt Assignments

AlphaStation 200 Series System				
	PIRQ 0	**PIRQ 1**	**PIRQ 2**	**PIRQ 3**
SCSI	.	.	.	x
Embedded Ethernet	x	.	.	.
Slot 1, INTA	.	x	.	.
Slot 1, INTB	x	.	.	.
Slot 1, INTC	.	.	x	.
Slot 1, INTD	.	x	.	.
Slot 2, INTA	.	.	x	.
Slot 2, INTB	.	x	.	.
Slot 2, INTC	x	.	.	.
Slot 2, INTD	.	.	x	.
PIRQ0 = Ethernet | 1B | 2C				
PIRQ1 = 1A | 1D | 2B				
PIRQ2 = 1C | 2A | 2D				
PIRQ3 = SCSI				

Table 6-3. PCI Interrupt Assignments *(continued)*

AlphaStation 400 Series System				
	PIRQ 0	**PIRQ 1**	**PIRQ 2**	**PIRQ 3**
SCSI	.	.	.	x
Slot 1, INTA	x	.	.	.
Slot 1, INTB	.	.	x	.
Slot 1, INTC	.	x	.	.
Slot 1, INTD	x	.	.	.
Slot 2, INTA	.	x	.	.
Slot 2, INTB	x	.	.	.
Slot 2, INTC	.	.	x	.
Slot 2, INTD	.	.	x	.
PIRQ0 = 1A | 1D | 2B | 3C				
PIRQ1 = 2A | 2D | 3B | 1C				
PIRQ2 = 3A | 3D | 1B |2C				
PIRQ3 = SCSI				

7

System Power-Up and Initialization

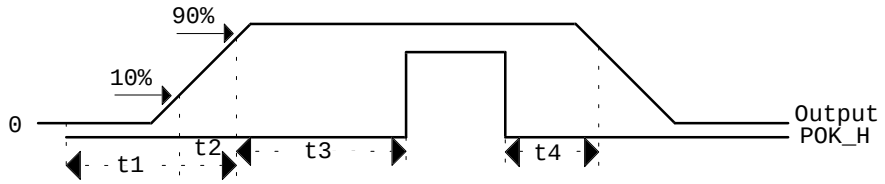
Overview

This chapter explains system power-up and initialization for the Digital AlphaStation 200 and 400 Series systems, as the following topics outline:

- Power-up sequence
- Power supply and input power requirements
- SROM
- POST
- Console initialization

Power-Up Sequence

Figure 7-1 illustrates the power supply timing. POK_H is asserted by the power supply to indicate that 5.0-Volt and 3.3-Volt outputs are above the required undervoltage thresholds. When one of these output voltages falls below the undervoltage thresholds or when the main power has been off beyond the recommended time, POK_H is negated.



- t1: Turn-on time: 1 second maximum
- t2: Rise time: 70 msec maximum
- t3: Delay turn on: 100-500 msec
- t4: Delay turn off: 1 msec minimum

Figure 7-1. Power Supply Timing

The signal timing shown in Figure 7-1 applies to both 5-Volt and 3.3-Volt outputs.

Power Supply and Input Power Requirements

AlphaStation 200 Series System

The 180-watt power supply for the Digital AlphaStation 200 Series system provides five DC voltages: +12-Volt, -12-Volt, +5-Volt, -5-Volt, and +3.3-Volt DC. These voltages are used by the various components within the system. Table 7-1 shows the AC input characteristics for the AlphaStation 200 Series system.

Table 7-1. AlphaStation 200 Series System AC Input Characteristics

Rated Voltage Range	Rated Input Current [1]	Operating Frequency Range
100-Volt AC – 120-Volt AC	4 A	47 Hz – 63 Hz
220-Volt AC – 240-Volt AC	3 A	47 Hz– 63 Hz

[1] Includes outlet current.

AlphaStation 400 Series System

The 300-watt power supply for the Digital AlphaStation 400 Series system provides five DC voltages: +12-Volt, -12-Volt, +5-Volt, -5-Volt, and +3.3-Volt DC. Various components within the system use these voltages. See Table 7-2 for details on the AC input characteristics for the AlphaStation 400 Series system.

Table 7-2. AlphaStation 400 Series System AC Input Characteristics

Rated Voltage Range	Maximum Range	Rated Input Current [1]	Operating Frequency Range
100-Volt AC – 120-Volt AC	88-Volt AC – 132-Volt AC	8 A	47 Hz – 63 Hz
220-Volt AC – 240-Volt AC	176-Volt AC – 264-Volt AC	4 A	47 Hz – 63 Hz

[1] Includes outlet current.

8

AlphaStation Firmware

Overview

This chapter first explains how to use the firmware for the Digital AlphaStation 200 and 400 Series systems and then gives information on console commands, as the following topics outline:

- Firmware components
- Initialization
- SROM features
- DROM features
- ARC console features
- SRM console features
- PALcode

Firmware Components

The following sections discuss the Digital AlphaStation Series system firmware.

Figure 8-1 shows the relationships between the following interfaces: console user; operating system; and system hardware.

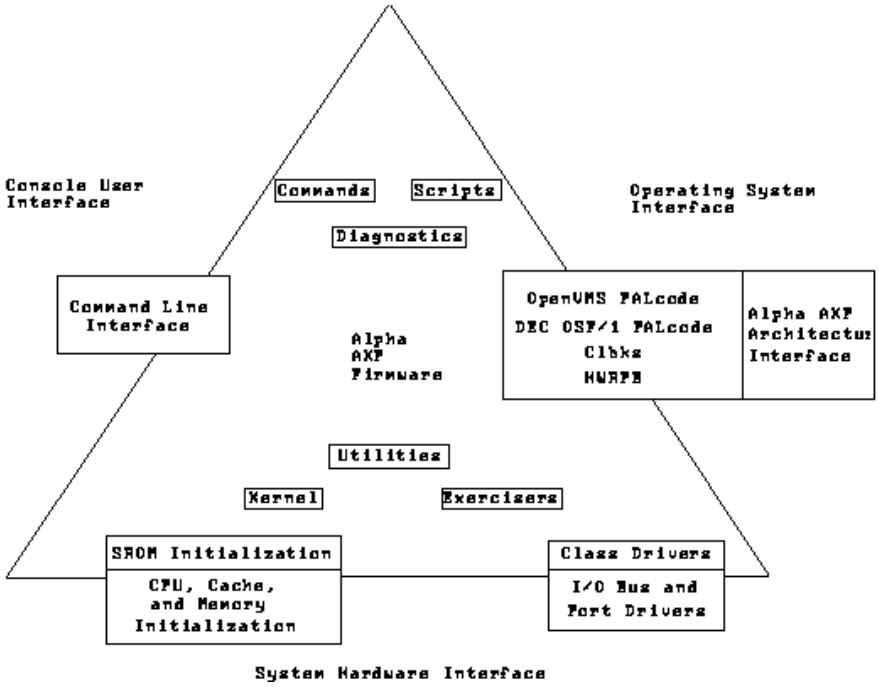


Figure 8-1. AlphaStation Interface Relationships

Initialization

In a normal system power-up, firmware initialization occurs in the following sequence, assuming that (1) there are no hard errors and (2) the firmware jumpers are in the normal position, as listed below:

1. SROM
2. DROM
3. SRM or ARC
4. Operating system

SROM Features

The SROM code performs the following tasks:

- Initializes the CPU
- Sizes and configures tests and initializes memory
- Tests and intializes the core logic
- Loads the DROM code (or PALcode and console code if there is a DROM error)
- Transfers execution to the DROM (or console)

The SROM uses the diagnostic LEDs to indicate progress while its code is executing. The sequence is also outputted to the CPU serial port. (A special adapter to attach a terminal to the CPU serial port is required.)

Loading the SROM Code

The SROM code resides in a 64K-bit ROM. When the system is powered on, the SROM code is loaded into the CPU's instruction cache (Icache). Once the SROM code is loaded, the CPU begins executing the code.

Following power-on, the CPU loads its I-stream internal cache from an external 64-bit SROM, clocking in the data as a serial bit stream. All I-cache bits are loaded from the 65536-bit serial stream, including both data and control bits; the size of the loaded program is therefore 7136 bytes. Data is loaded, least-significant bit first, starting from LW0 (LongWord0, 32 bits), then LW2, LW4, LW6, TAG (21 bits), ASN (6 bits), the ASM bit, the V bit, LW1, LW3, LW5, LW7, and, lastly, BHT (8 bits).

SROM LED Codes

Table 8-1 outlines the SROM LED codes and the related code meanings.

Table 8-1. AlphaStation Series System SROM Code Actions

Indicator Values[1] Bit 7 ... Bit 0	Hex Value	Meaning
● ● ● ● ● ● ● ●	FF	Initialize CPU (BIU_CTL and ABOX registers initialized).
● ● ● ● ● ● ● ○	FE	Initialize bank 8 logic. Executing memory sizing code.
● ● ● ● ● ● ○ ●	FD	Memory sizing completed. Configuring memory.
● ● ● ● ● ● ○ ○	FC	Memory configuration successful. Bcache initialization started. Initializing all memory to zeroes.
● ● ● ● ● ○ ● ●	FB	Bcache initialization successful. Bcache references OFF and Dcache OFF. Initialize the low 8MB of memory to zero. Executing memory test 1 of 4.
● ● ● ● ● ○ ● ○	FA	Memory test 1 of 4 complete. Executing memory test 2 of 4. Bcache references ON and Dcache OFF.
● ● ● ● ● ○ ○ ●	F9	Memory test 2 of 4 complete. Executing memory test 3 of 4. Bcache references OFF and Dcache ON.
● ● ● ● ● ○ ○ ○	F8	Memory test 3 of 4 complete. Executing memory test 4 of 4. Bcache references ON and Dcache ON.
● ● ● ● ○ ● ● ●	F7	Memory test 4 of 4 complete.
● ● ● ● ○ ● ● ○	F6	Initialize the core logic registers.
● ● ● ● ○ ● ○ ●	F5	Reserved for future.
● ● ● ● ○ ● ○ ○	F4	Reserved for future.
● ● ● ● ○ ○ ● ●	F3	Load the DROM code into memory.
● ● ● ● ○ ○ ● ○	F2	DROM and flashROM corrupted
● ● ● ● ○ ○ ○ ●	F1	Successful load and checksum of DROM
● ● ● ● ○ ○ ○ ○	F0	Initialize registers required by console firmware and the PAL_BASE and EXEC_ADDR registers.

[1]The filled-in circle (●) indicates that the LED is on, and the open circle (○) indicates off.

SROM Beep Codes

Beep codes are heard from the system's speaker as three groups of beeps. For example, if the SROM code could not find any good memory, you would hear a 1-3-3 beep code (one beep, a pause, a burst of three beeps, a pause, and another burst of three beeps). Table 8-2 shows the SROM beep codes and their meanings for the Digital AlphaStation 200 and 400 Series systems.

Table 8-2. AlphaStation SROM Beep Codes

Beep Code	Meaning
1-1-4	The SROM code could not read the DROM or flashROM header, or there was a checksum failure.
1-2-4	The SROM code detected a hard failure (for example, a Bcache failure).
1-3-3	The SROM could not find 2 MByte of good memory, or no memory is present.

Leaving the SROM Code

When the SROM code has completed its tasks, it normally loads the DROM code and turns control over to it. The SROM checks to see if the DROM contains the proper header and that the checksum is correct. If either check fails, the SROM code reads a location in the TOY NVRAM. The location indicates which console firmware (the SRM or the ARC) should be loaded.

When the console firmware is loaded, the header check and the checksum are checked. If either is in error, the SROM code jumps to its mini-console routine. With the appropriate adapter, you can attach a terminal to the CPU's serial port and use the mini-console. Typically, this port is used in the manufacturing environment.

DROM Features

The DROM contains code that performs power on self-test (POST). The DROM, a 64-KByte UV EPROM, contains:

- Mini-console routines
- POST routines
- Manufacturing test tools
- Floppy loader
- Flash loader

Loading the DROM code

The SROM code loads the DROM code into memory and starts it.

DROM LED Codes

Table 8-3 shows the DROM POST steps and LED codes for the Digital AlphaStation 200 and 400 Series systems.

Table 8-3. AlphaStation DROM POST Actions and LED Codes

Indicator Values[2] Bit 7 ... Bit 0	Hex Value	Meaning
● ● ● ● ● ○ ● ○	DF	DROM code entered.
● ● ○ ● ● ● ● ○	DE	PCI Bridge core logic errors cleared.
● ● ○ ● ● ● ○ ●	DD	Memory test passed.
● ● ○ ● ● ● ○ ○	DC	FlashROM ID test passed.
● ● ○ ● ● ○ ● ●	DB	NVRAM test passed.
● ● ○ ● ● ○ ● ○	DA	SCSI controller (53C810) test passed.
● ● ○ ● ● ○ ○ ●	D9	System I/O (82378) test passed.
● ● ○ ● ● ○ ○ ○	D8	TOY (3287) test passed.
● ● ○ ● ○ ● ● ●	D7	Keyboard controller (8242) test passed.
● ● ○ ● ○ ● ● ○	D6	Super I/O (87332) test passed.
● ● ○ ● ○ ● ○ ●	D5	Interrupts test passed.
● ● ○ ● ○ ● ○ ○	D4	Floppy loader called.
● ● ○ ● ○ ○ ● ●	D3	Jumping to floppy code.
● ● ○ ● ○ ○ ● ○	D2	Flash loader called.
● ● ○ ● ○ ○ ○ ●	D1	Jumping to flash code.
● ● ○ ● ○ ○ ○ ○	D0	Power on self test passed, DROM console running
● ● ● ○ ○ ○ ● ○	E2	Floppy load failed
● ● ● ○ ○ ○ ○ ●	E1	Flash load failed
○ ○ ○ ○ ○ ○ ● ○	20	Machine check occurred.

[2]The filled-in circle (●) indicates that the LED is on, and the open circle (○) indicates off.

DROM Beep Codes

Beep codes are heard from the system's speaker as three groups of beeps. For example, if the DROM code detected a realtime clock failure, you would hear a 1-2-1 beep code (one beep, a pause, a burst of two beeps, a pause, and one more singel beep). Table 8-4 shows the DROM beep codes and their meanings for the Digital AlphaStation 200 and 400 Series systems.

Table 8-4. AlphaStation DROM Beep Codes

Beep Code	Meaning
1-2-1	The DROM code detected a realtime clock (BQ3287) failure, or the realtime clock interrupt did not occur.
3-2-4	The DROM code detected a keyboard/mouse controller failure.
3-2-1	The DROM code was unable to read the header of the flashROM, or the flashROM checksum failed. Therefore the DROM code attempted to boot from the floppy diskette. The attempt failed because: 1. There is no floppy in the drive. 2. The Alpha boot block is missing from the floppy.
3-2-3	The DROM code was directed by the position of J5 to load the floppy, but there is no floppy in the drive.
3-3-1	The DROM code detected a hard failure during testing. The LEDs display the failure code.

Leaving the DROM Code

The DROM can load the ARC or SRM console firmware or load the contents of a firmware floppy.

When the DROM loads the ARC or SRM console firmware, it performs a header check and a checksum. If either failed, the DROM attempts to load a firmware from a floppy. This is a failsafe feature.

When the DROM attempts to load firmware from a floppy, it examines the floppy for an Alpha boot block. If the boot block is present, the DROM code jumps to the boot block. If the boot block is not present, the DROM code jumps to the DROM mini-console. Figure 8-2 illustrates the possible DROM code actions.

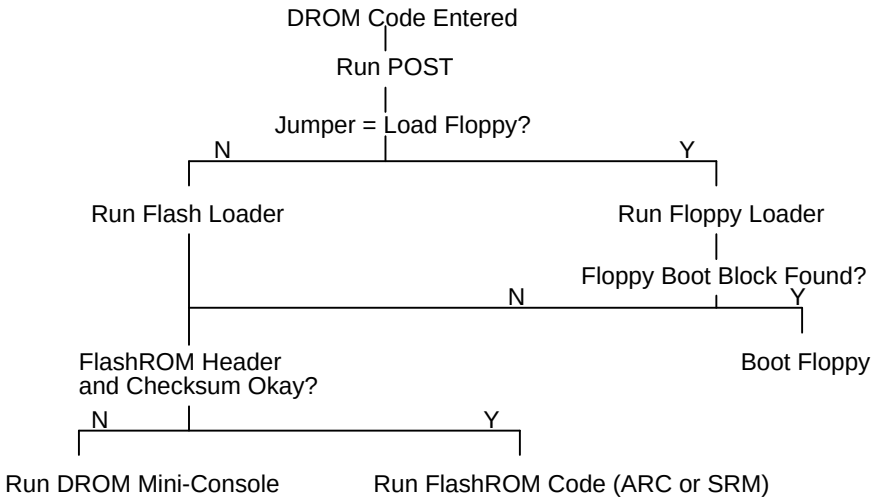


Figure 8-2. Possible DROM Code Actions

ARC Console Features

The ARC console supports the Microsoft Windows NT operating system. The ARC console features an easy-to-use menu interface. The console includes:

- Easy to read hardware configuration display.
- Tools to manage the environment variables.
- Flexible boot selection menu.

ARC Console LED Codes

Table 8-5 outlines the SROM LED codes and the related code meanings.

Table 8-5. ARC Console LED Codes

Indicator Values[3] Bit 7 ... Bit 0	Hex Value	Meaning
● ● ● ● ● ● ○ ●	FD	ARC environment loaded.
● ● ● ● ● ● ○ ○	FC	ARC console initialized (normal final state).
● ● ● ● ● ○ ● ○	FA	ARC serial port initialized.
● ● ● ● ● ○ ○ ●	F9	ARC initialize keyboard controller.
● ● ● ● ○ ● ● ●	F7	ARC video okay.
● ● ● ● ○ ● ● ○	F6	ARC broken video or keyboard.
● ● ● ● ○ ● ○ ○	F4	ARC fatal firmware error.

NOTE

Note: The ARC console codes reuse codes that were used by the SROM.

[3]The filled-in circle (●) indicates that the LED is on, and the open circle (○) indicates off.

SRM Console Features

The SRM console supports the Digital UNIX and OpenVMS operating systems. The SRM console firmware provides the services and functionality commonly found in much more expensive machines. The console includes:

- An operator interface
- An operating system bootstrap
- Support for operating system restarts
- Self-test diagnostics

SRM Console LED Codes

Table 8-6 outlines the SROM LED codes and the related code meanings.

Table 8-6. SRM Console LED Codes

Indicator Values[4] Bit 7 Bit 0	Hex Value	Meaning
● ● ● ● ● ● ● ●	FF	SRM console starting.
● ● ● ● ● ● ● ○	FE	SRM initialize idle PCB.
● ● ● ● ● ● ○ ●	FD	SRM initialize semaphores.
● ● ● ● ● ● ○ ○	FC	SRM initializing heap (dynamic memory).
● ● ● ● ● ● ○ ●	FB	SRM initializing heap (dynamic memory).
● ● ● ● ● ○ ● ○	FA	SRM initializing heap (dynamic memory).
● ● ● ● ● ○ ○ ●	F9	SRM initializing driver structures.
● ● ● ● ● ○ ○ ○	F8	SRM initializing idle process PID.
● ● ● ● ○ ● ● ●	F7	SRM initializing file system.
● ● ● ● ○ ● ● ○	F6	SRM initializing timer data structures.
● ● ● ● ○ ● ○ ●	F5	SRM lower the IPL.
● ● ● ● ○ ● ○ ○	F4	SRM entering the idle loop.
● ● ● ○ ● ● ● ●	EF	SRM memory configuration.
● ● ○ ● ● ● ● ●	DF	SRM initialize IRQ vector table and configure PCI bus.
● ● ● ○ ● ● ● ○	EE	SRM DDB startup parts 1, 2, and 3, and locate HWRPB

[4]The filled-in circle (●) indicates that the LED is on, and the open circle (○) indicates off.

Table 8-6 SRM Console LED Codes *(continued)*

Indicator Values Bit 7 ... Bit 0	Hex Value	Meaning
● ● ● ○ ● ● ○ ●	ED	SRM: DDB startup parts 1, 2, and 3, and locate HWRPB
● ● ● ○ ● ● ○ ○	EC	SRM: DDB startup parts 1, 2, and 3, and locate HWRPB
● ● ● ○ ● ○ ● ●	EB	SRM: test memory greater then 8 MB.
● ● ● ○ ● ○ ● ○	EA	SRM: DDB startup part 4.
● ● ● ○ ● ○ ○ ●	E9	SRM: set keyboard type according to language variable.
● ● ● ○ ● ○ ○ ○	E8	SRM: initialize environment variables.
● ● ● ○ ○ ● ● ●	E7	SRM: initialize SCSI.
● ● ● ○ ○ ● ● ○	E6	SRM: DDB startup part 5.
● ● ● ● ● ● ○ ●	E5	SRM:show version and console idle (normal final state)

NOTE

The SRM console codes reuse codes that were used by the SROM.

ISA Configuration Utility

ISA (industry-standard architecture) devices are not capable of being probed for configuration information by the Digital UNIX or OpenVMS operating systems. Therefore, you must enter ISA option information manually using the ISA configuration utility (ISACFG). Run this utility before installing a new ISA option module on a Digital AlphaStation 200 or 400 Series system running either the Digital UNIX or OpenVMS operating systems.

Command Format

The syntax of the ISACFG command is:

```
isacfg [-slot <slot#>] [-dev <device#>]
[-all|-rm|-mk|-mod] [-<field> <value>] . . .
```

The ISACFG command options are described in Table 8-7.

Table 8-7. SRM ISACFG Command Options

Command Option	Description
-all	Shows the entire configuration table. Overrides all other commands.
-dev <dev#>	Optional; defaults to 0 if not entered. On a multifunction or multiport adapter, this specifies the device on the adapter.
-dmachan{0-3} <#>	Allows you to specify up to four DMA (direct memory access) channels for the device.
-dmamode{0-3} <#>	Allows you to specify the DMA type for -dmachan{0-3}. DMA modes are: 1 - Block 2 - Demand 4 - Single 8 - Cascade
-enadev <#>	Allows you to specify whether an entry is enabled or disabled. Disabled devices are not used in resource allocation calculations. The possible values are: 0 - No (disabled) 1 - Yes (enabled)

Table 8-7. SRM ISACFG Command Options *(continued)*

Command Option	Description
-etyp <#>	Defines an entry type for this entry. The # sign can be: 0 - Causes the entry to be deleted 1 - Single option 2 - Embedded multiport device 3 - Multiport option device
-handle <string>	Binds a name to the driver (up to 15 characters).
-init	Initializes the configuration table to the default settings.
-iobase{0-5} <#>	Specifies up to six I/O base registers (in hexadecimal) for a particular device entry.
-irq{0-3} <#>	Allows you to assign up to four IRQ (interrupt request) channels to the device (use decimal IRQ levels).
-membase{0-2} <#>	Specifies up to three R/W ISA memory regions (hexadecimal).
-memlen{0-2} <#>	Specifies the length corresponding to membase{0-2} (hexidecimal).
-mk	Adds an entry into the table.
-mod	Modifies an entry in the table.
-rm	Deletes an entry from the table.
-rombase <#>	Specifies an address for ISA BIOS ext. ROM (hexadecimal).
-romlen <#>	Specifies length of ROM (hexadecimal).
-slot <slot#>	Allows you to enter a unique slot number for each ISA adapter. You may assign the numbers in any order. The slot number does not relate to a physical ISA adapter position in the motherboard. Slot 0 is reserved for the local multiport adapter.
-totdev <#>	Placeholder for you to keep track of the total number of devices, specified by the # sign, at this slot. Modify this for your own use.

Adding ISA Options to OpenVMS and Digital UNIX Systems

When you add a supported ISA option to an AlphaStation 200 Series system running the OpenVMS or Digital UNIX operating system, perform the procedure shown in Table A-8.

Table 8-8. Adding Options to OpenVMS or Digital UNIX Systems

Step	Action	Result or Next Step
1.	Perform operating system configuration tasks, if any. Refer to your operating system installation guide and release notes.	The operating system is prepared for the ISA option.
2.	Shut down the system.	The system is at the console prompt (>>>).
3.	`>>>isacfg` *options*	Adds the new ISA option to the SRM console configuration table using the appropriate command options.
4.	`>>>init`	Typing `init` allows the changes to be used.
5.	Configure the ISA option.	Use the manual that came with your ISA option to set the proper configuration.
6.	Turn off the system and install the ISA option.	Refer to your AlphaStation *User Information* for more information.
7.	Turn on the system and boot.	The operating system boots and sees the new ISA option.

ISACFG Command Examples

This section shows examples of ISACFG commands you use to enter the DE205, sound card, and the FAX/MODEM options into the configuration database. Examples to display, modify, and remove table entries are included as well. In some cases, scripts are available to issue the proper ISACFG command. Script commands are preceded by an "add_" prefix.

Adding the DE205 option:

```
>>>add_de205
```

– or –

```
>>>isacfg -slot 1 -dev 0 -mk -handle DE200-LE\
_> -irq0 5 -iobase0 300 -membase0 d0000 -memlen0\
_> 10000 -etyp 1 -enadev 1
```

Adding the sound card option:

```
>>>add_sound
```

– or –

```
>>>isacfg -slot 2 -etyp 1 -mk -iobase0 530 -iobase1 388
-irq0 9 -dmachan0 0 -dmachan1 1 -handle PCXBJ -enadev 1
```

Adding the FAX/MODEM option:

```
>>>add_fax
```

– or –

the following two commands:

```
>>>isacfg -mod -slot 0 -dev 3 -enadev 0
```

```
>>>isacfg -slot 4 -dev 0 -ml -handle COM4 -irq0 3 \
_> -iobase0 2e8 -etyp 1 -enadev 1
```

Displaying the configuration database:

```
>>>isacfg -all
```

Modifying the IRQ0 entry of an option:

```
>>>isacfg -mod -slot 1 -irq0 14
```

Removing an entry:

```
>>>isacfg -rm -slot 1 -dev 0
```

SRM Scripts

A script is an ASCII string that is interpreted by the SRM console. Parameters can be passed into a script indicating specific options.

To view a script, enter the "`cat` *`script_name`*" command. This will result in the script named by *`script_name`* being displayed.

9

Fault Management

Overview

This chapter describes the decoding of error messages as produced by the AlphaStation Series system hardware.

The AlphaStation 200 and 400 Series systems can run three different operating systems. This chapter describes the type of information that is available to the operating systems but does not cover the format of the error logger within the operating systems.

The following general topics are covered in this chapter:

- Control signal codes
- Summary of errors
- Machine check logout frame
- Error registers
- PALcode and operating system responsibilities
- Error format
- SCB 660 fatal machine checks
- SCB 670 processor fatal machine checks
- Additional errors

Control Signal Codes

The AlphaStation 200 and 400 Series system control signals are used as communications and control between the major system components. The state of these signals are useful in determining the cause of an error. The following section lists the various control signals and their state interpretations.

PCI Cycle Codes

The PCI bus transactions are encoded on the four C/BE[3:0] lines. Table 9-1 shows the cycle type definitions.

Table 9-1. PCI Cycle Codes

Code	Cycle Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	"
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	"
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

Cycle Acknowledgment

The cAck_h lines connecting to the CPU signal cycle codes for completions of cycle transactions. Table 9-2 shows the cAck cycle code types.

Table 9-2. PCI cAck Cycle Codes

Code	Cycle Type
000	IDLE
001	HARD_ERROR
010	SOFT_ERROR - . This code is not used.
011	STL_C FAIL or STQ_C FAIL
100	OK
101	Undefined
110	Undefined
111	Undefined

Cycle Request

The cReq lines are used to indicate the cycle type at the start of an external cycle. Table 9-3 shows the cReq cycle code types.

Table 9-3. PCI cReq Cycle Codes

Code	Cycle Type
000	IDLE
001	BARRIER
010	FETCH
011	FETCH_M
100	READ_BLOCK
101	WRITE_BLOCK
110	LDL_L or LDQ_L
111	STL_C or STQ_C

IO Commands

The ioCmd lines are used by the PCI bridge chip to request an action by the cache and memory controller chip. Table 9-4 shows the PCI IO command codes.

Table 9-4. PCI IO Commands

Code	CPU controls sysBus Cycle Type	PCI Bridge controls sysBus Cycle Type
000	IDLE	IDLE
001	ClrLock	Flush
010	cpuDRAck ok_NCache_NChk	Write
011	cpuDRAck ok_NCache	Write masked
100	cpuCAck ok	Read
101	cpuCAck Hard_Error	Read Burst
110	cpuCAck Soft_Error	Read Wrapped
111	cpuCAck STxC_Fail	Read Burst Wrapped

Summary of Errors

All errors addressed in this document are summarized in the following sections.

Machine Check ID

Each machine check that the system supports equates to a Machine Check ID that is logged in the Machine Check Logout Frame at MCLF+10. Table 9-5 lists all valid Machine Check IDs for the AlphaStation 200 and 400 Series systems as reported by PALcode.

Table 9-5. Machine Check ID Codes

Code (hex)	Description	SCB	Recovery Action
80	Tag Parity Error	660	Fatal
82	Tag Control Error	660	Fatal
84	Hardware Error	670	Fatal
86	Correctable ECC	-	Not implemented
88	Noncorrectable ECC	-	Not implemented
8A	Unknown Error	670	Fatal
8C	CackSoft Error	670	Fatal
8E	BugCheck	670	Fatal
90	OS Bugcheck	670	Fatal
92	Dcache Parity Error	670	Fatal
94	Icache Parity Error	670	Fatal
96	c3 Tag Parity Error	670	Fatal
201	I/O Read/Write Retry Timeout	660	Fatal
202	DMA Data Parity Error	660	Fatal
203	I/O Data Parity Error	660	Fatal
204	Slave Abort PCI Transaction	660	Fatal
205	DEVSEL Not Asserted	660	Fatal
206	Correctable Read Error	–	Not implemented
207	Uncorrectable Read Error	660	Fatal
208	Invalid Page Table Lookup (Scatter Gather)	660	Fatal
209	Memory Cycle Error	660	Fatal
20A	Bcache Tag Address Parity Error	660	Fatal
20B	Bcache Tag Control Parity Error	660	Fatal
20C	Nonexistent Memory Error	660	Fatal
20D	SIO Check Condition	660	Fatal

Machine Check Logout Frame

The following is the format of the machine check logout frame built by the console firmware. All registers in Table 9-6 are CPU-specific registers.

Table 9-6. Machine Check Logout Frame

63	47	31	15 0	
R | S |	SBZ		Bytes	+000h
System offset = [???h]		Processor offset = [???h]		+008h
		Mcheck id		+010h
PAL Temp registers [31:0]<63:0>				+018h
EXC_ADDR				+110h
EXC_SUM				+118h
EXC_MASKk				+128h
ICCSR				+128h
PAL_BASE				+130h
HIER				+138h
HIRR				+140h
MM_CSR				+148h
DC_STAT				+150h
DC_ADDR				+158h
ABOX_CTL				+160h
BIU_STAT				+168h
BIU_ADDR				+170h
BIU_CTL				+178h
FILL_SYNDROME				+180h
FILL_ADDR				+188h
VA				+190h
BC_TAG				+198h

Machine Check Logout Frame *(continued)*

All registers on this page are system-specific registers for the Cache and Memory Controller chip (DECchip 21071-CA).

COMA_GCR	+1A0h
COMA_EDSR	+1A8h
COMA_TER	+1B0h
COMA_ELAR	+1B8h
COMA_EHAR	+1C0h
COMA_LDLR	+1C8h
COMA_LDHR	+1D0h
COMA_BASE0	+1D8h
COMA_BASE1	+1E0h
COMA_BASE2	+1E8h
COMA_CNFG0	+1F0h
COMA_CNFG1	+1F8h
COMA_CNFG2	+200h

Machine Check Logout Frame *(continued)*

All registers on this page are system-specific registers for the PCI Bridge chip (DECchip 21071-DA).

EPIC_DCSR	+208h
EPIC_PEAR	+210h
EPIC_SEAR	+218h
EPIC_TBR1	+220h
EPIC_TBR2	+228h
EPIC_PBR1	+230h
EPIC_PBR2	+238h
EPIC_PMR1	+240h
EPIC_PMR2	+248h
EPIC_HARX1	+250h
EPIC_HARX2	+258h
EPIC_PMLT	+260h
EPIC_TAG0	+268h
EPIC_TAG1	+270h
EPIC_TAG2	+278h
EPIC_TAG3	+280h
EPIC_TAG4	+288h
EPIC_TAG5	+290h
EPIC_TAG6	+298h
EPIC_TAG7	+2A0h
EPIC_DATA0	+2A8h
EPIC_DATA1	+2B0h
EPIC_DATA2	+2B8h
EPIC_DATA3	+2C0h
EPIC_DATA4	+2C8h
EPIC_DATA5	+2D0h
EPIC_DATA6	+2D8h
EPIC_DATA7	+2E0h

Error Registers

CPU internal errors are reported through the BIU_STAT register

For CPU external interrupts, the PALcode parses the HIRR register in the CPU to determine the major error IRQ.

Once the interrupt is determined, the PALcode parses one of the registers shown in Table 9-7 for detailed information on the cause of the error.

Table 9-7. Error Registers

Nmemonic	Register Name	Bus Address	MCLF[5] Offset
BIU_STAT	Bus Interface Unit Status	–	168
DCSR	Diag. Control & Status	1 A000 0000	208
GCR	Error & Diag. Status	1 8000 0000	1A0

PALcode and Operating System Responsibilities

In handling errors, the PALcode is responsible for parsing the exception and building the logout frame. All errors produce the complete logout frame detailed in Table 9-7.

The PALcode is responsible for the following actions :

- Examines all error bits
- Decides on the nature of the machine check or interrupt
- Performs corrective action if possible
- Builds AlphaStation 400 Series Machine Check Logout Frame
- Builds stack frame
- Clears error bits
- Passes control to the operating system through SCB

[5]MCLF = machine check log frame

The operating system machine check handler is responsible for the following actions :

- Creates kernel rvent jeader frame
- Appends the machine check logout frame
- Updates error log
- Executes fault analysis using the saved machine check frame and context

Error Format

It is assumed that the user of this section will see the error as it is handed off to the operating system from the system PALcode. SCB offset can best organized this.

You can enter an error routine from either the CPU vectoring to an SCB or from a post-machine check process to reconstruct an error for reporting. The general layout for the remainder of this section is shown in Table 9-8 .

Table 9-8. Error Format

Machine Check Code	Error
Error Name	The software name of the error.
Register_name	The register name and bit that identifies the error.
Bit Description	Text describing the bit.
Recovery:	
Analysis:	
Faulting FRU:	

SCB 660 Fatal Machine Checks

Machine check codes vectoring through SCB 660 range from 0x201 to 0x20C . These machine checks cause an ERROR-IRQ interrupt on the CPU's IRQ0 line. This interrupt indicates that the PCI bridge chip detected an abnormal condition during a transaction.

Machine Check Code 0x201, Retry Timeout Error

See Table 9-9 for information on the retry timeout errors .

Table 9-9. Error: Retry Timeout

Error name:	mchk$c_iort
Register name:	EPIC_DCSR bit<5> = 1 - iORT (MCLF+208)
Bit description:	Retry Timeout Error CPU initiated R/W timed out.
Recovery:	Not recoverable. Clear error by writing to 1 A000 0000, bit<5> with a one.
Analysis:	A timeout error occurred after retrying access to the address [EPIC_PEAR}. Examine PEAR (MCLF+210) bit<31:0> to determine the value of AD<31:0> when the error was logged.
Faulting FRU:	PCI or ISA option.

Machine Check Code 0x202, DMA Data Parity Error

See Table 9-10 for information on machine check code 0x202, DMA data parity errors .

Table 9-10. Error: DMA Data Parity Error

Error name:	mchk$c_ddpe
Register name:	EPIC_DCSR bit<8> = 1 - dDPE (MCLF+208)
Bit description:	DMA Data Parity Error. A parity error occurred in the data phase of a DMA.
Recovery:	Not recoverable.
Analysis:	A DMA parity error occurred at the address [EPIC_PEAR}. Examine PEAR (MCLF+210) bit<31:0> to determine the value of AD<31:0> when the error was logged.
Faulting FRU:	

Machine Check Code 0x203, I/O Parity Error

See Table 9-11 for information on machine check code 0x203, I/O parity errors .

Table 9-11. Error: I/O Parity

Error name:	mchk$c_iope
Register name:	EPIC_DCSR bit<9> = 1 - iOPEI, /O Parity Error (MCLF+208)
Bit description:	An I/O parity error occurred in the data phase of an I/O R/W transaction.
Recovery:	Not recoverable.
Analysis:	An I/O parity error occurred at [PEAR] during a [pCmd] cycle. (MCLF+208) bit<21:18>EPIC_DCSR - pCmd field which indicates the PCI cycle type when the PCI initiated error is logged. Refer to Table 9-1 for PCI Codes.(MCLF+210) bit<31:0> EPIC_PEAR - to determine value of AD<31:0> when error was logged.
Faulting FRU:	

Machine Check Code 0x204, Target Abort

See Table 9-12 for information on machine check code 0x204, target abort .

Table 9-12. Target Abort

Error name:	mchk$c_tabt
Register name:	EPCI_DCSR bit<10> = 1 - tABT(MCLF+208)
Bit description:	A PCI slave device ended an I/O R/W transaction using the PCI target abort protocol.
Recovery:	Not recoverable. Clear error by writing to 1 A000 0000, bit<10> with a one.
Analysis:	A PCI option requested a target abort during a [pCmd] cycle to address [EPIC_PEAR] EPIC_DCSR (MCLF+208) bit<21:18> - pCmd field which indicates the PCI cycle type when the PCI initiated error is logged. Refer to Table 9-1 for PCI Codes. (MCLF+210) bit<31:0> EPIC_PEAR - to determine value of AD<31:0> when error was logged. Read 1 E006 0140 (SIO Device Status Register) (not saved in MCLF) If bit<15:11> != 0 - Determine the cause of abort If bit<11> = 1 - SIO generated a target abort If bit<12> = 1 - SIO received target abort while master of bus.

Table 9-12. Target Abort *(continued)*

Analysis *(continued)*:	Read 1 E007 0140 - SCSI Device Status Register If bit<15:11> != 0 - Determine the cause of abort. If bit<15> = 1 - SCSI detected parity error If bit<14> = 1 - SCSI signalled system error If bit<13> = 1 - SCSI received master abort If bit<12> = 1 - SCSI received target abort If bit<11> = 1 - SCSI signalled target abort If bit<8> = 1 - Parity Error checking is enabled plus SCSI asserted PERR or observed PERR assert by the bus master Read 1 E00B 0000 - PCI Option Slot 1 If bit<15:11> != 0 - Determine the cause of abort If bit<15> = 1 - Slot 1 Option detected parity error If bit<14> = 1 - Slot 1 Option signalled system error If bit<13> = 1 - Slot 1 Option received master abort If bit<12> = 1 - Slot 1 Option received target abort If bit<11> = 1 - Slot 1 Option signalled target abort If bit<8> = 1 - Parity Error checking is enabled plus Slot 1 Option asserted PERR or observed PERR assert by the bus master Read 1 E00C 0000 - PCI Option Slot 2 If bit<15:11> != 0 - Determine the cause of abort If bit<15> = 1 - Slot 2 Option detected parity error If bit<14> = 1 - Slot 2 Option signalled system error If bit<13> = 1 - Slot 2 Option received master abort If bit<12> = 1 - Slot 2 Option received target abort If bit<11> = 1 - Slot 2 Option signalled target abort If bit<8> = 1 - Parity Error checking is enabled plus Slot 2 Option asserted PERR or observed PERR assert by the bus master. Read 1 E00D 0000 - PCI Option Slot 3 If bit<15:11> != 0 - Determine the cause of abort If bit<15> = 1 - Slot 3 Option detected parity error If bit<14> = 1 - Slot 3 Option signalled system error If bit<13> = 1 - Slot 3 Option received master abort If bit<12> = 1 - Slot 3 Option received target abort If bit<11> = 1 - Slot 3 Option signalled target abort If bit<8> = 1 - Parity Error checking is enabled plus Slot 3 Option asserted PERR or observed PERR assert by the bus master If bit<13> = 1 - SIO generated a master abort while bus master.
Faulting FRU:	PCI or ISA option.

Machine Check Code 0x205, No Device

See Table 9-13 for information on machine check code 0x205, No Device .

Table 9-13. No Device

Error name:	mchk$c_ndev
Register name:	EPIC_DCSR bit<11> = 1 - (MCLF+208)
Bit description:	DEVSEL# was not asserted in response to an I/O R/W initiated by the EPIC Chip.
Recovery:	Not recoverable.. Clear error by writing to 1 A000 0000, bit<11> with a one.
Analysis:	Either there is no device or the device at [EPIC_PEAR] did not respond during a [pCmd] cycle. EPIC_DCSR - pCmd field (MCLF+208) bit<21:18> indicates the PCI cycle type when the PCI initiated error is logged. Refer to Table 9-1 for PCI Codes. EPIC_PEAR(MCLF+210) bits<31:0> to determine value of AD<31:0> when error was logged.
Faulting FRU:	PCI or ISA option.

Machine Check Code 0x206, Correctable Memory Error

See Table 9-14 for information on machine check code 0x206, correctable memory errors .

Table 9-14. Error: Correctable Memory

Error name:	mchk$c_cmrd
Register name:	EPIC_DCSR bit<12> = 1 - cMRD (MCLF+208)
Bit description:	Correctable Memory Error. This error should never occur since the AlphaStation 200 and 400 Series systems do not use ECC.
Recovery:	Not recoverable.
Analysis:	A correctable memory error was reported. The cache and memory controller chip reported an error in ECC which is not implimented. Check the state of the DISABLE CORRECTABLE bit at MCLF+208 bit<3>. A one state is the correct state(MCLF+208) bit<3> to report state of Disable Correctable.
Faulting FRU:	Motherboard (200 Series system) or CPU module (400 Series system).

Machine Check Code 0x207, Uncorrectable Memory Error

See Table 9-15 for information on machine check code 0x207, uncorrectable memory errors .

Table 9-15. Error: Uncorrectable Memory

Error name:	mchk$c_umrd
Register name:	EPIC_DCSR bit<13> = 1 - uMRD (MCLF+208)
Bit description:	Uncorrectable Memory Read Data. An uncorrectable error was encountered by the PCI bridge (21071-DA) in the data read from the DMA Read Buffer in the data path chips during a DMA read or scatter gather read.
Recovery:	Not recoverable.
Analysis:	A memory read data error occurred at [SEAR]. Look at EPIC_SEAR (MCLF+218) bits<31:4> to determine value of sysAdr<33:6> when error was logged.
Faulting FRU:	

Machine Check Code 0x208, Invalid Page Table Lookup

See Table 9-16 for information on machine check code 0x208, invalid page table lookup.

Table 9-16. Invalid Page Table Lookup

Error name:	mchk$c_iptl
Register name:	EPIC_DCSR bit<14> = 1 - iPTL (MCLF+208)
Bit description:	Invalid Page Table Lookup. The longword scatter/gather map entry being accessed was invalid.
Recovery:	Not recoverable.
Analysis:	An invalid access was detected during a [pCmd] cycle at address [EPIC_PEAR]. If (MCLF+208) bit<5,8,9,10 or 11> are set, the address for this error is lost. EPIC_DCSR (MCLF+208) bits<21:18> - pCmd field indicates the PCI cycle type when the PCI initiated error is logged. Refer to Table 9-1 for PCI Codes. EPIC_PEAR (MCLF+210) bit<31:0> - to determine value of AD<31:0> when error was logged.
Faulting FRU:	SIMM, CPU module (400 Series system) or motherboard (200 Series system).

Machine Check Code 0x209, Memory Error

See Table 9-17 for information on machine check code 0x209, memory error .

Table 9-17. Memory Error

Error name:	mchk$c_merr
Register name:	EPIC_DCSR bit<15> = 1 - mErr (MCLF+208)
Bit description:	Memory Error. An error code was recieved in the ioCAck<1:0> field in response to a memory access.
Recovery:	Not recoverable.
Analysis:	The SIMM bank containing the memory error wa [calculated bank]. If (MCLF+208) bit<12 or 13> are set, the address for this error is lost. EPIC_SEAR (MCLF+218) bit<31:4> - to determine value of sysAdr<33:6> when error was logged. MCLF+1D8 bit<15:5> Bank 0 Base Address Register MCLF+1F0 bit<4:1> Bank 0 Configuation Register MCLF+1E0 bit<15:5> Bank 1 Base Address Register MCLF+1F8 bit<4:1> Bank 1 Configuation Register MCLF+1E8 bit<15:5> Bank 2 Base Address Register MCLF+200 bit<4:1> Bank 2 Configuation Register Compare Base Address Registers and order them Compare sysAdr <33:23> from sysBus Error Address Register to each and detemine which SIMM was being accessed. Configuration<4:1> encoding Bit<4:1> Memory Size Hex value 0000 1024 MB 0x7FFFF 0001 512 MB 0x3FFFF 0010 256 MB 0x1FFFF 0011 128 MB 0x0FFFF 0100 64 MB 0x07FFF 0101 32 MB 0x03FFF 0110 16 MB 0x01FFF 0111 8 MB 0x00FFF 1xxx Reserved
Faulting FRU:	SIMM, CPU module (400 Series), or motherboard (200 Series).

Machine Check Code 0x20A, Bcache Tag Address Parity Error

See Table 9-18 for information on machine check code 0x20A, Bcache tag address parity error .

Table 9-18. Bcache Tag Address Parity Error

Error name:	mchk$c_ctaperr
Register name:	COMA_EDSR bit<1> = 1 (MCLF+1A8)
Bit description:	Bcache Tag Address Parity Error Indicates that a tag probe encountered bad parity in the tag address RAM.
Recovery:	Not recoverable.
Analysis:	If COMA_EDSR bit<4> = 1 - a DMA transaction caused the error. Then COMA_EDSR bit<8:6> - ioCmd<2:0> state when error was logged If COMA_EDSR bit<4> = 0 - A CPU requested transaction caused error. Then COMA_EDSR bit<8:6> - cpuCReq<2:0> state when error was logged If COMA_EDSR bit<5> = 1 - A victim write caused the error.
Faulting FRU:	CPU module (400 Series), or motherboard (200 Series).

Machine Check Code 0x20B, Bcache Tag Control Parity Error

See Table 9-19 for information on machine check code 0x20B, Bcache tag control parity error .

Table 9-19. Bcache Tag Control Parity Error

Error name:	mchk$c_ctcperr
Register name:	COMA_EDSR bit<2> = 1 - (MCLF+1A8)
Bit description:	Bcache Tag Control Parity Error. Indicates that a tag probe encountered bad parity in the tag control RAM.
Recovery:	Not recoverable.
Analysis:	If COMA_EDSR bit<4> = 1 - A DMA transaction caused the error. Then COMA_EDSR bit<8:6> - ioCmd<2:0> state when error was logged If COMA_EDSR bit<4> = 0 - A CPU requested transaction caused error. Then COMA_EDSR bit<8:6> - cpuCReq<2:0> state when error was logged If COMA_EDSR bit<5> = 1 - A victim write caused the error.
Faulting FRU:	CPU module (400 Series), or motherboard (200 Series).

Machine Check Code 0x20C, Nonexistent Memory Error

See Table 9-20 for information on machine check code 0x20C, nonexistent memory error .

Table 9-20. Nonexistent Memory Error

Error name:	mchk$c_nxmerr
Register name:	COMA_EDSR bit<3> = 1 - (MCLF+1A8)
Bit description:	Nonexistent Memory Error. Indicates that a read or write occurred to an invalid address which does not map to any memory bank, CSR or I/O quadrant.
Recovery:	Not recoverable.
Analysis:	If COMA_EDSR bit<4> = 1 - A DMA transaction caused the error. Then COMA_EDSR bit<8:6> - ioCmd<2:0> state when error was logged If COMA_EDSR bit<4> = 0 - A CPU requested transaction caused error. Then COMA_EDSR bit<8:6> - cpuCReq<2:0> state when error was logged. If COMA_EDSR bit<5> = 1 - A victum write caused the error.
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).

Machine Check Code 0x20D, I/O Bus Error

See Table 9-21 for information on machine check code 0x20D, I/O bus error .

Table 9-21. I/O Bus Error

Error name:	mchk$c_siochk
Register name:	HIRR bit<5> = 1 (MCLF+140)
Bit description:	IRQ3 - NMI/SERR - This interrupt indicates that an ISA or PCI device detected an abnormal condition during a transaction.
Recovery:	Not recoverable.
Analysis:	An I/O option at address [EPIC_PEAR] asserted IOCHK. EPIC_DCSR (MCLF+208) bit<21:18> - pCmd field indicates the PCI cycle type when the PCI initiated error is logged. Refer to Table 9-1 for PCI Codes. EPIC_PEAR (MCLF+210) bit<31:0> - to determine value of AD<31:0> when error was logged. Read register at 1 C000 0C20 (SIO Status and Control Register). Bit<6> set indicates an ISA option reported the error. Bit<7> set indicates a PCI option reported the error.
Faulting FRU:	ISA option or PCI option.

Machine Check Code 0x80, Bcache Tag Parity Error

See Table 9-22 for information on machine check code 0x80, Bcache tag parity error .

Table 9-22. Bcache Tag Parity Error

Error name:	mchk$c_tperr
Register name:	BIU_STAT bit<3> = 1 (MCLF+168)
Bit description:	A backup cache tag probe encountered bad parity in the tag address RAM
Recovery:	Not recoverable.
Analysis:	BIU_STAT bit<6:4> - Indicates cycle type on the cReg_h pins when error occurred. BIU_ADDR - Contains the physical address associated with this error bits<7:0> BC_TAG - Backup Cache Tag Register null cycle If BC_TAG bit<0> = 1 Indicates the last operation before an error was logged was a HIT to backup cache BC_TAG bit<1> Contains the state of the TAGCTL_P control parity bit BC_TAG bit<2> Contains the state of the TAGCTL_D dirty bit BC_TAG bit<3> - Contains the state of the TAGCTL_S shared bit (n/a) BC_TAG bit<4> Contains the state of the TAGCTL_V Valid bit BC_TAG bit<21:5> Contains the value of TAG<33:17> BC_TAG bit<22> Contains the state of the TAG_P data parity bit
Faulting FRU:	CPU module (400 Series), or motherboard (200 Series).

Machine Check Code 0x82, Bcache Tag Control Parity Error

See Table 9-23 for information on machine check code 0x82, Bcache tag control parity error .

Table 9-23. Bcache Tag Control Parity Error

Error name:	mchk$c_tcperr	
Register name:	BIU_STAT bit<3> = 1 (MCLF+168)	
Bit description:	A backup cache tag probe encountered bad parity in the tag control RAM.	
Recovery:	Not recoverable.	
Analysis:	BIU_STAT bit<6:4>	Indicates cycle type on the cReg_h pins when error occurred.
	BIU_ADDR	Contains the physical address associated with this error bits<7:0>
	BC_TAG	Backup Cache Tag Register null cycle
	If BC_TAG bit<0> = 1	Indicates the last operation before an error was logged was a HIT to backup cache
	BC_TAG bit<1>	Contains the state of the TAGCTL_P control parity bit
	BC_TAG bit<2> -	Contains the state of the TAGCTL_D dirty bit
	BC_TAG bit<3> -	Contains the state of the TAGCTL_S shared bit (n/a)
	BC_TAG bit<4> -	Contains the state of the TAGCTL_V Valid bit
	BC_TAG bit<21:5>	Contains the value of TAG<33:17>
	BC_TAG bit<22>	Contains the state of the TAG_P data parity bit
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).	

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Machine Check Code 0x84, Hard Error

See Table 9-24 for information on machine check code 0x84, hard error .

Table 9-24. Hard Error

Error name:	mchk$c_herr
Register name:	BIU_STAT bit<1> = 1 (MCLF+168)
Bit description:	Indicates an CPU external cycle was terminated with a HARD_ERROR on cAck_h pins. This mode is not supported.
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	

Machine Check Code 0x86, Correctable ECC

See Table 9-25 for information on machine check code 0x86, correctable ECC .

Table 9-25. Correctable ECC

Error name:	mchk$c_ecc_c
Register name:	This machine check is not implemented in the 21064 CPU chip.
Bit description:	
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	

Machine Check Code 0x88, Noncorrectable ECC

See Table 9-26 for information on machine check code 0x88, noncorrectable ECC .

Table 9-26. Noncorrectable ECC

Error name:	mchk$c_ecc_nc
Register name:	This machine check is not implemented in the 21064 CPU chip.
Bit description:	
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	

Machine Check Code 0x8A, Unknown Error

See Table 9-27 for information on machine check code 0x8A, unknown error .

Table 9-27. Unknown Error

Error name:	mchk$c_unknown
Register name:	BIU_STAT (MCLF+168) EPIC_DCSR (MCLF+1A0) COMA_GCR (MCLF+208)
Bit description:	
Recovery:	
Analysis:	If none of the error registers contain a bit that is set to indicate an error, an unknown error machine check will result.
Faulting FRU:	

Machine Check Code 0x8C, Soft Error

See Table 9-28 for information on machine check code 0x8C, soft error .

Table 9-28. Soft Error

Error name:	mchk$c_Cacksoft
Register name:	BIU_STAT bit<2> = 1 (MCLF+168)
Bit description:	Indicates an CPU external cycle was terminated with a SOFT_ERROR on cAck_h pins. This mode is not supported.
Recovery:	Not recoverable.
Analysis:	If this error occurs, the ABOX_CTL bit<2> was set and a device returned a soft error code with Ack_h. This mode is not supported. ABOX_CTL bit<2> should be zero.
Faulting FRU:	

Machine Check Code 0x8E, Bugcheck

See Table 9-29 for information on machine check code 0x8E, bugcheck .

Table 9-29. Bugcheck

Error name:	mchk$c_bugcheck
Register name:	
Bit description:	
Recovery:	Not recoverable.
Analysis:	This machine check is the result of a breakpoint being executed in debug mode.
Faulting FRU:	

Machine Check Code 0x90, OS Bugcheck

See Table 9-30 for information on machine check code 0x90, OS bugcheck .

Table 9-30. OS Bugcheck

Error name:	mchk$c_os_bugcheck
Register name:	
Bit description:	
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	

Machine Check Code 0x92, Primary Cache Data Fill Error (Dcache)

See Table 9-31 for information on machine check code 0x92, primary cache data fill error (Dcache) .

Table 9-31. Primary Cache Data Fill Error (Dcache)

Error name:	mchk$c_dcperr	
Register name:	BIU_STAT bit<10> = 1 and BIU_STAT bit<11> = 0 (MCLF+168)	
Bit description:	Indicates that data with a parity error was received from Bcache or memory while performing a Dcache fill.	
Recovery:	Not recoverable.	
Analysis:	BIU_STAT bit<13:12>	Identifies the quadword within the hexaword primary cache fill block which caused the error.
	FILL_ADDR	Contains the physical address associated with this error in bits<14:8>
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).	

Machine Check Code 0x94, Primary Cache Data Fill Error (Icache)

See Table 9-32 for information on machine check code 0x94, primary cache data fill error (Icache) .

Table 9-32. Primary Cache Data Fill Error (Icache)

Error name:	mchk$c_icperr	
Register name:	BIU_STAT bit<10> = 1 and BIU_STAT bit<11> = 1 (MCLF+168)	
Bit description:	Indicates that data with a parity error was received from Bcache or memory while performing a Icache fill.	
Recovery:	Not recoverable.	
Analysis:	BIU_STAT bit<13:12>	Identifies the quadword within the hexaword primary cache fill block which caused the error.
	FILL_ADDR	Contains the physical address associated with this error in bits<14:8>
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).	

Primary Cache Fill ECC Error

See Table 9-33 for information on the primary cache fill ECC error .

Table 9-33. Primary Cache Fill ECC Error

Error name:	
Register name:	BIU_STAT bit<8> = 1 (MCLF+168)
Bit description:	Indicates that the data received from outside the CPU contained an ECC error during a primary cache data fill operation.
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).

ADDITIONAL ERRORS

The following error bits may be set but do not have an associated machine check code. Review of these need to be made in order to assure having determinate errors.

Bcache Multiple Error

See Table 9-34 for information on the Bcache multiple error .

Table 9-34. Bcache Multiple Error

Error name:	
Register name:	BUI_STAT bit<7> = 1 (MCLF+168)
Bit description:	Indicates a *fatal error* was reported from the Comanche chip or bit<3 or 4> are set while an error was being logged into this register.
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).

Lost Error

See Table 9-35 for information on the lost error .

Table 9-35. Lost Error

Error name:	
Register name:	EPIC_DCSR bit<0> = 1 (MCLF+208)
Bit description:	Lost Error. Multiple errors occurred when an error address was already locked. *This error is fatal.*
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).

Primary Cache Multiple Error

See Table 9-36 for information on the primary cache multiple error .

Table 9-36. Primary Cache Multiple Error

Error name:	
Register name:	BIU_STAT bit<14> = 1 (MCLF+168)
Bit description:	Indicates that a primary cache fill operation resulted in parity error while bit<10 or 8> were set.
Recovery:	Not recoverable.
Analysis:	
Faulting FRU:	CPU module (400 Series) or motherboard (200 Series).

10

Connector and Cable Information

Overview

This chapter presents information on connectors and cables used in the Digital AlphaStation 200 and 400 Series systems, according to the following topics:

- AlphaStation 200 Series system internal connectors
- AlphaStation 400 Series system connectors and cables
- PCI slots
- ISA expansion slots
- External connectors
- Internal cables

AlphaStation 200 Series System Internal Connectors

Motherboard

This section describes the internal connectors on the Digital AlphaStation 200 Series system motherboard.

Serial Diagnostic Port

The serial diagnostic port, J7, on the motherboard is a 10-pin male connector. The port is designed to support system testing during manufacturing. You need an adapter to use a standard DECconnect cable. Table 10-1 identifies the diagnostic port's pins and signals.

Table 10-1. Serial Diagnostic Port Connector Pinout

Pin	Signal	Pin	Signal
1	Open	6	BSROMOE_L
2	Ground	7	SROMOVRD
3	+12 Volt	8	VDD
4	Ground	9	BSROMCLK
5	Ground	10	SROMCDAT

Speaker Connector

The Digital AlphaStation 200 Series system motherboard has a connector, J18, for the internal speaker. If the sound card is installed, the speaker is attached to the sound card directly and J18 is unused. Table 10-2 identifies the speaker connector pins and signals.

Table 10-2. AlphaStation 200 Series System Speaker Connector Pinout

Signal	Pin
+5 Volt (VDD)	1
Open	2
Open	3
Speaker signal	4

Floppy Disk Controller

The Digital AlphaStation 200 Series system motherboard contains a National PC87332 Super I/O chip. The floppy disk controller (FDC) portion of the Super I/O chip is routed to connector J16 on the motherboard. Table 10-3 lists the signals and pins for connector J16.

Table 10-3. Floppy Device Controller Connector Pinouts

Signal	Pin	Signal	Pin
DENSEL	2	Ground	1
-MTR3	4	Ground	3
DRATE0	6	Ground	5
-INDEX	8	Ground	7
-MTR0	10	Ground	9
-DR1	12	Ground	11
-DR0	14	Ground	13
-MTR1	16	Ground	15
-DIR	18	Open	17
-STEP	20	Ground	19
-WRDATA	22	Ground	21
-WGATE	24	Ground	23
-TRK0	26	Ground	25
-WP	28	Open	27
-RDDATA	30	Ground	29
-HDSEL	32	Ground	31
-DISKCH	34	Ground	33

Sound Card Connector

The Digital AlphaStation 200 Series system has a private 90-pin connector, J23, on the motherboard for a custom sound card. The connector is logically on the ISA bus, although neither the connector nor the sound card is ISA-standard.

Front-Panel Lights and Switches Connector

The Digital AlphaStation 200 Series system control and indicator panel is connected to J5 on the motherboard. The front-panel board of the Digital AlphaStation 200 Series system includes two LEDs (power on and disk busy) and a reset switch. A short cable connects the front panel to the motherboard. Table 10-4 lists the signals and pin numbers for the front-panel connector pinouts.

Table 10-4. AlphaStation 200 Series System Front-Panel Connectors

Signal	Pin
Disk busy LED	1
LED power	2
Reset switch input	3
VDD	4
Open (key)	5
Ground	6
Ground	7

Internal SCSI Bus Connector J15

The Digital AlphaStation 200 Series system has a 50-pin SCSI bus connector on the motherboard designed for SCSI devices mounted within the system enclosure. Table 10-5 identifies the internal SCSI bus connector's pins and signals.

Table 10-5. Internal SCSI Bus Connector

Signal	Pin	Signal	Pin
-SCSI_D0	2	Ground	1
-SCSI_D1	4	Ground	3
-SCSI_D2	6	Ground	5
-SCSI_D3	8	Ground	7
-SCSI_D4	10	Ground	9
-SCSI_D5	12	Ground	11
-SCSI_D6	14	Ground	13
-SCSI_D7	16	Ground	15
-SCSI_PAR	18	Ground	17
Ground	20	Ground	19
Ground	22	Ground	21
Reserved	24	Reserved	23
TERMPWR	26	Open	25
Reserved	28	Reserved	27
Ground	30	Ground	29
-SCSI_ATN	32	Ground	31
Ground	34	Ground	33
-SCSI_BSY	36	Ground	35
-SCSI_ACK	38	Ground	37
-SCSI_RST	40	Ground	39
-SCSI_MSG	42	Ground	41
-SCSI_SEL	44	Ground	43
-SCSI_CD	46	Ground	45
-SCSI_REQ	48	Ground	47
-SCSI_IO	50	Ground	49

Power Connectors

The Digital AlphaStation 200 Series system motherboard has two connector that receive power from the power supply. The connectors, J19 and J20, are 12 pins each. Table 10-6 identifies the pins and voltages.

Table 10-6. AlphaStation 200 Series System Motherboard Power Connectors

J19		J20	
Voltage	**Pin**	**Voltage**	**Pin**
Open	1	Ground	1
VDD	2	Ground	2
+12 Volt	3	Ground	3
-12 Volt	4	+3.3 Volt	4
Ground	5	+3.3 Volt	5
Ground	6	+3.3 Volt	6
Ground	7	+3.3 Volt	7
Ground	8	+3.3 Volt	8
-5 Volt	9	+3.3 Volt	9
VDD	10	Ground	10
VDD	11	Ground	11
VDD	12	Ground	12

Fan Connector

The Digital AlphaStation 200 Series system may have either a 210-watt or a 180-watt power supply. In systems that have the the 210-watt supply, the system fan is powered directly from the power supply. In systems that have the 180-watt supply, the fan is connected to the J29 on the motherboard. J29 is a 2-pin connector, where pin 1 is +12 Volts and pin 2 is ground.

Riser Card

The Digital AlphaStation 200 Series system riser card plugs directly into the motherboard. The riser card contains connectors for PCI bus and ISA bus options as well as a 20-pin connector, J1. The Ethernet LAN controller uses J1 for attachment unit interface (AUI) signals going to and from the media adapter unit (MAU) .

The riser also has a connector for the MAU. This 20-pin connector, J1, attaches the card to the Ethernet LAN controller located on the riser card. Table 10-7 identifies the signals and pins on MAU connector J1.

Table 10-7. Media Adapter Unit AUI Pinouts

Signal	Pin	Signal	Pin
AUITDP	1	AUITDM	2
AUICDP	3	AUICDM	4
AUIRDP	5	AUIRDM	6
TPRDM	7	TPRDP	8
TPOD	9	TPOB	10
TPOA	11	TPOC	12
Ground	13	-BUF_LINK_PASS_LED	14
Ground	15	-BUF_NET_ACTIVE_LED	16
Ground	17	+12 Volt	18
Ground	19	VDD	20

Sound Card

The Digital AlphaStation 200 Series system sound card has three internal connectors (J5, J6, and J8), as Table 10-8 shows.

Table 10-8. AlphaStation 200 Series System Sound Card Connectors

Connector	Type	Pin	Connection
J5	4-pin header	1	4-32-Ohm speaker
		2	Unconnected
		3	Unconnected
		4	Ground
J6	4-pin header	1	Left channel in from CD-ROM
		2	Ground
		3	Ground
		4	Right channel in from CD-ROM
J8			Unused
J9	Jumpers	N/A	N/A

AlphaStation 400 Series System Connectors and Cables

Motherboard

This section describes the floppy and front-panel lights and switches connectors for the AlphaStation 400 Series system.

Floppy

Table 10-9 lists the signals and pins for the Digital AlphaStation system floppy device controller (FDC) connector pinouts.

Table 10-9. Floppy Device Controller Connector Pinouts

Signal	Pin	Signal	Pin
DENSEL	2	Ground	1
MTR3\	4	Ground	3
DRATE0	6	Ground	5
INDEX\	8	Ground	7
MTR0\	10	Ground	9
DR1\	12	Ground	11
DR0\	14	Ground	13
MTR1\	16	Ground	15
DIR\	18	Open	17
STEP\	20	Ground	19
WRDATA\	22	Ground	21
WGATE\	24	Ground	23
TRK0\	26	Ground	25
WP\	28	Open	27
RDDATA\	30	Ground	29
HDSEL\	32	Ground	31
DISKCH\	34	Ground	33

Front-Panel Lights and Switches Connector

The front-panel board of the Digital AlphaStation 400 Series system includes three LEDs: power on, disk busy, and turbo (the turbo LED is unused), as well as a reset switch. A short cable connects the front panel to the motherboard. Table 10-10 lists the signals and pin numbers for the Digital AlphaStation 400 Series system front-panel connector pinouts.

Table 10-10. AlphaStation 400 Series System Front-Panel Connector Pinouts (J31)

Signal	Pin
Ground	1
Ground	2
+5 Volt	3
Open	4
Reset switch input	5
Turbo LED (STURBO L)	6
Power-on LED (SPOWER H)	7
Disk busy LED (HDACTIVE L)	8

- Internal SCSI Bus
- Power Connectors
- Memory SIMM Connectors
- CPU Module Connector

CPU Module: Serial Diagnostic Port

The Digital AlphaStation Series system's serial diagnostic port (Table 10-11), a 10-pin connector, is located inside the system enclosure and is not normally accessible. You need an adapter in order to use a standard DECconnect cable.

Table 10-11. Serial Diagnostic Port Connector Pinout

Signal	Pin	Pin	Description
Open	1	6	BSROMOE_L
Ground	2	7	SROMOVRD
+12 Volt	3	8	Vdd
Ground	4	9	BSROMCLK
Ground	5	10	SROMCDAT

PCI Slots

Notice that Table 10-12 does not match the pin numbering in the PCI specification. The position of the signals is the same, although the pin numbers are different.

Table 10-12. PCI Slot Connector Pinouts

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
Open	1	61	-12 Volt	AD18	31	91	+3.3 Volt
+12 Volt	2	62	Open	AD16	32	92	AD17
Open	3	63	Ground	+3.3 Volt	33	93	CBE2#
Open	4	64	Open	FRAME#	34	94	Ground
Vdd	5	65	Vdd	Ground	35	95	IRDY#
INTA#	6	66	Vdd	TRDY#	36	96	+3.3 Volt
INTC#	7	67	INTB#	Ground	37	97	DEVSEL#
Vdd	8	68	INTD#	STOP#	38	98	Ground
Open	9	69	Open	+3.3 Volt	39	99	PCILOCK #
Vdd	10	70	Open	Open	40	100	PERR#
Open	11	71	Open	Open	41	101	+3.3 Volt
Ground	12	72	Ground	Ground	42	102	SERR#
Ground	13	73	Ground	PAR	43	103	+3.3 Volt
Open	14	74	Open	AD15	44	104	CBE1#
PCI_ RESET#	15	75	Ground	+3.3 Volt	45	105	AD14
vdd	16	76	PCICLK	AD13	46	106	Ground
PCI_GNT#	17	77	Ground	AD11	47	107	AD12
Ground	18	78	PCI_REQ#	Ground	48	108	AD10
Open	19	79	Vdd	AD09	49	109	Ground

Table 10-12. PCI Slot Connector Pinouts *(continued)*

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
AD30	20	80	AD31	CBE0#	50	110	AD08
+3.3 Volt	21	81	AD29	+3.3 Volt	51	111	AD07
AD28	22	82	Ground	AD06	52	112	+3.3 Volt
AD26	23	83	AD27	AD04	53	113	AD05
Ground	24	84	AD25	Ground	54	114	AD03
AD24	25	85	+3.3 Volt	AD02	55	115	Ground
IDSEL	26	86	CBE3#	AD00	56	116	AD01
+3.3 Volt	27	87	AD23	Vdd	57	117	Vdd
AD22	28	88	Ground	Open	58	118	Open
AD20	29	89	AD21	Vdd	59	119	Vdd
Ground	30	90	AD19	Vdd	60	120	Vdd

ISA Expansion Slots

Table 10-13 lists the ISA slot connector pinouts for the Digital AlphaStation 200 and 400 Series systems.

Table 10-13. ISA Slot Connector Pinouts

Signal	Pin	Pin	Signal
IOCHK\	1	32	Ground
SD07	2	33	RSTDRV
SD06	3	34	Vdd
SD05	4	35	IRQ9
SD04	5	36	-5 Volt
SD03	6	37	DREQ2
SD02	7	38	-12 Volt
SD01	8	39	ZEROWS\
SD00	9	40	+12 Volt
IOCHRDY	10	41	Ground
AEN	11	42	SMEMW\
SA19	12	43	SMEMR\
SA18	13	44	IOWC\
SA17	14	45	IORC\
SA16	15	46	DACK3\
SA15	16	47	DREQ3
SA14	17	48	DACK1\
SA13	18	49	DREQ1
SA12	19	50	REFRESH\
SA11	20	51	SYSCLK
SA10	21	52	IRQ7
SA09	22	53	IRQ6
SA08	23	54	IRQ5
SA07	24	55	IRQ4

Table 10-13. ISA Slot Connector Pinouts *(continued)*

Signal	Pin	Pin	Signal
SA06	25	56	IRQ3
SA05	26	57	DACK2\
SA04	27	58	EOP
SA03	28	59	BALE
SA02	29	60	Vdd
SA01	30	61	OSC
SA00	31	62	Ground
SBHE\	63	81	MEMCS16\
LA23	64	82	IOCS16\
LA22	65	83	IRQ10
LA21	66	84	IRQ11
LA20	67	85	IRQ12
LA19	68	86	IRQ15
LA18	69	87	IRQ14
LA17	70	88	DACK0\
MRDC\	71	89	DREQ0
MWTC\	72	90	DACK5\
SD08	73	91	DREQ5
SD08	74	92	DACK6\
SD08	75	93	DREQ6
SD08	76	94	DACK7\
SD08	77	95	DREQ7
sd08	78	96	Vdd
SD08	79	97	MASTER\
SD08	80	98	Ground

External Connectors

The external connectors of the Digital AlphaStation 200 Series systems allow for a number of cables and devices to be attached, as Figure 10-1 and Table 10-14 show.

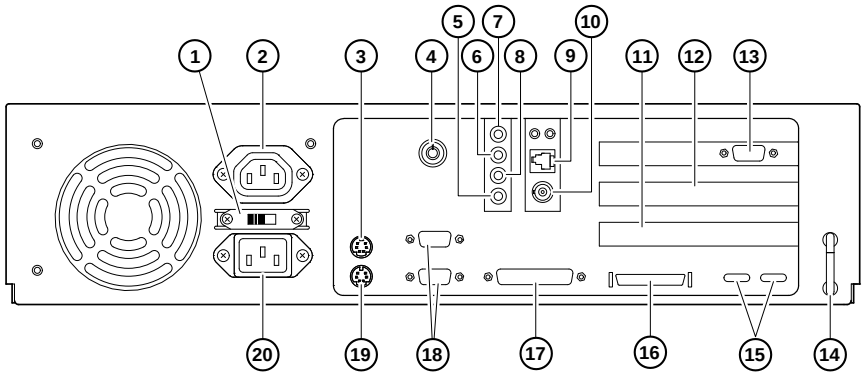


Figure 10-1. AlphaStation 200 Series System Rear Connectors

Table 10-14. AlphaStation 200 Series System Rear Connectors

Figure Legend	Connector	Function
1	Voltage selector switch	Allows you to set your system to work with 115 or 230 Volts AC power.
2	Monitor power connector	Use to connect a monitor to AC power. *If your monitor consumes more than 2 Amps at 115 Volts (1 Amp at 230 Volts), connect it directly to your wall outlet.* This connector may be missing from future versions of the system.
3	Keyboard connector	Use to connect a 101- or 102-key keyboard.
4	System (chassis) lock	Locks top cover.

Table 10-14. AlphaStation 200 Series System Rear Connectors *(continued)*

Figure Legend	Connector	Function
5	Sound card line in connector	Brings audio signals into the card (for example, from a stereo amplifier).
6	Sound card line out connector	Routes audio signals to an external amplifier.
7	Sound card headphone jack	Connector for the headphones or amplified speakers.
8	Sound card microphone jack	Connector for the microphone.
9	Twisted pair connector	Connection to the embedded Ethernet controller .
10	ThinWire connector	Connection to the embedded Ethernet controller .
11	ISA expansion slot	Used for half-size ISA expansion options only.
12	PCI/ISA expansion slot	Either a PCI or ISA option can use this slot.
13	PCI expansion slot	Used for PCI expansion options. (In earlier systems, this slot was a PCI/ISA combo slot. The slot was changed to PCI only to support two-board PCI options.) In this example, a PCI graphics adapter is in the slot.
14	Security loop	Attaches padlock and security cable.
15	LED viewing ports	Ports for viewing diagnostic LED indicators.
16	SCSI port	Provides the interface between the system unit and external SCSI devices.
17	Enhanced bidirectional parallel port	Connects an industry-standard parallel printer or other parallel device.
18	Serial port connectors	Connects serial devices.
19	Mouse connector	Connects a PS/2-compatible mouse.
20	AC power connector	Connects the system to AC power.

The external connectors of the Digital AlphaStation 400 Series systems allow for a number of cables and devices to be attached, as Figure 10-2 and Table 10-15 show.

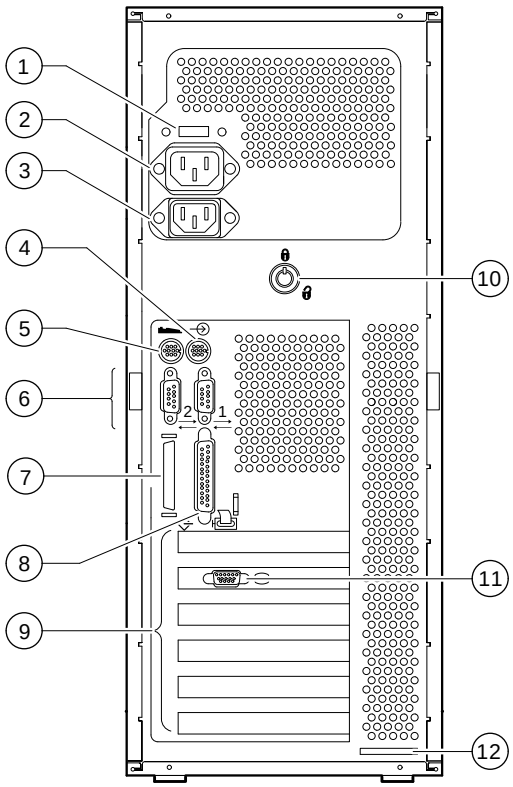


Figure 10-2. AlphaStation 400 Series System Rear Connectors

Table 10-15. AlphaStation 400 Series System Rear Connectors

Figure Legend	Connector	Function
1	Voltage selector switch	Allows you to set your system to work with 115 or 230 Volt AC power.
2	Monitor power connector	Connects a monitor to AC power. *If your monitor consumes more than 2 Amps at 115 Volt (1 Amp at 230 Volt), connect it directly to your wall outlet.*
3	AC power connector	Connects the system to AC power.
4	Mouse connector	Connects a PS/2-compatible mouse.
5	Keyboard connector	Connects a 101- or 102-key keyboard.
6	Serial port connectors	Connects serial devices.
7	SCSI connector	Provides the interface between the system unit and external SCSI devices.
8	Parallel port connector	Allows you to connect an industry-standard parallel printer.
9	Expansion board slots	Allow you to install up to two full-size PCI, up to three full-size ISA, and one additional PCI or ISA expansion boards.
10	System (chassis) lock	Locks outside panels.
11	Video port (on option module)	Provides the interface between video/graphics expansion module (option) and the supported monitor.
12	Security loop	Attaches security lock or cable.

Table 10-16 shows the external cables for the AlphaStation 400 Series system.

Table 10-16. AlphaStation 400 Series System External Connectors

External Connector	Purpose
SCSI	High-density, single-ended 50-pin shielded device connector.
Keyboard	Standard workstation keyboard connector.
Mouse	Standard PC mouse connector.
COM1, COM2	Standard PC nine-pin communication connectors.
Parallel port	Enhanced parallel port.

Parallel Port

Table 10-17 lists the signals and pin positions for Digital AlphaStation parallel port connector pinouts.

Table 10-17. Parallel Port Connector Pinout

Signal	Pin
PSTRB\	1
PDAT0	2
PDAT1	3
PDAT2	4
PDAT3	5
PDAT4	6
PDAT5	7
PDAT6	8
PDAT7	9
PACK\	10
PBUSY	11
PE	12
SLCT	13
PAUTOFD\	14
PERROR\	15
PINIT\	16
PSLCTIN\	17
Ground	18
Ground	19
Ground	20
Ground	21
Ground	22
Ground	23
Ground	24
Ground	25

Serial Line Units

COM1/2 Pinouts

Table 10-18 lists the signals and pin positions for the Digital AlphaStation COM1 and Com2 connector pinouts.

Table 10-18. COM1 and COM 2 Connector Pinouts

Signal	Pin
DCD	1
RX	2
TX	3
DTR	4
Ground	5
DSR	6
RTS	7
CTS	8
RI	9

SCSI

The relative position of signals (Table 10-19) on the Digital AlphaStation Series system's internal and external connectors are the same; however, the conventions for pin numbering differ between the two. Pin 36 on the external connector is used to disable the on-board active terminator when the pin is grounded by an external device.

Table 10-19. SCSI Connector Pinouts

Signal	Internal	External	Signal	Internal	External
DB0\	2	26	Ground	1	1
DB1\	4	27	Ground	3	2
DB2\	6	28	Ground	5	3
DB3\	8	29	Ground	7	4
DB4\	10	30	Ground	9	5
DB5\	12	31	Ground	11	6
DB6\	14	32	Ground	13	7
DB7\	16	33	Ground	15	8
DBP\	18	34	Ground	17	9
Ground	20	35	Ground	19	10
Ground	22	36	Ground	21	11
Reserved	24	37	Reserved	23	12
TERMP WR	26	38	Open	25	13
Reserved	28	39	Reserved	27	14
Ground	30	40	Ground	29	15
ATN\	32	41	Ground	31	16
Ground	34	42	Ground	33	17
BSY\	36	43	Ground	35	18
ACK\	38	44	Ground	37	19
RST\	40	45	Ground	39	20
MSG\	42	46	Ground	41	21
SEL\	44	47	Ground	43	22
C/D\	46	48	Ground	45	23
REQ\	48	49	Ground	47	24
I/O\	50	50	Ground	49	25

Connector Pinouts

Pin 36 on the Digital AlphaStation Series system's external SCSI connector controls an active SCSI terminator. When an external cable is plugged in, a low-level ground is sensed on this circuit, which disables the on-board terminator. In this case, a device at the end of the external SCSI cable must provide far-end bus termination.

Keyboard/Mouse

Table 10-20 lists the signals and pin positions for the Digital AlphaStation Series system keyboard connector pinouts.

Table 10-20. Keyboard Connector Pinouts

Signal	Pin
KBDATA	1
Open	2
Ground	3
+5 Volt	4
KBCLK	5
Open	6

Table 10-21 lists the signals and pin positions for the Digital AlphaStation Series system mouse connector pinouts.

Table 10-21. Mouse Connector Pinouts

Signal	Pin
MSDATA	1
Open	2
Ground	3
+5 Volt	4
MSCLK	5
Open	6

Internal Cables

The Digital AlphaStation 200 Series system includes several internal cables, as Table 10-22 illustrates.

Table 10-22. AlphaStation 200 Series System Internal Cables

Internal Cable	Purpose
Speaker	Attaches internal speaker to either the motherboard or the audiocard.
SCSI	Connects internal SCSI device to SCSI controller on the motherboard. A SCSI terminator must be installed on the SCSI device at the end of this cable.
Floppy	Connects an internal floppy drive and optional internal tape drive to a controller on the motherboard.
MAU	*Optional:* Connects to the Ethernet controller on the riser card.
Front-panel	Attaches the front-panel lights and switches board to the motherboard.
Power (several)	Permanently attached to the power supply and provide power, ground, and fan speed control to the motherboard.

Sound Card

The connectors for the Digital AlphaStation 200 Series system sound card are shown in Table 10-23 .

Table 10-23. AlphaStation 200 Series System Sound Card Connectors

Connector	Type	Pin	Connection
J7 (top)	3.5-mm jack	N/A	Stereo headphones
J4 (2nd)	3.5-mm jack	N/A	Stereo line out
J2 (3rd)	3.5-mm jack	N/A	Monaural electret microphone (2.2 kOhm to 2.5 Volt)
J3 (bottom)	3.5-mm jack	N/A	Stereo line in
J5	4-pin header	1	4-32-Ohm speaker

Table 10-23. AlphaStation 200 Series System Sound Card Connectors *(continued)*

Connector	Type	Pin	Connection
		2	Unconnected
		3	Unconnected
		4	Ground
J6	4-pin header	1	Left channel in from CD-ROM
		2	Ground
		3	Ground
		4	Right channel in from CD-ROM

Table 10-24 lists and describes the internal cables for the Digital AlphaStation 400 Series system.

Table 10-24. AlphaStation 400 Series System Internal Cables

Internal Cable	Purpose
SCSI bus	Connects internal SCSI devices to SCSI controller on the motherboard. A SCSI terminator must be installed on the SCSI device at the end of this cable.
Floppy disk controller	Connects an internal floppy drive and optional internal tape drive to a controller on the motherboard.
Front-panel	Attaches the front-panel lights and switches board to the motherboard.
Power (several)	Permanently attached to the power supply and provide power, ground, and CPU fan-speed control to the motherboard.

11
Registers

Overview

This chapter contains brief descriptions of the registers in the Digital AlphaStation 200 and 400 Series systems. For full register descriptions, refer to the appropriate documents as noted. The registers are organized by sections , as outlined below:

- CPU registers. (Refer to *DECchip 21064 and 21064A Microprocessor Hardware Reference Manual*, order number EC-Q9ZUA-TE, Digital Equipment Corporation.)
- Cache and memory control CSRs. (Refer to *DECchip 21071/21072 Core Chip Sets Data Sheet*, order number EC-N0648-72, Digital Equipment Corporation.)
- PCI bus bridge CSRs. (Refer to *DECchip 21071/21072 Core Chip Sets Data Sheet* , order number EC-N0648-72, Digital Equipment Corporation.)
- PCI Bus Device Registers
  - PCI to ISA bridge. (*Intel 82378ZB Data Book*, Intel)
  - AlphaStation 200 Series Ethernet controller. (Refer to *DECchip 21040 Ethernet Controller Data Sheet*,order number EC-N0752-72, Digital Equipment Corporation.)
  - SCSI controller. (Refer to *NCR 53C810 PCI-SCSI I/O Processor Data Manual*, NCR.)
- ISA Bus Device Registers
  - Super I/O III chip. (Refer to *PC87332 Super I/O III Chip*, National Semiconductor.)
  - Keyboard controller. (Refer to *8242 Keyboard Controller Specification*, Intel, PHOENIX Technologies, Ltd.)

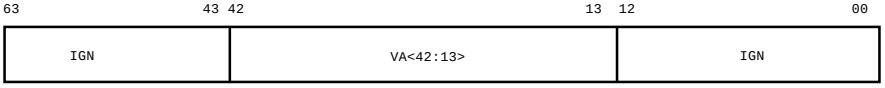
CPU Registers

Access the internal CPU registers by using the HW_MTPR (Move To Processor Register) and HW_MFPR (Move From Processor Register) instructions.

☞ Refer to the *DECchip 21064 and 21064A Microprocessor Hardware Reference Manual*, order number EC-Q9ZUA-TE, Digital Equipment Corporation.

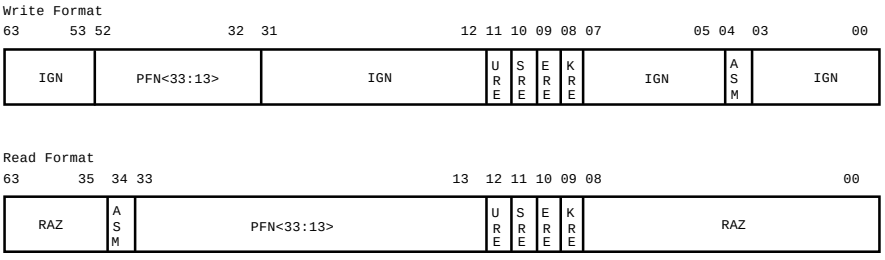
Translation Buffer Tag (TB_TAG) Register

The TB_TAG register is a write-only register that holds the tag for the next translation buffer update operation in the Instruction Translation Buffer or the Data Translation Buffer.



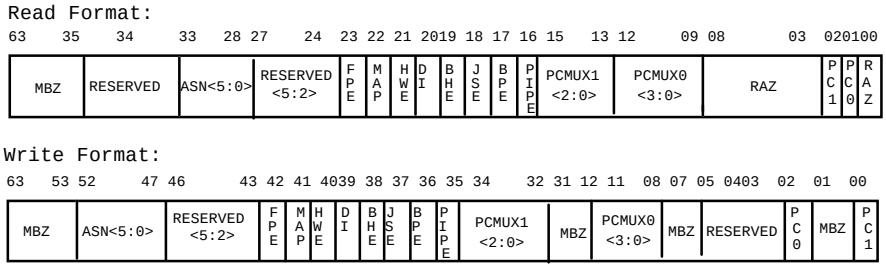
Instruction Translation Buffer Page Table Entry (ITB_PTE) Register

The ITB_PTE register is a read/write register, representing 12-page table entries split into two distinct arrays. The first 8-page table entries provide small-page (8-KByte) translations while the remaining 4 provide large (4 MByte) translations.



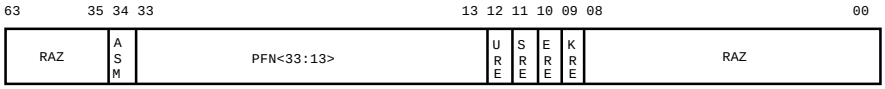
Instruction Cache Control and Status Register (ICCSR)

The ICCSR contains various Ibox hardware enables.



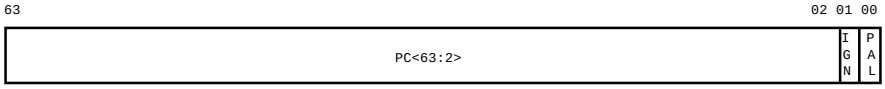
Instruction Translation Buffer Page Table Entry Temp (ITB_PTE_TEMP) Register

The ITB_PTE_TEMP register is a read-only holding register for ITB_PTE read data.



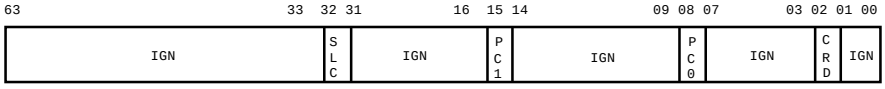
Exceptions Address (EXC_ADDR) Register

The EXC_ADDR register is a read/write register used to restart the machine after exceptions or interrupts.



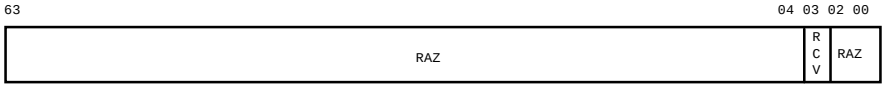
Clear Serial Line Interrupt Register (SL_CLR)

The SL_CLR register is a write-only register that clears the serial line interrupt request, performance counter interrupt requests, and CRD (corrected read data) interrupt requests.



Serial Line Receive (SL_RCV) Register

The SL_RCV register contains a single read-only bit (RCV). This bit provides an on-chip serial line function.



Instruction Translation Buffer ZAP (ITBZAP) Register

A write to the ITBZAP register invalidates all 12 translation buffer (ITB) entries.

Instruction Translation Buffer ASM (ITBASM) Register

A write to the ITBASM register invalidates all ITB entries in which the ITB_PTE ASM bit is equal to zero.

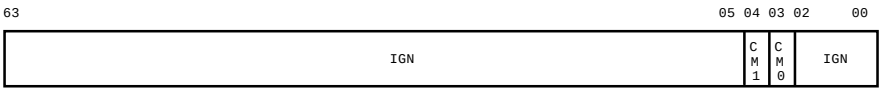
Instruction Translation Buffer IS (ITBIS) Register

A write to the ITBIS register invalidates all 12 translation buffer (ITB) entries.

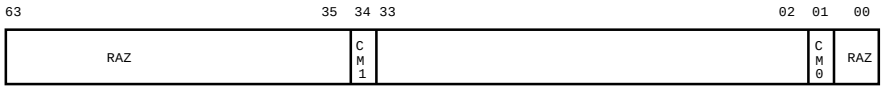
Processor Status (PS) Register

The PS register is a read/write register containing only the current mode bits of the architecturally defined PS.

Write Format

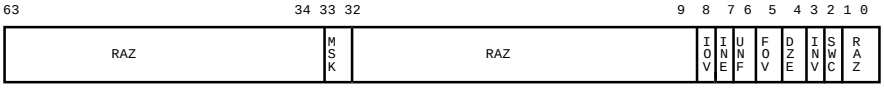


Read Format



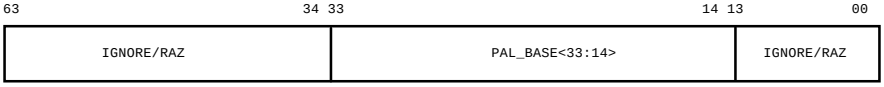
Exception Summary (EXC_SUM) Register

The EXC_SUM register contains various types of arithmetic traps that have occurred since the last time the register was written to (cleared). Any write to the EXC_SUM register clears bits <08:02>.



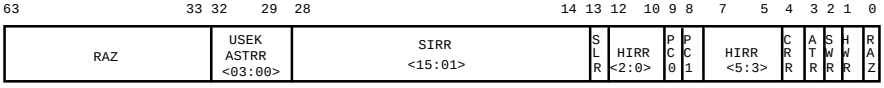
PAL Base Address (PAL_BASE) Register

The PAL_BASE address register is a read/write register containing the base address for the PALcode.



Hardware Interrupt Request Register (HIRR)

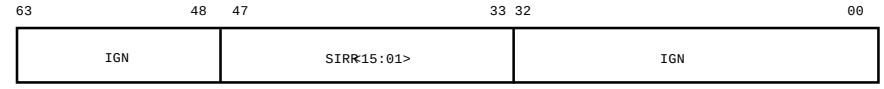
The hardware interrupt request register is a read-only register that provides a record of all currently outstanding interrupt requests and summary bits at the time of a read.



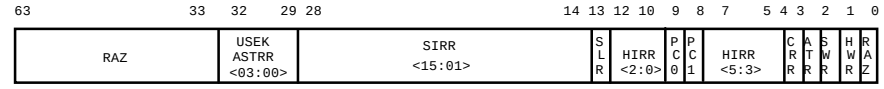
Software Interrupt Request Register (SIRR)

The SIRR is a read/write register used to control software interrupt requests.

Write Format:



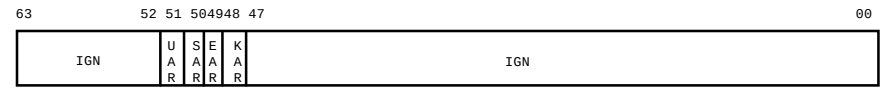
Read Format:



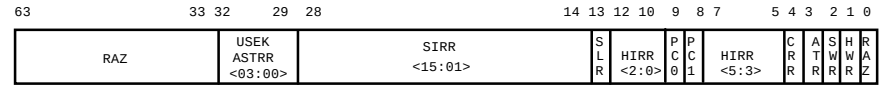
Asynchronous Trap Request Register (ASTRR)

The ASTRR is a read/write register containing bits to request AST interrupts in each of the processor modes.

Write Format:



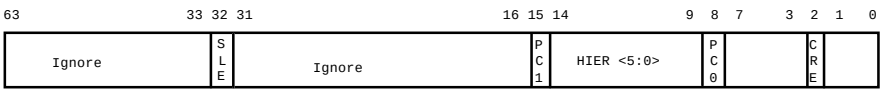
Read Format:



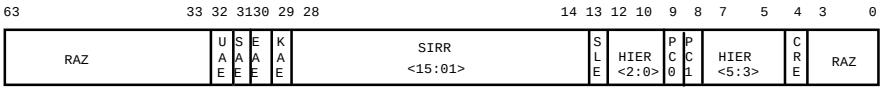
Hardware Interrupt Enable Register (HIER)

The hardware interrupt enable register enables interrupts from the corresponding bits of the hardware interrupt request register (HIRR).

For Writes:



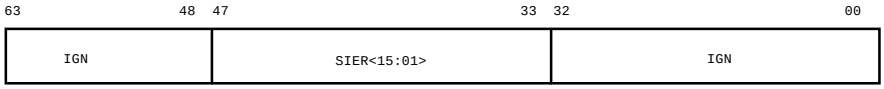
For Reads:



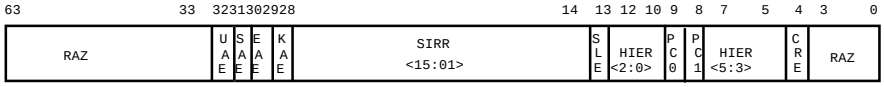
Software Interrupt Enable Register (SIER)

The SIER is a read/write register that enables corresponding bits of the SIRR requesting interrupts.

For Writes:



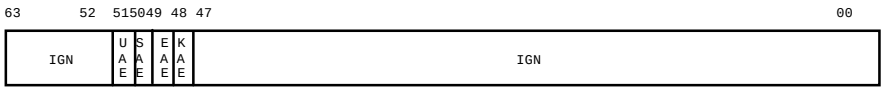
For Reads:



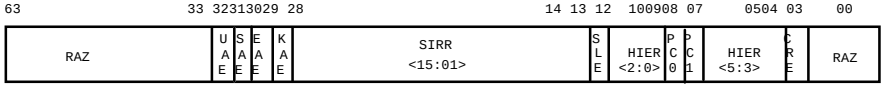
AST Interrupt Enable Register (ASTER)

The ASTER is a read/write register that enables corresponding bits of the ASTRR requesting interrupts.

For Writes:

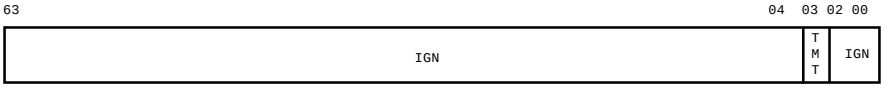


For Reads:



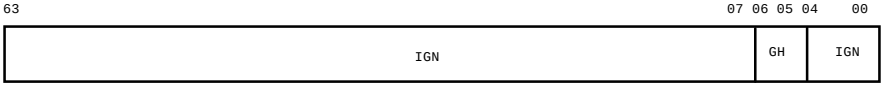
Serial Line Transmit Register (SL_XMIT)

The SL_XMIT register contains a single write-only bit (TMT). The bit provides an on-chip serial line function.



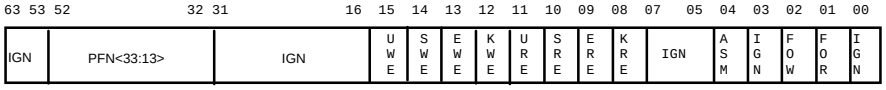
Translation Buffer Control (TB_CTL) Register

The TB_CTL register contains the granularity hint (GH) field. The GH field selects between the 21064/21064A TB page-mapping sizes.



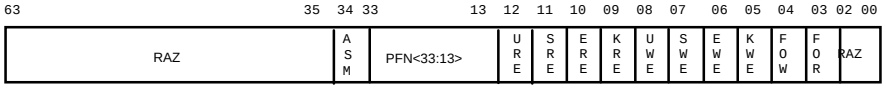
Data Translation Buffer Page Table Entry Register (DTB_PTE)

The DTB_PTE register is a read/write register representing the 32-entry DTB.



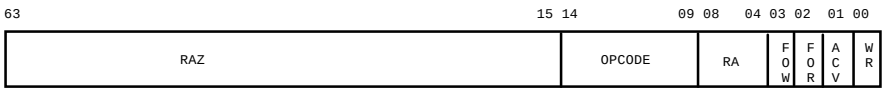
Data Translation Buffer Page Table Entry Temporary (DTB_PTE_TEMP) Register

The DTB_PTE_TEMP register is a read-only holding register for DTB_PTE read data.



Memory Management Control and Status Register (MM_CSR)

The MM_CSR is used latch and save information about data stream faults.



Virtual Address (VA) Register

The VA register latches the effective VA associated with D-stream faults or DTB misses. The VA and the MM_CSR are locked against further updates until the software reads the VA register.

Data Translation Buffer ZAP (DTBZAP) Register

The DTBZAP is a pseudo register. A write to this register invalidates all 32 DTB entries.

Data Translation Buffer ASM (DTBASM) Register

The DTBASM is a pseudo register. A write to this register invalidates all 32 DTB entries in which the ASM bit is equal to zero.

Data Translation Buffer Invalidate Single (DTBIS) Register

The DTBIS is a pseudo register. A write to this register invalidates the DTB entry that maps the virtual address help in the integer register.

Flush Instruction Cache (FLUSH_IC) Register

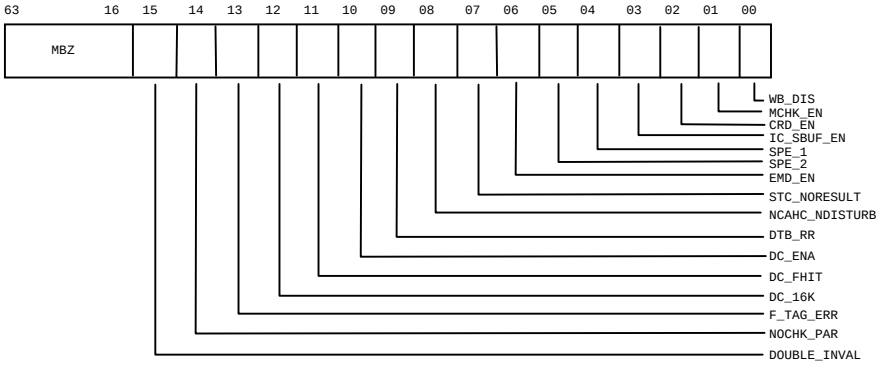
The FLUSH_IC is a pseudo register. A write to this register flushes the entire instruction cache.

Flush Instruction Cache ASM (FLUSH_IC_ASM) Register

The FLUSH_IC_ASM is a pseudo register. A write to this register invalidates all Icache blocks in which the ASM bit is clear.

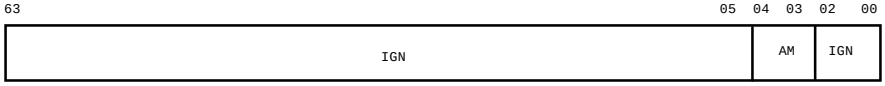
Abox Control Register

The Abox control register is a *write-only register*. It is included only to show what it controls.



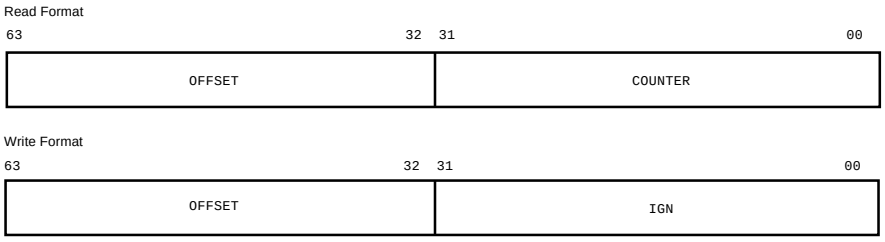
Alternate Processor Mode (ALT_MODE) Register

The ALT_MODE register is a write-only register. It contains the AM field that is used to specify the alternate processor mode used by HW_LD and HW_ST instructions that have their ALT bit set.



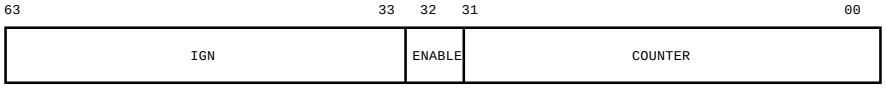
Cycle Counter (CC) Register

When enabled, the CC register increments once each CPU cycle.



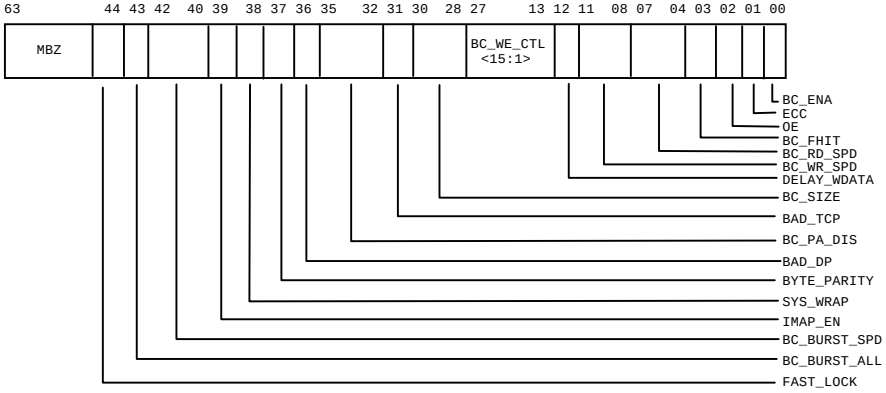
Cycle Counter Control (CC_CTL) Register

The CC_CTL register is write-only. This register controls the CC register.



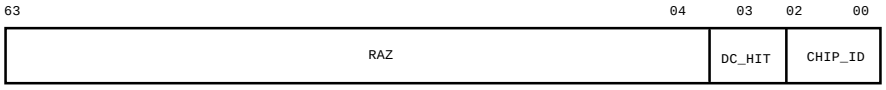
Bus Interface Unit Control (BIU_CTL) Register

The BIU_CTL register is a *write-only register*. It is included here only to show what it controls.



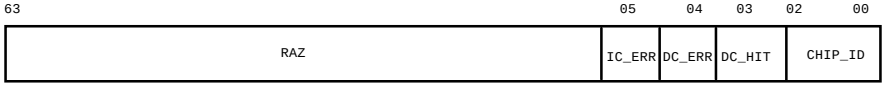
Data Cache Status (DC_STAT) Register

The DC_STAT register is a read-only register used only in the 21064 chip. When an external parity error is recognized during a primary cache fill operation, the DC_STAT register is locked until the DC_ADDR register is read.



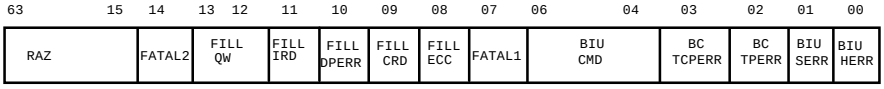
Cache Status (C_STAT) Register

The C_STAT register is a read-only register used only in the 21064A chip. It has the same address as the DC_STAT register in the 21064 chip. When an external parity error is recognized during a primary cache fill operation, the DC_STAT register is locked until the DC_ADDR register is read.



Bus Interface Unit Status (BIU_STAT) Register

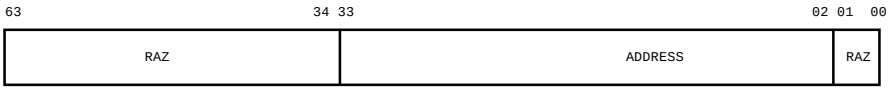
The BIU_STAT register is a read-only register. When the BIU_HERR, BIU_SERR, BC_TPERR, or BC_TCPERR bit is set, the BIU_STAT<6:0> register bits are locked until the BIU_ADDR register is read.



Bus Interface Unit Address (BIU_ADDR) Register

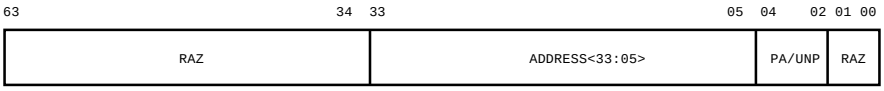
The BIU_ADDR register is a read-only register. It contains the physical address associated with errors reported by BIU_STAT<7:0>. The BIU_ADDR register's contents are valid when BIU_HERR, BIU_SERR, BC_TPERR, or BC_TCPERR bit are set. A read of the BIU_ADDR register unlocks both BIU_ADDR and BIU_STAT<7:0>.

If the BIU_CMD field of the BIU_STAT register indicates that the error-receiving transaction was READ_BLOCK or load_locked, then BIU_ADDR<4:2> are unpredictable. If the BIU_CMD contains any other command, then BIU_ADDR<4:2> contains zeros.



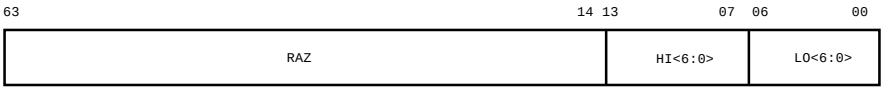
Fill Address (FILL_ADDR) Register

The FILL_ADDR register is a read-only register that contains the physical address associated with errors reported by BIU_STAT<14:08>. Its contents are meaningful only when FILL_ECC or FILL_DPERR is set. Reading the FILL_ADDR register unlocks FILL_ADDR, BIU_STATS<14:08>, and FILL_SYNDROME.



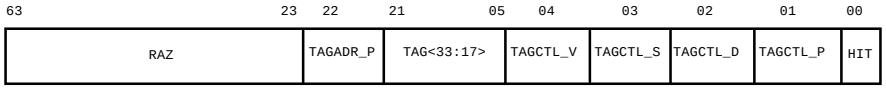
Fill Syndrome (FILL_SYNDROME) Register

The FILL_SYNDROME is a 14-bit read-only register. If the DECchip 2106 is in ECC mode and an ECC error is recognized during a primary cache fill operation, the syndrome bits associated with the bad quadword are locked in this register. The FILL_SYNDROME register is unlocked when the FILL_ADDR register is read.



Backup Cache Tag (BC_TAG) Register

The BC_TAG register is a read-only register. Unless it is locked, the BC_TAG register is loaded with the results of every backup cache tag probe. When a tag or tag control parity error or primary fill data error (parity or ECC) occurs, this register is locked against further updates. The software reads the LSB by using the HW_MFPR instruction. Every read shifts the contents one position to the right, which requires a series of reads. Unlock the register by using a HW_MTPR to the BC_TAG.



Cache and Memory Control CSRs

The core logic provides a secondary cache and memory controller, PCI interface, and a data path interface. Several control and status registers (CSRs) are located in the core logic. The CSRs reside in two areas of the core logic: the cache and memory control and the PCI bridge.

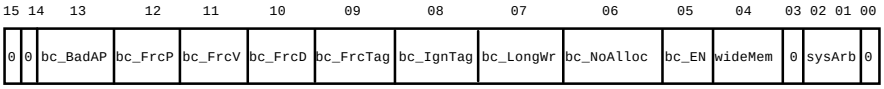
☞ Refer to *DECchip 21071/21072 Core Chip Sets Data Sheet,* order number EC-N0648-72, Digital Equipment Corporation.

The Digital AlphaStation 200 and 400 Series systems use neither the video capabilities nor memory banks three through seven. Bank eight is used to access the flashbus.

The cache memory control CSRs are 16-bits wide and addressed on cache-line boundaries only. Writes to read-only registers could result in unpredictable behavior. Only zeroes should be written to unspecified bites within a CSR. Only bits <15:0> of each CSR are defined.

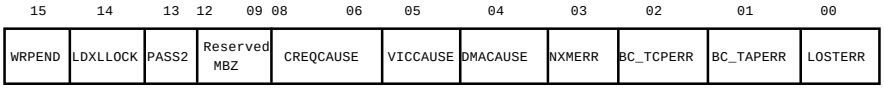
General Control Register

The general control register (1 8000.0000) contains status information that affects the major operational modes of the cache and memory control chip.



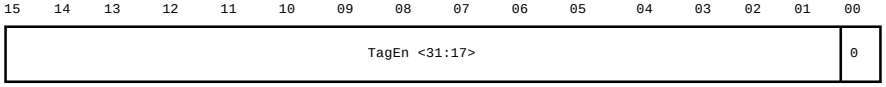
Error and Diagnostic Status Register

The error and diagnostic status register (1 8000.0040) is a read-only register located in the core logic. When an error occurs, an error bit is set and the address is locked in the Error Low and Error High Address Registers. Any additional errors occurring after the address is locked cause lostErr to be set.



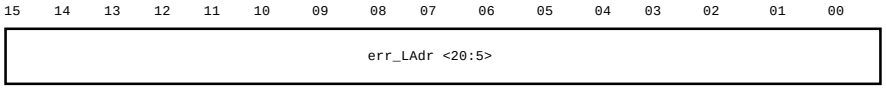
Tag Enable Register

The tag enable register is a read/write register (1 8000.0060) that indicates which bits of the cache tag are to be compared with sysAdr<33:5>. If a bit is 1, the corresponding bits in sysAdr<33:5> and tagAdr<31:17> are compared. If a bit is 0, there is no comparison of those bits and the tagAdr bit is assumed to be tied low on the module. Bits <15:1> in the register represent tagAdr<31:17>.



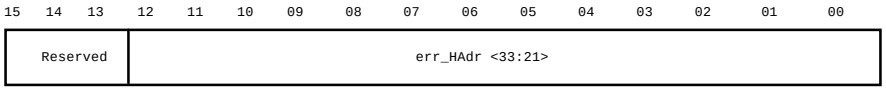
Error Low Address Register

The error low address register (1 8000.0080) locks the low order bits of the sysBus address that caused the error that set the bc_TAPErr, bc_TCPErr. or nxMErr bit in the EDSR. If a victim read caused the error, then the victim address is not latched; rather the address of the transaction is latched. Bits <15:0> represent sysAdr<20:5>. This register is read-only and only valid when an error is indicated.



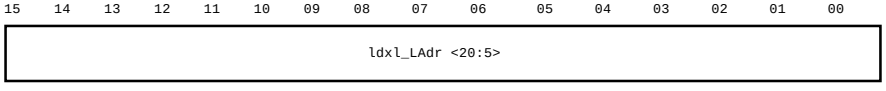
Error High Address Register

The error high address register (1 8000.00A0) locks the high order bits of the sysBus address that caused the error that set the bc_TAPErr, bc_TCPErr. or nxMErr bit in the EDSR. If a victim read caused the error, then the victim address is not latched; rather the address of the transaction is latched. Bits <12:0> represent sysAdr<33:21>. This register is read-only and only valid when an error is indicated.



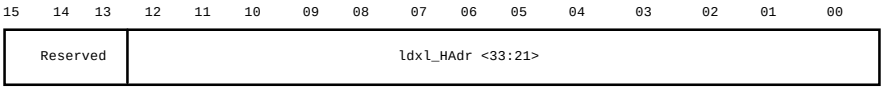
LDxL Low Address Register

The LDx_L low address register (1 8000.00C0) stores the low order bits of the last locked address. Bits <15:0> represent sysAdr<20:5>. This register is read-only.



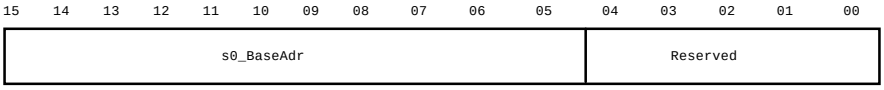
LDxL High Address Register

The LDx_L low address register (1 8000.00E0) stores the low order bits of the last locked address. Bits <12:0> represent sysAdr<33:21>. This register is read-only.



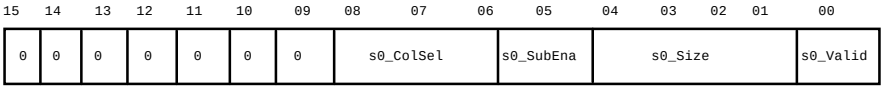
Bankset 0-8 Base Address Registers

Each memory bankset has a corresponding base register (Bank 0 Address: 1 8000 0800, Bank 1 Address: 1 8000 0820, Bank 2 Address: 1 8000 0840). The bits in this register are compared with the incoming sysAdr to determine the bankset being addressed. The contents of this register are validated by setting the valid bit in the configuration register of that bankset. The AlphaStation 200 Series and 400 Series systems use bank registers 0, 1, and 2 for main memory.



Bankset 0-7 Configuration Registers

Each memory bankset has a corresponding configuration register (Bank 0 Address: 1 8000 0A00, Bank 1 Address: 1 8000 0A20, Bank 2 Address: 1 8000 0A40). This register contains mode bits and bits for memory address generation, as well as bankset decoding. The AlphaStation 200 Series uses configuration registers 0, 1, and 2 for main memory.

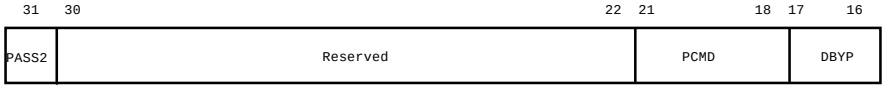


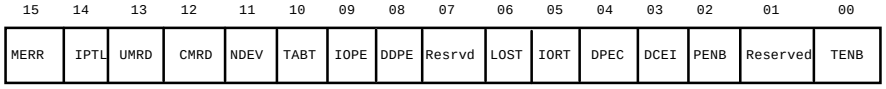
PCI Bus Bridge CSRs

The PCI bridge CSRs are 32-bits wide (longword) and addressed on cache-line boundaries (address <4:2> must be 0). Writes to read-only registers do not cause errors and are acknowledged as normal. Only zeroes should be written to unspecified bites within a CSR. Addresses in this CSR space not specified here should not be read or written.

Diagnostic Control and Status Register

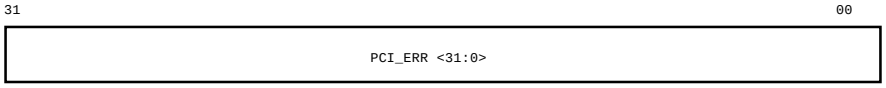
The diagnostic control and status register (CSR) (1 A000.0220) provides control of operational and diagnostic modes. It also reports status and error conditions relating to the PCI-interface section of the core logic.





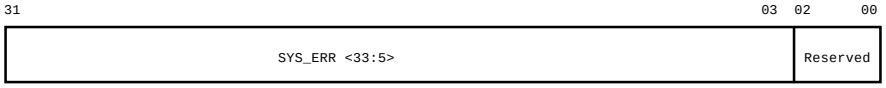
PCI Error Address Register

The PCI error address register (1 A000.0240) logs the address of various errors relating to PCI bus transactions.



Sysbus Error Address Register

The sysBus error address register (1 A000.0260)logs the address of various errors relating to sysBus transactions.

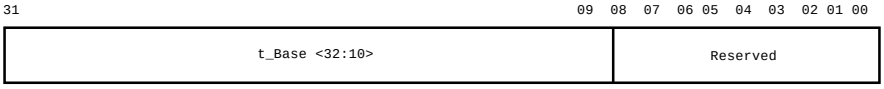


Translated Base Registers

The t_Base field of the translated base registers (1 and 2, 1 A000 00C0 and 1 A000 00E0) specify the base CPU address for either the:

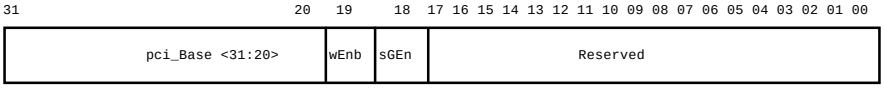
- Translated PCI address for the PCI target window (if scatter/gather is disabled).
- Scatter/gather map table for the PCI target window (if scatter/gather is enabled).

This register is read/write.



PCI Base Registers

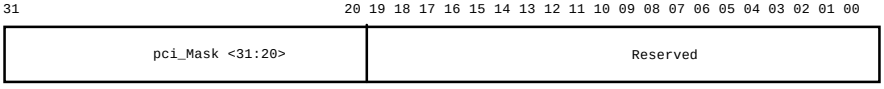
The two PCI base registers (1 A000 0100 and 1 A000 0120) are used in the mapping of PCI addresses to physical memory addresses (one base register for each of the two allowed regions).



PCI Mask Registers

The PCI mask registers (1 A000 0140 and 1 A000 0160) are used with the PCI base registers to allow two regions in PCI memory space to be mapped to system memory. The pciMask <31:20> field specifies the size of the PCI target window. It is also used in the translation of the PCI address to the CPU address.

This register is read/write.



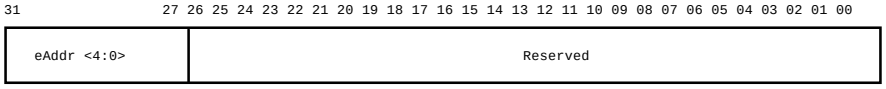
Host Address Extension Register 0

The HAXR0 register (1 A000 0180) is hardcoded to 0. A read from this register returns a 0; a write does nothing.

Host Address Extension Register 1

The host address extension register 1 (HARX1) (1 A000 01A0) is used to generate AD<31:27> on CPU-initiated transactions that address PCI memory space.

The eAddr<4:0> field is used as the upper five PCI address bits (AD<31:27>). The field is read/write.

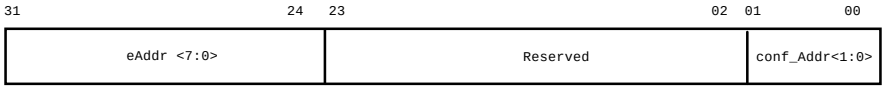


Host Address Extension Register 2

The host address extension register 2 (HARX2) (1 A000 01C0) is used to generate AD<31:24> on CPU-initiated transactions that address PCI I/O space. It is also used to generate AD<1:0> during PCI configuration reads and writes.

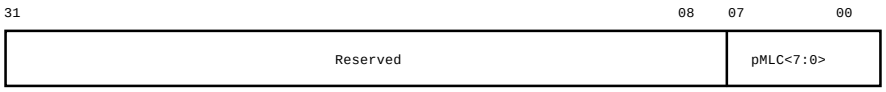
The eAddr<7:0> field is used as the upper five PCI address bits (AD<31:27>). The field is read/write.

The conf_Addr<1:0> field is used as the lower PCI address bits (AD<1:0>) during CPU-initiated transactions to PCI configuration space.



Master Latency Timer Register

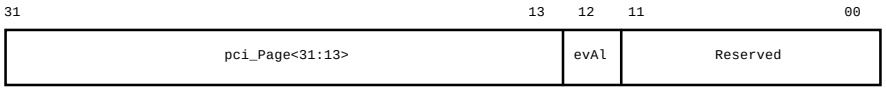
The pMLC<7:0> field of the PCI master latency register (PMLT) (1 A000 01E0) is loaded into the master latency timer register at the start of a PCI master transaction initiated by the PCI bus bridge chip.



TLB Tag Registers 0-7

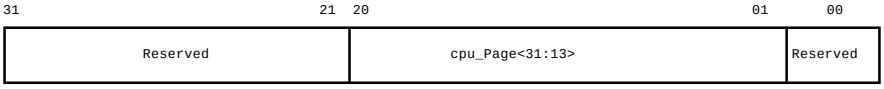
These registers (0. = 1 A000 0200, 1.= 1 A000 0220, 2. = 1 A000 0240, 3. = 1 A000 0260, 4. = 1 A000 0280, 5. = 1 A000 02A0, 6. = 1 A000 02C0, 7. = 1 A000 02E0) are read only. The pci_Page<31:13> field specifies the PCI page address (TAG) corresponding to the translated CPU page address in the associated TLB data register.

The entry valid (eVal) bit can be read through bit <12>. Normally, the invalid bit contains the value read during a page table entry read.



TLB Data Registers 0-7

These registers (0 = 1 A000 0300, 1 = 1 A000 0320, 2 = 1 A000 0340, 3 = 1 A000 0360, 4 = 1 A000 0380, 5 = 1 A000 03A0, 6 = 1 A000 03C0, 7 = 1 A000 03E0) are read only. The cpu_Page<32:13> field allows bits <32:13> of the CPU address to be read.



I/O Registers

PCI Bus Device Registers

Ethernet Controller Registers

☞ Refer to *DECchip 21040 Ethernet Controller Data Sheet* , order number EC-N0752-72, Digital Equipment Corporation

CSR0 - Bus Mode Register - offset 00h

CSR1 - Transmit Poll Demand - offset 08h

CSR2 - Receive Poll Demand - offset 10h

CSR3 - Rx List Base Address - offset 18h

CSR4 - Tx List Base Address - offset 20h

CSR5 - Status Register - offset 28h

CSR6 - Operation Mode Register - offset 30h

CSR7 - Interrupt Mask Register - offset 38h

CSR8 - Missed Frame Counter - offset 40h

CSR9 - ENET ROM Register - offset 48h

CSR11 - Full Duplex Register - offset 58h

CSR12 - SIA Status Register - offset 60h

CSR13 - SIA Conductivity Register - offset 68h

CSR14 - SIA Tx Rx Register - offset 70h

SCSI Controller Registers

Table 11-1 shows the SCSI chip registers for the Digital AlphaStation 200 and 400 Series systems.

☞ Refer to *NCR 53C810 PCI-SCSI I/O Processor Data Manual*, NCR.

Table 11-1. SCSI Chip Register Map

				Mem I/O	Config I/O
SCNTL3	SCNTL2	SCNTL1	SCNTL0	00h	80h
GPREG	SDID	SXFER	SCID	04h	84h
SBCL	SSID	SOCL	SFBR	08h	88h
SSTAT2	SSTAT1	SSTAT0	DSTAT	0ch	8ch
DSA				10h	90h
RESRV'D			ISTAT	14h	94h
CTEST3	CTEST2	CTEST1	CTEST0	18h	98h
TEMP				1ch	9ch
CTEST6	CTEST5	CTEST4	DFIFO	20h	a0h
DCMD	DBC			24h	a4h
DNAD				28h	a8h
DSP				2ch	ach
DSPS				30h	b0h
SCRATCH A				34h	b4h
DCNTL	DWT	DIEN	DMODE	38h	b8h
ADDER				3ch	bch
SIST1	SIST0	SIEN1	SIEN0	40h	c0h
GPCNTL	MA CNTL	RESRV'D	SLPAR	44h	c4h
RESRV'D	RESPID	STIME1	STIME0	48h	c8h
STEST3	STEST2	STEST1	STEST0	4ch	cch
RESRV'D			SIDL	50h	d0h
RESRV'D			SODL	54h	d4h
RESRV'D			SBDL	58h	d8h
SCRATCH B				5ch	dch

ISA Bus Device Registers

Table 11-2 shows the ISA device addresses for the Digital AlphaStation Series systems.

Table 11-2. ISA Device Addresses

Device/Register	ISA I/O Addresses	PCI Addresses	CPU Sparse Addresses
Keyboard/Mouse	060 –	0000.0060	1 C000.0C00
	064	0000.0064	1 C000.0C80
TOY Clock	070 –	0000.0070	1 C000.0E00
	071	0000.0071	1 C000.0E20
Serial Port 1	3F8 –	0000.03F8	1 C000.7F00
	3FF	0000.03FF	1 C000.7FE0
Serial Port 2	2F8 –	0000.02F8	1 C000.5F00
	2FF	0000.02FF	1 C000.5FE0
Parallel Port	378 –	0000.0378	1 C000.6F00
	37F	0000.037F	1 C000.6FE0
FDC	3F0 –	0000.03F0	1 C000.7E00
	3F7	0000.03F7	1 C000.7EE0

Keyboard and Mouse Registers

☞ Refer to *8242 Keyboard Controller Specification*, Intel, PHOENIX Technologies, Ltd.

TOY Clock Registers

☞ Refer to *BQ4285 Time of Year/NVR Chip*, Benchmarq.

Serial Port Registers

☞ Refer to *PC87332 Super I/O III Chip*, National Semiconductor.

Parallel Port Registers

☞ Refer to *PC87332 Super I/O III Chip*, National Semiconductor.

Floppy Disk Controller Registers

☞ Refer to *PC87332 Super I/O III Chip*, National Semiconductor.

Sound Card Registers

The ID and status register is read only.

Audio ID and Status Register

The registers allow access to the digital interface logic, the Analog Devices AD1848 CODEC, and the Yamaha YMF562 synthesizer. (See Table 11-3.) Notice that the synthesizer address is fixed and is unaffected by the I/O base address setting.

Table 11-3. Audio Register Offsets

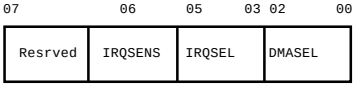
Address	Register
I/O Base + 0	Command Register (W/O)
I/O Base + 1	Reserved
I/O Base + 2	Reserved
I/O Base + 3	ID and Status Register (R/O)
I/O Base + 4	AD1848
I/O Base + 5	AD1848
I/O Base + 6	AD1848
I/O Base + 7	AD1848
388h	YM562 synth
389h	YM562 synth
38Ah	YM562 synth
38Bh	YM562 synth

Notice that the Microsoft Sound System documents the ID and status register as follows, but the Digital AlphaStation 200 Series system sound card implements all DMA and interrupt channels. The ChannelAvail bit is zero when all DMA channels (0, 1, 3) and interrupt channels (7, 9, 10, 11) are available. When only DMA channels 1 or 3 and interrupts 7 or 9 are free for use, the ChannelAvail bit returns a one.

The IrqSense bit is a 1 when there is a pending interrupt. The version identifies the revision of the sound card hardware. The current value is 04h.

The command register is write only.

Audio Command Register



When IRQSENS is written to a "1," the status register returns the state of the selected interrupt channel in bit <6>. See Table 11-4.

Table 11-4. Audio IRQ Selection

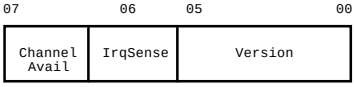
IRQSEL	Interrupt
000	Disabled
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	Reserved
110	Reserved
111	Reserved

Table 11-5 shows the channel selections for the Digital AlphaStation 200 Series system's audio DMA.

Table 11-5. AlphaStation 200 Series system Audio DMA Channel Selection

DMASEL	Play Channel	Capture Channel
000	Disabled	Disabled
001	DMA 0	Disabled
010	DMA 1	Disabled
011	DMA 3	Disabled
100	Disabled	DMA 0
101	DMA 0	DMA 0
110	DMA 1	DMA 1
111	DMA 3	DMA 1

Audio ID and Status Register



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