Date: October 10, 1994

DECchip 21041 features

1.0 Overview

This memo lists the 21041 features. It describes in detail each feature in terms of pinout, system configuration and software interface. The 21041 incorporates the following features:

- BOOT ROM support
- MicroWire serial EEPROM (93C46 or such) support
- Widen the transmit automatic polling
- Early interrupt on the first receive buffer of the packet
- A new output pin to select between AUI and 10Base-2 ports
- AUI/10Base-T port autosensing
- 3.3v/5v universal PCI pads
- Full-Duplex autodetect - Nway scheme
- Power management (sleep mode)
- LED support: rx, tx, col, rx_match, tx_jabber, link, polarity
- General purpose timer
- New capture effect algorithm
- Full Dulpex Smart arbitration scheme
- Support big endian byte ordering mode also for descriptors
- Implements the PCI spec pinout recommendation to allow board layout within trace length restriction.

The 21041 is based on the existing DECchip 21040. It has the same architecture with enhanced features and it is software compatible with the 21040. For reduced features implementations, it can be operated in 21040 mode which results in exactly the same behavior like the 21040.

Mode selection is done by Mode_Select (pin #91). This pin will be tied to VSS in order to select 21040 mode. It will be not connected, in order to select 21041 mode (internally pulled up). Upon HW or SW reset, the 21041 senses this input and selects either mode accordingly. If 21041 mode is selected the Mode_Select pin changes its functionality, turning into Boot_ROM ChipSelect output pin.

1.1 Pinout

This section provides information about the 21041 pinout. It lists all the pins and has a cross reference to the 21040. Some pin names were changed to reflect the different function (sometimes several multiplexed functions) that they are being used for, in the 21041.

1 TMS	31 VSS	61 VDD	91 MODE_SELECT/BR_CE_L
2 TDI	32 AD<21>	62 VDD	92 AUI_BNC
3 VSS	33 AD<20>	63 AD<9>	93 BR_AD<7>/SR_DIN
4 TDO	34 AD<19>	64 AD<8>	94 TP_TD--
5 INT_L	35 VDD	65 VSS	95 TP_TD+
6 RST_L	36 AD<18>	66 C_BE_L<0>	96 TP_TD-
7 VDD	37 AD<17>	67 AD<7>	97 TP_TD++
8 VSS	38 AD<16>	68 AD<6>	98 VSS
9 CLK	39 VSS	69 VSS	99 VDD
10 VDD_CLAMP	40 C_BE_L<2>	70 VDD	100 AUI_TD+
11 GNT_L	41 FRAME_L	71 AD<5>	101 AUI_TD-
12 REQ_L	42 IRDY_L	72 AD<4>	102 VSS
13 AD<31>	43 TRDY_L	73 VDD	103 VDD
14 AD<30>	44 VDD	74 AD<3>	104 TP_RD+
15 VSS	45 DEVSEL_L	75 AD<2>	105 TP_RD-
16 AD<29>	46 STOP_L	76 VSS	106 AUI_CD+
17 AD<28>	47 PERR_L	77 AD<1>	107 AUI_CD-
18 VDD	48 VSS	78 AD<0>	108 VDD
19 AD<27>	49 SERR_L	79 BR_A<0>/SR_DOUT	109 AUI_RD+
20 AD<26>	50 PAR	80 BR_A<1>/SR_SK	110 AUI_RD-
21 VSS	51 C_BE_L<1>	81 SR_CS	111 VDD
22 AD<25>	52 VSS	82 VDD	112 VSS
23 AD<24>	53 AD<15>	83 XTAL2	113 BR_AD<6>
24 VSS	54 AD<14>	84 XTAL1	114 BR_AD<5>
25 C_BE_L<3>	55 AD<13>	85 VDD	115 BR_AD<4>
26 IDSEL	56 VDD	86 IREF	116 BR_AD<3>
27 AD<23>	57 AD<12>	87 VDDAC	117 BR_AD<2>
28 AD<22>	58 AD<11>	88 VCAP_H	118 BR_AD<1>
29 VSS	59 AD<10>	89 VDDAC	119 BR_AD<0>
30 VDD	60 VSS	90 VSS	120 TCK

The following table lists all the pin names that have been changed and describes the new functionality.

21040	21041	Description
VSS	BR_AD<7>/SR_DIN	BOOT ROM Address/Data<7> or Serial ROM DIN
EXT_CLSN	BR_AD<6>	BOOT ROM Address/Data<6> or Transmit LED
EXT_RX	BR_AD<5>	BOOT ROM Address/Data<5> or Collision LED
EXT_RXEN	BR_AD<4>	BOOT ROM Address/Data<4> or Receive matching address LED
EXT_RCLK	BR<AD<3>	BOOT ROM Address/Data<3> or Receive LED
EXT_TX	BR_AD<2>	BOOT ROM Address/Data<2> or TP Polarity/General purpose 2 LED
EXT_TCLK	BR_AD<1>	BOOT ROM Address/Data<1> or Transmit Jabber LED / General Purpose 1 LED
EXT_TXEN	BR_AD<0>	BOOT ROM Address/Data<0> or LinkPass
SCLK	BR_A<1>/SR_SK	BOOT ROM Address<1> or Serial ROM clock
SDIN	BR_A<0>/SR_DOUT	BOOR ROM Address <0> or Serial ROM Dout
SRST	SR_CS	Serial ROM Chip Select
VSS	ModeSelect/BR_CE_L	Mode Select or BOOT ROM Chip Enable
AUI_TP	AUI_BNC	AUI or BNC output select line

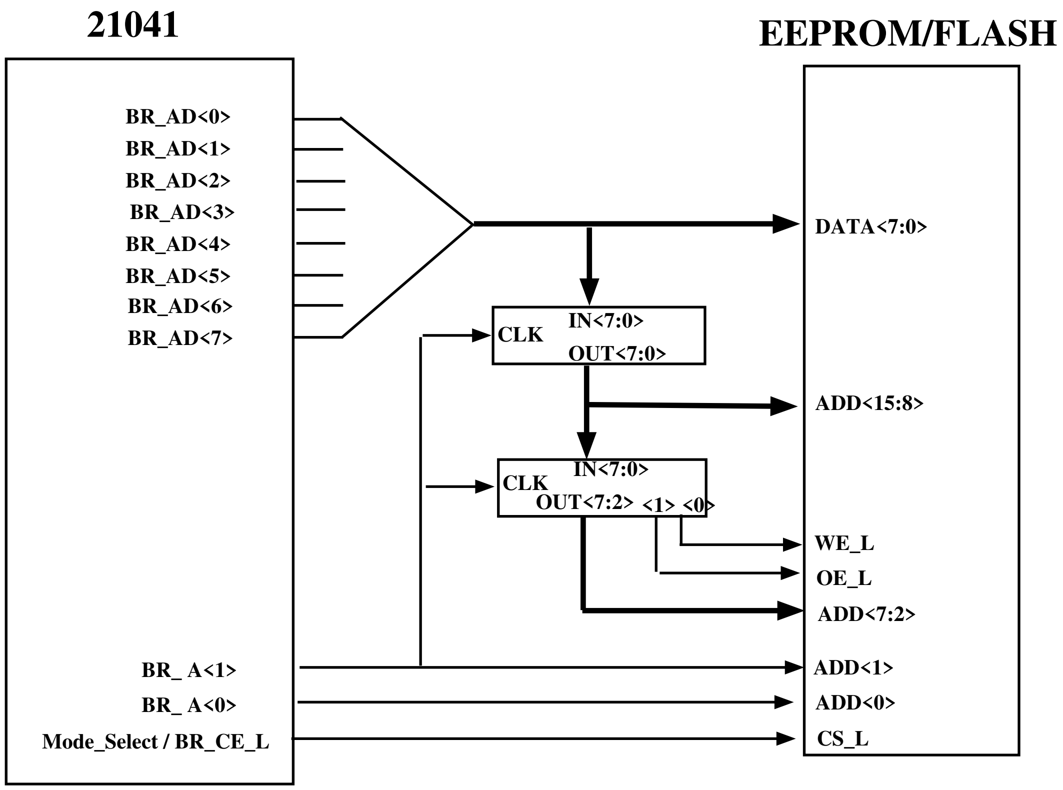
2.0 Boot ROM support

21041 will incorporate support for Boot ROM. The Boot ROM contains a code that can be executed for device-specific initialization and, possibly a system boot function. During machine boot, the BIOS looks for BOOTable devices by searching a specific signature (55AA) Once found, the BIOS copies the code from the BOOT ROM to a shadow RAM in the host memory and executes it from the RAM. The new Boot ROM interface supports:

- 5V or 12V FLASH memory - for code upgrade
- 120nS EEPROM or faster
- Up to 256KByte address space

2.0 System configuration

The following diagram shows the connection of a 64Kbyte Boot ROM.



As seen in the diagram, two 8-bit edge trigger latches are used to latch the Boot ROM address lines. 21041's first byte access cycle to Boot ROM (either read or write) in composed of three cycles:

- cycle #1 - Address<7:2> . WR_L and OE_L are driven in BR_AD<7:0> and latched in the upper latch.
- cycle #2 - Address<15:8> are driven in BR_AD<7:0> and latched by the upper D_FF. At the same time, Address<7:2>. WR_L and OE_L are propagated to the lower latch.
- cycle #3 - Add<1:0> are driven. BR_CE_L is asserted. BR_AD<7:0> will carry the data to be read/written from/to the Boot ROM.

The additional three consecutive bytes are read/written by driving the BR_ADD<1:0> lines. BR_A<1:> is used also to latch the addresses in the two latches. Therefore, it is driven in a way that there is no transition from low to high.

In order to interface to a 256KByte BOOT ROM, the following steps should be taken:

- Replace the 8 bit latch with 9 bit latch.
- Address bit <16> is taken off the first latch output Q8, using pin BR_A<0>/SR_DOUT (#79) as input to D8
- Address bit <17> is taken off the second latch output Q8, using Q8 of the first latch as input to D8.

2.2 Software interface

The BOOT ROM can be accessed in two ways:

- DWORD (32 bit) access from the PCI expansion ROM address space (21041 transfers all 4 bytes regardless the byte mask).
- Byte access (Read/write) via CSR9 and CSR10

The PCI Expansion ROM base address is part of the 21041 configuration registers (in Add 30H). Bits <31:18> contains the expansion ROM base address. Bits <17:1> are tied to '0' indicating the HOST that the 21041 allocates 256K byte for BOOT ROM (regardless the actual size of the BOOT ROM). Bit <0> is used by the HOST to enable/disable the access to the Boot ROM. Expansion ROM base address format is:

31 — 24 —	16								8								0
Expansion ROM base address	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**EN**

In order to access the BOOT ROM, the following actions must be taken:

- BIOS writes all '1' to Expansion ROM base address register
- BIOS reads Expansion ROM base address register to determine the BOOT ROM size
- BIOS writes the Expansion ROM base address and set bit EN in the Expansion ROM base address register

From this point, 21041 monitors the PCI address lines and compares AD<31:18> bit to the address written in the PCI Expansion ROM base address. Bits AD<17:2> carry out the BOOT ROM address.

The access to the Boot ROM is done also via the CSR9 and CSR10 registers. CSR10 is used to store the address (byte offset). CSR9 holds the command (read/write) and the data to be read/write. CSR9/CSR10 format is:

	31							24							16 … 8 … 0
CSR10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	**Boot ROM offset**

	31							24								16							8	0
CSR9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	MOD	RD	WR	BR	SR	REG	1	1	**DATA**

- **MOD** - Mode Select - This bit is tied to ModeSelect pin (inverted). It indicatse the operating mode (21040 or 21041)
- **RD -** Read from the Boot ROM
- **WR** - Write to the Boot ROM
- **BR** - Select BOOT ROM
- **SR** - Select Serial ROM
- **REG** - Select external register (to be described in an application note)
- **DATA** - BOOT ROM data - This field is valid only if Boot ROM is selected

Comments:

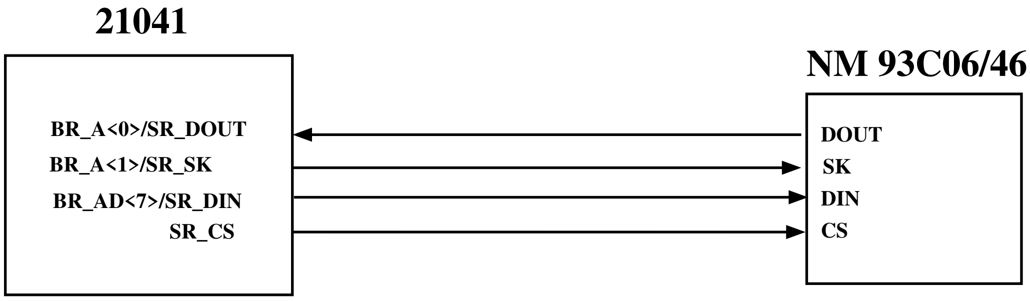
- For Boot ROM read operations CSR9<14> and CSR9<12> must be set
- For Boot ROM write operations, CSR9<13> and CSR9<12> must be set

3.0 MicroWire Serial EPROM support

21041 incorporates support of MicroWire serial EEPROM (93C46 or such). The serial EEPROM contains the IEEE address. The EEPROM pins are fully software driven. All pins (SK, Din, Dout, CS) are connected directly to CSR9 bits. Therefore, all EPROM timing (sequences, setup time, hold time and delays) must be handled by the driver. The sequences for EPROM accesses will be provided separately in an application note.

3.1 System configuration

The following diagram shows the connection to the serial EPROM



3.2 Software interface

The EPROM access is done via CSR9. CSR9 format is:

	31							24								16								8								0
CSR9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	MOD	RD	WR	BR	SR	REG							DO	DI	SK	CS

- **MOD** - Mode Select - This bit is tied to ModeSelect pin (inverted). It indicates the operating mode (21040 or 21041)
- **RD -** Read from the Boot ROM
- **WR** - Write to the Boot ROM
- **BR** - Select BOOT ROM
- **SR** - Select Serial ROM
- **REG** - Select external register
- **DO** - data out - Contains the data to be read from the EPROM

- **DI** - data in - Contains the address and the data to be written to the EPROM
- **SK** - Serial ROM clock
- **CS** - Serial ROM Chip Select

For serial ROM operations CSR9<11> must be set with CSR9<13> or with CSR9<14> before start the accesses (read/write) to the serial ROM.

4.0 Widen the Transmit automatic polling

The number of options for Transmit Automatic Polling values was increased. In 21040, 4 values were allowed:

- No transmit automatic polling
- Transmit automatic polling every 200 microseconds
- Transmit automatic polling every 800 microseconds
- Transmit automatic polling every 1.6 milliseconds

Four values were added: 12.8, 25.6, 51.2 and 102.4 microseconds. The new CSR0 format is:

31							24						16		8				0
1	1	1	1	1	1	1	1	1	1	1	DBO	ATP	DAS	CAL	BURST LEN	BLE	DSL	RR	SWR

ATP - Automatic Poll demand:
000 - Disabled
001 - Poll Demand every 200 microseconds
010 - Poll Demand every 800 microseconds
011 - Poll Demand every 1.6 milliseconds
100 - Poll Demand every 12.8 microseconds
101 - Poll Demand every 25.6 microseconds
110 - Poll Demand every 51.2 microseconds
111 - Poll Demand every 102.4 microseconds

The new transmit automatic polling values are being supported in both 21040 and 21041 modes.

5.0 Early interrupt

21041 generates an interrupt (called ER) upon completion processing the first receive buffer. The ER bit will be asserted:

- In case of one buffer per descriptor, upon completion writing the buffer.
- In case of two buffers per descriptor, upon completion writing the first buffer.

ER and RI bits will never be asserted together. RI clears automatically the ER bit in CSR5. The following bits were added:

CSR5<14> - ER: Early receive interrupt bit.
CSR7<14> - ERM - Early receive interrupt mask bit

The Early interrupt bit is being supported in both 21040 and 21041 modes.

6.0 AUI, 10Base-2 ports selection

A new output pin which selects between AUI and 10Base-2 ports was added. The new pin (#92 - AIU_BNC) is used mainly to enable/disable the external BNC Transceiver. The new pin is SW driven and is connected directly to CSR15<3>.

AUI_BNC pin replaces AUI_TP input pin in the 21040. Also CSR12<PAUI> - Pin AUI_TP Indication is reserved in 21041 mode.

7.0 10Base-T, AUI and 10Base-2 autosensing

21041 (in conjunction with the SW driver) provides full autosensing between 10Base-T, AUI and 10Base-2 ports. This is done by sensing the TP port and the receive activity of the ports always regardless the port selection. This section describes the HW implementation. A complete autosensing algorithm will be provided later.

Two interrupts are generated:

- LNF - Transition from Link Pass to Link Fail in TP mode (this interrupt exists in the current silicon)
- LP - Transition from Link Fail to Link Pass,(in both modes).

The following bits were added:

CSR5<4> - LP: Link Pass interrupt bit.
CSR7<4> - LPM: Link Pass interrupt mask bit

In addition, two bits which indicate the network activity on the ports were added. These bits are used to allow the SW driver to auto-sense between the AUI and 10Base-2 ports. the bits are:

- CSR12<8> - S_RxA: This bit is set when there was a receive activity on the selected port the since the last SIA reset.
- CSR12<9> - NS_RxA: This bit is set when there was a receive activity on the non selected port the since the last SIA reset.

These bits is read/write-one-to-clear by the HOST.

The autosensing capability is programmed via CSR14<15> - TAS: TP/AUI Auto-sensing Enable. In Autosensing mode, the driver must set also the following bits: :

- CSR14<3> - LSE: Link Pulse Send Enable
- CSR14<5:4> - CPEN: Compensation Enable
- CSR14<12> - LTE: Link Test Enable
- CSR14<13> - APE: Auto Polarity Enable
- CSR14<14> - SPP: Set Polarity Plus

8.0 3.3V/5V universal PCI pad

PCI specification Rev 2.0 defines two signaling environments: 3.3V and 5V. 21041 will support both environments.

5V signaling environment:

Is based on absolute switching voltage in order to be compatible with TTL switching level. The pin voltage levels are:

Vih = 2.0V min, VCC +0.5 max (VCC max = 5.25V)
Vil = -0.5V min, 0.8V max
Voh = 2.4V min
Vol = 0.55V max

3.3V signaling environment:

Is based on VCC relative switching voltage.. The pin voltage levels are:

Vih = 0.475VCC min, VCC +0.5 max (VCC min = 3V)
Vil = -0.5V min, 0.325VCC max (VCC max = 3.6V)
Voh = 0.9VCC min
Vol = 0.1VCC max

The 3.3V/5V universal PCI pad is being supported in both 21040 and 21041 modes.

9.0 Full-Duplex autodetect - Nway scheme

The Digital's proprietary auto detect scheme is no longer supported in 21041. The FD interrupt (CSR5<FD>, CSR7<FDM> and CSR11, the FDX register were removed.

Instead, the Nway auto-detect scheme will be supported. Since, this standard is not staibilized yet, the circuitry will be added but not tested intensively (with the intention to change the logic when the standard will be closed).

The Nway scheme is an interoperability solution that addresses the need to automatically configure the network nodes. It provides autodetect capabilities such as speed sensing (10/100Mbps), the PHY type and Half/Full Duplex mode. 21041 implements the Half/Full Duplex mode autodetection. The Nway builds upon the existing 10Base-T link pulse scheme and is based on data exchange between two nodes in the Physical layer.

The Nway implementation is done without SW driver involvement. The 21041 will notify the host what is the mode which was detected (Half/Full duplex).

New bits were added to CSR12 and CSR14 for NWay software interface. The bits that were added are:

- CSR12<10> - NNR (NWay Negotiation Request)
  When set the NWay negotiation starts again.
- CSR12<11> - ARF (Advertised Remote Fault)
  When set indicates that the 21041 transmits its ability with the Remote Fault bit asserted.
- CSR12<14:12> - NAS (NWay Arbitration State)
  These bits indicates the state of the NWay arbitration finite state machine as follows:
  - 000 NWay disable
  - 001 transmit disable
  - 010 ability detect
  - 011 acknowledge detect
  - 100 complete acknowledge
  - 101 FLP link good - NWay complete
  - 110 link check
- CSR12<15> LPN (Link Partner NWay-able)
  This bit is set when the link partner is an NWay-able device.

- CSR12<31:16> LPC (Link Partner's Link Code Word)
  These bits contains the partner's link code word as defined in IEEE 802.3 Standard. This field is meaningful only when CSR12<LPN> is read as "1" and CSR12<NAS> is read as "101".
- CSR14<6> HDE (Half Duplex Enable)
  This bit is meaningful only when CSR14<7> is set. When set the 21041 advertises its ability to work in either half-duplex of full-duplex modes. When clear, the 21041 advertises its ability to work in full-duplex mode only.
- CSR14<7> NWE (NWay Enable)
  When set, the NWay auto-negotiation logic is enabled to perform negotiation with a link partner in order to determine the network environment (full-duplex or half-duplex).
  when clear, the NWay auto-negotiation is disabled and the working mode is determined via CSR6<FD> bit.

10.0 Power management

21041 incorporates a power saving mode called 'sleep' mode. The 21041 power consumption, in this mode will be reduced to several milli Watts. Entering to sleep mode is done by setting bit 31 in the CFDA configuration register.

Most of the circuitry inside the chip will be disabled. This includes the DMA, FIFOs, Rxm, TxM, SIA, Digital PLL, Receive/Transmit pins and the general purpose timer. Only the PCI block and its pads will be enabled.

During sleep mode, the SW driver is allowed to access only the PCI configuration registers. In order to enter to sleep mode, the SW driver should takes the following steps:

- Stop RX/TX processes
- Stop SIA (reset CSR13<0> bit)
- Verify that the Rx and Tx processes are in stop state
- Set CFDA<PWR> bit

The first three steps can be replaced by software reset.

In order to exit sleep mode, the following steps should be taken:

- Clear CFDA<PWR>
- Wait 10 milliSec

- Start the SIA (set CSR13<0>
- Activate the Rx and Tx processes

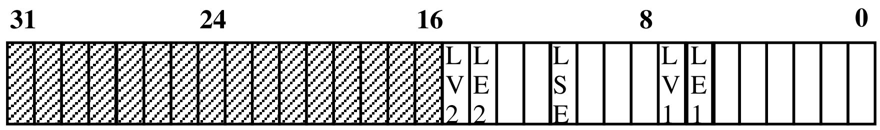
11.0 LED support

The EXT_SIA pins are used to carry out the Boot ROM address/data lines and to drive 7 LEDs. The 7 LEDs are:

- Pin #119 - LinkPass
- Pin #118 - Transmit Jabber / General purpose LED 1
- Pin #117 - TP Polarity / General purpose LED 2
- Pin #116 - Receive
- Pin #115 - Receive Matching address
- Pin #114 - Collision
- Pin #113 - Transmit

Five LEDs (Transmit Jabber, Receiving, Receive Matching Address, Collision and Transmitting) are stretched in a range of 52mSec to 78mSec.

LinkPass and Transmit Jabber LEDs can be used also as general purpose LEDs. The mode selection and their value is set in CSR15. The following figure shows the bits that were added to CSR15 for LED dupport.

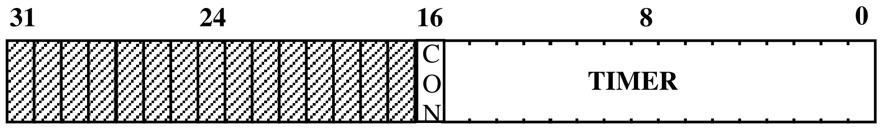


LE1 - General Purpose LED 1 Enable
LV1 - General Purpose LED 1 Value
LSD - Led Stratcher Enable - when set, the 5 LEDs are stretched
LE2 - General Purpose LED 2 Enable
LV2 - General Purpose LED 2 Value

12.0 General Purpose timer

21041 incorporates a 16-bit general purpose timer. This timer is used by the SW driver for timing functions not always supplied by the operating system .

The timer is located in CSR11 instead of the Full-Duplex detection register. The timer format is:



- **TIMER** - Value in 204.8 microSec cycles
- **CON** - When set, the timer is working in continuous operating mode. when cleared, the timer is working in One Shot operating mode

Upon timer expiration, the 21041 generates an interrupt called TM. The following bits were added

CSR5<11> - TM: Timer Expired interrupt
CSR7<11> - TMM: Timer Expired interrupt mask

Comments:

- After reset, CSR11 value is 0
- In one shot operating mode, after receiving interrupt, the timer value is cleared
- When writing a new value to CSR11, the new value is entered immediately and no interrupt will be generated as a results of the previous value.
- Writing 0 to CSR11 stops the operation of the timer. No interrupt will be generated.

13.0 New capture effect algorithm

A fix was added to the capture effect algorithm. The new algorithm behaves the same as the old algorithm except for the case when the 21041 is working in the 2,0 Backoff mode and a transmission completes successfully.

- In the old algorithm the 21041 will wait for another successful transmission before doing a Backoff of 2, on the next collision.
- In the New algorithm the 21041 will Backoff 2 slots on the next collision and not wait for another successful transmission.

In addition, a new mode called 'new capture effect' was added. In this mode, 21041 enables the stop backoff algorithm only in Backoff 2 state. A new bit

(CSR6<31> called SCE - Special Capture Effect) was added to enable/disable this mode.

14.0 Full Duplex smart arbitration scheme

In addition to the smart arbitration scheme (described in 21040 HW reference manual section 5.2.) a new condition was added.

While working in Full-Duplex mode and both, receive and transmit FIFOs exceeded the threshold (Tr), the DMA moves to Round-Robin based arbitration scheme between the two processes. The complete condition is:

If (FDX mode) and (Txreq) and (Rxreq) and (Txen) and (RxF>tr) and (TxF>tr)

Than Round-Robin between the Receive and Transmit processes.

15.0 Descriptor Byte Ordering Mode

A new bit was added to CSR0 in order to enable more flexibility in big/little byte ordering for descriptors. In the 21040 there was no way to operate in big endian mode for descriptors (CSR0<BLE> is applicable for data buffers only).
The new bit in 21041 is CSR0<20> - Descriptor Byte Ordering Mode (DBO). When this bit is set, the 21041 operates in big endian byte ordering mode for descriptors. When clear, descriptor operations will be done in little endian byte ordering mode.
Note that CSR0<BLE> and CSR0<DBO> are completely independent. Any mixture of the two is legal.