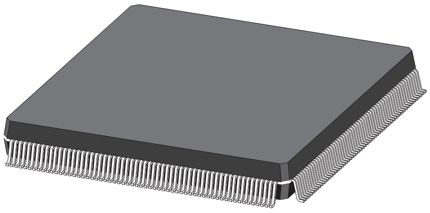
DECchip 21071 and DECchip 21072 Core Logic Chipsets

Product Brief

April 1994



Description

The DECchip 21071 and DECchip 21072 core logic chipsets provide a cost-effective solution for designing uniprocessor systems using the DECchip 21064 family of Alpha AXP microprocessors. The chipsets include a secondary cache and memory controller, PCI interface, and corresponding data path functions. The chipsets provide ample flexibility to the system designer in building the memory and I/O subsystem and require minimal discrete logic on the module. The 21071 and 21072 chipsets contain three unique gate arrays:

- 21071-CA (Cache/memory controller)—208 PQFP
- 21071-DA (PCI interface)—208 PQFP
- 21071-BA (Data path)—208 PQFP

Features

- Supports the entire family of Alpha AXP microprocessors
- DECchip 21071:
  - –128-bit cache/64-bit memory
  - –Two DECchip 21071-BA chips
  - –One DECchip 21071-CA chip
  - –One DECchip 21071-DA chip
- DECchip 21072:
  - –128-bit cache/128-bit memory
  - –Four DECchip 21071-BA chips
  - –One DECchip 21071-CA chip
  - –One DECchip 21071-DA chip
- System clock frequency up to 33 MHz
- Secondary Bcache cache/memory controller:
  - –Write-back cache
  - –Size from 128 KB to 16 MB
  - –Bcache SRAMs, 17 ns and faster
  - –32-bit parity/32-bit ECC on Bcache (DECchip 21072 only)
  - –8 MB to 6 GB of memory supported
  - –267 MB/s CPU write bandwidth, 107 MB/s CPU read bandwidth
  - –32-bit parity/32-bit ECC on memory data (DECchip 21072 only)
  - –RAS/CAS memory bus to industry-standard SIMMs
  - –DRAM controller with fully programmable timing with 15 ns granularity
- High-performance PCI bridge
  - –32-bit multiplexed address/data
  - –Industry standard
  - –No glue logic needed to connect PCI-compliant chips
  - –120 MB/s DMA write bandwidth, 70 MB/s DMA read bandwidth, 82 MB/s programmed I/O write bandwidth, 22 MB/s programmed I/O read bandwidth
  - –Scatter/gather map support
- Graphics support
  - –High bandwidth memory data path to video RAM (VRAM)
  - –Provides support for direct connection to VRAM frame buffer

System Overview

To build a system using the DECchip 21071 or DECchip 21072 chipsets, you need the following components:

- DECchip 21064 microprocessor
- PCI interrupt controller
- Bcache
- DECchip 21072 chipset
- Serial ROM interface to the CPU
- DRAM SIMMs
- PCI local bus peripherals
- PCI local bus arbiter
- Bcache PALs

DECchip 21071 – The DECchip 21071 chipset supports a 64-bit wide data path to memory. This configuration has:

- Two DECchip 21071-BA (data path) chips
- One DECchip 21071-CA (cache/memory controller) chip
- One DECchip 21071-DA (PCI bridge) chip

In this configuration, each data path slice connects to 64 bits of the DECchip 21064 data bus (sysData) and 32-bits of the memory data bus (memData). The DECchip 21071 supports 32-bit parity on the B2 cache and memory.

DECchip 21072 – The DECchip 21072 chipset supports a 128-bit wide data path. This configuration has:

- Four DECchip 21071-BA (data path) chips
- One DECchip 21071-CA (cache/memory controller) chip
- One DECchip 21071-DA (PCI bridge) chip

In this configuration each data path slice connects to 32 bits of the DECchip 21064 data bus (sysData) and 32 bits of the memory data bus (memData). The extra 32 bits on the sysData side in each data path slice are used for ECC check bits for sysData and memData (sysCheck and memCheck). Therefore the DECchip 21072 chipset supports both 32-bit parity and 32-bit ECC on the Bcache and memory.

sysBus – The DECchip 21071-CA, DECchip 21071-BA, and DECchip 21064 (CPU) chips communicate with each other over the sysBus. The sysBus essentially is the DECchip 21064 pin bus with some additional signals to handle DMA transactions between the DECchip 21071-CA and the DECchip 21071-DA chips.

epiBus – The DECchip 21071-DA chip communicates with the DECchip 21071-BA chips over the epiBus, which consists of:

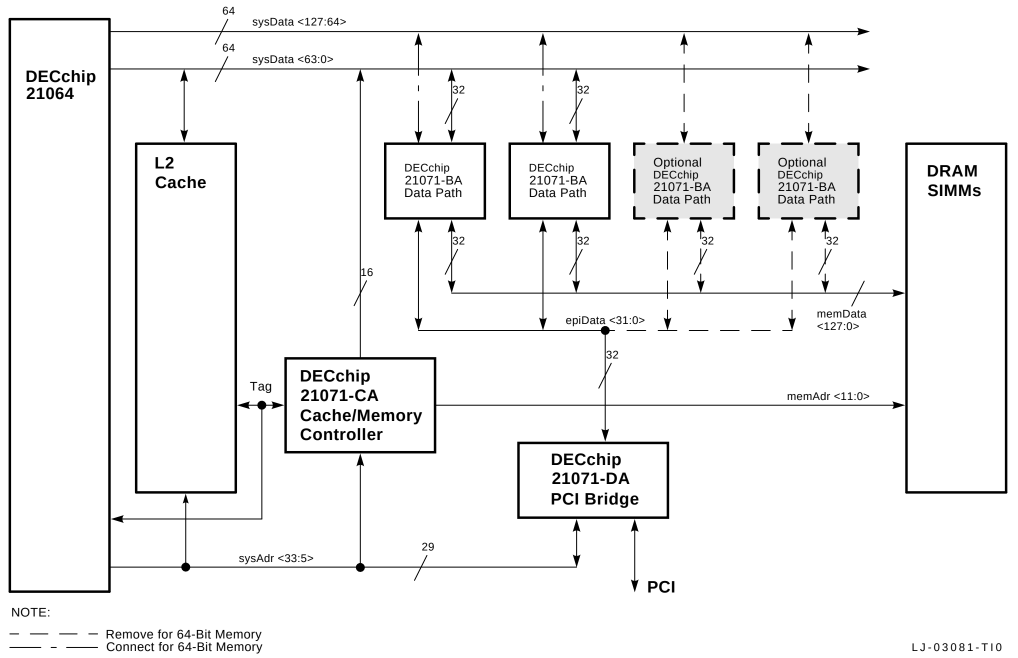
- 32 data bits (epiData)
- 4 byte enables
- Data path control signals

Memory – Systems built with the DECchip 21071 chipset can support memory in the range of 8 MB to 1 GB.

Systems built with the DECchip 21072 chipset can support memory in the range of 16 MB to 2 GB.

The DECchip 21071-CA chip supports 1M x 1, 1M x 4, 4M x 1, 4M x 4, and 16M x 1 DRAMs on the memory interface.

Figure 1 System Block Diagram



DECchip 21071-BA Microarchitecture

The DECchip 21071-BA functions as the data path for the cache/memory and I/O subsystem.

The DECchip 21071-BA contains the following data path functions.

Error Correction/Detection Logic—The DECchip 21071-BA supports longword (32 bits) parity in 64-bit and 128-bit memory mode. ECC mode is used with 128-bit wide memory by using some of the unused higher order CPU data bits as check bits. Error checking/generation is done only on DMA transactions. On CPU-initiated transactions, this function is performed by the CPU.

Memory Write Buffer—The memory write buffer has four entries; each entry is a cache line (32 bytes). This buffer is spread across the DECchip 21071-BA chips (two or four chips) in the system. Data stored in this buffer has been through all the cache coherency checks and is written to memory in the order it was received on the sysBus.

Memory Read Buffer—The memory read buffer is a one-cache-line (32 bytes) temporary holding buffer used to store data read from memory until it can be sent to the CPU or the DMA read buffer.

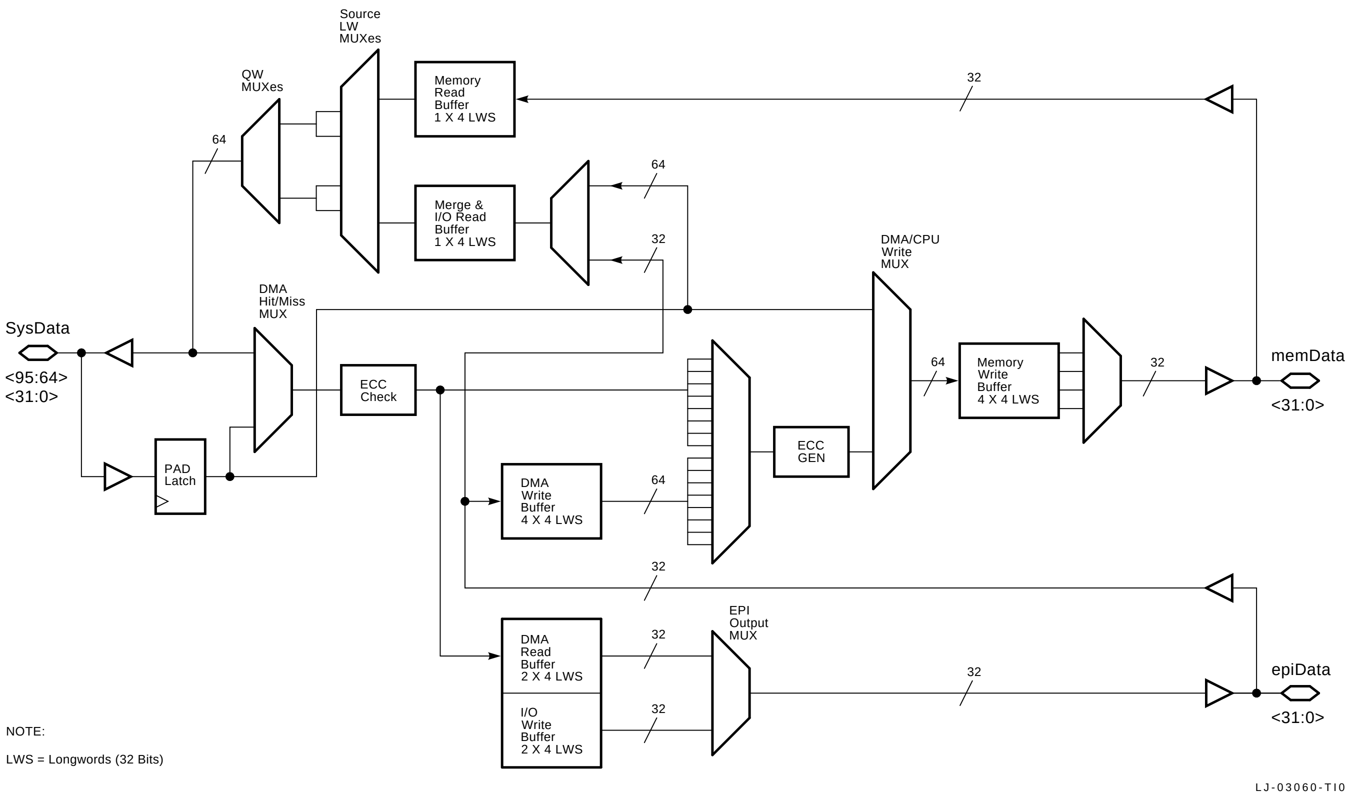
Merge Buffer—The merge buffer is a one-cache-line (32 bytes) temporary holding buffer used to store data written by the CPU on memory writes, or to store data read from the PCI bus on CPU reads.

I/O Write Buffer—The I/O write buffer has two entries, one cache line (32 bytes) each. Each entry alternately acts as a write buffer and a holding buffer for write data received from the CPU and directed towards the DECchip 21071-DA chip or PCI bus.

DMA Read Buffer—The DMA read buffer stores data that is being read from the memory by a device on the PCI bus. This buffer is two cache lines deep and is spread across the DECchip 21071-BA chips in the system.

DMA Write Buffer—The DMA write buffer stores four cache lines of PCI memory write data. Each entry is unloaded after the necessary cache coherency checks have been performed.

Figure 2 DECchip 21071-BA Block Diagram



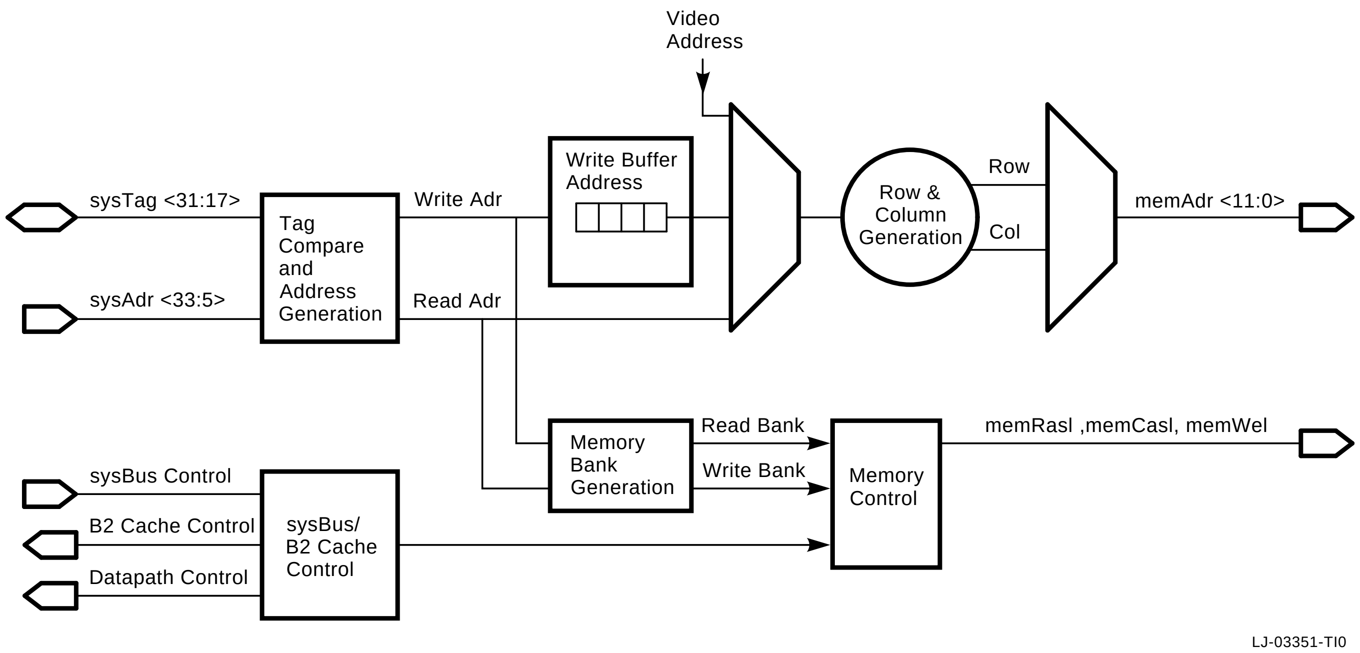
DECchip 21071-CA Microarchitecture

The DECchip 21071-CA chip performs the Bcache and memory control functions.

The DECchip 21071-CA provides the following features:

- Provides control for filling the Bcache and extracting victims on CPU-initiated transactions
- Provides control for probing the Bcache on DMA transactions and invalidating the Bcache on DMA write hits
- Provides arbitration between the CPU and the DECchip 21071-DA for control of the sysBus
- Stores addresses for the four cache-line-deep memory write buffer
- Controls the loading of the I/O write buffer and the DMA read buffer
- Uses fast page mode on the DRAMs to get improved performance on DMA burst reads and memory writes
- Supports a dumb frame buffer on the memory data bus

Figure 3 DECchip 21071-CA Block Diagram



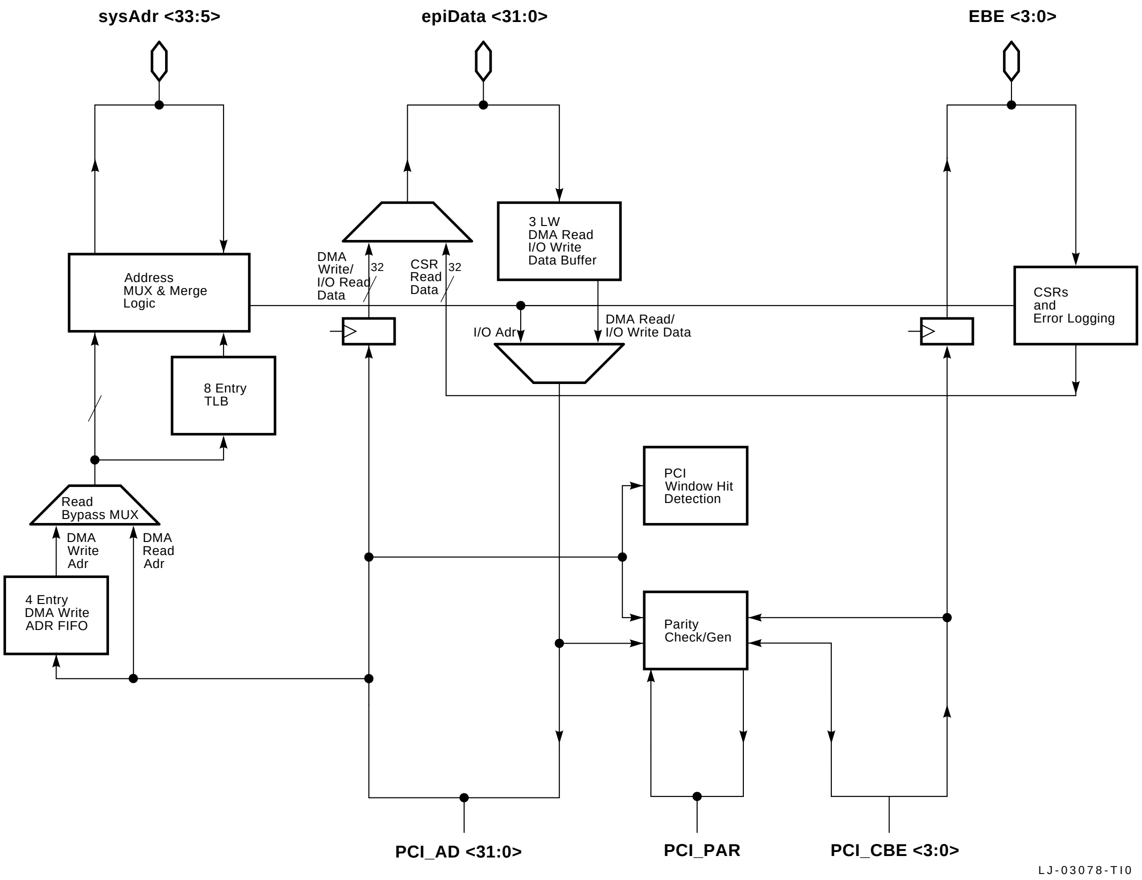
DECchip 21071-DA Microarchitecture

The DECchip 21071-DA chip functions as the bridge between the PCI and the CPU, its Bcache, and memory. The DECchip 21071-DA interface protocol is compliant with the PCI local bus. With the exception of a few pipeline registers and the parity tree, all the data path functions required to support the PCI reside in the DECchip 21071-BA chips.

The DECchip 21071-DA provides the following features:

- Scatter/gather mapping from the 32-bit PCI address to the 34-bit physical address, with an on-chip, 8-entry translation lookaside buffer (TLB) for fast address translations. To reduce cost, the scatter/gather tables are stored in memory and are automatically read by the DECchip 21071-DA (PCI bridge) when a translation misses in the TLB.
- Supports a maximum PCI burst length of 16 longwords on PCI memory reads and writes.
- Supports two types of addressing regions on CPU-initiated transactions to PCI space:
  - Sparse space for accesses with byte and word granularities, and a maximum burst length of 2.
  - Dense space for burst lengths from 1 to 8 on writes and a burst length of 2 on reads. This region can be used for memory-like structures such as frame buffers, which require high bandwidth accesses.
- Stores address information for the DMA write buffer, and controls the loading of the DMA write buffer and I/O read buffer.
- Stores address information for the I/O write buffer, and controls the unloading of the I/O write buffer and DMA read buffer.

Figure 4 DECchip 21071-DA Block Diagram



DECchip 21071–BA Characteristics

Power supply	Vss 0.0 V, Vdd 5 V ±5%
Operating temperature	Tj maximum = 100°C
Storage temperature range	−55°C to 125°C maximum
Power dissipation @ Vdd = 5.25 V Freq = 33 MHz	1.5 W maximum

DECchip 21071–CA Characteristics

Power supply	Vss 0.0 V, Vdd 5 V ±5%
Operating temperature	Tj maximum = 85°C
Storage temperature range	−55°C to 125°C maximum
Power dissipation @ Vdd = 5.25 V Freq = 33 MHz	1 W maximum

DECchip 21071–DA Characteristics

Power supply	Vss 0.0 V, Vdd 5 V ±5%
Operating temperature	Tj maximum = 85°C
Storage temperature range	−55°C to 125°C maximum
Power dissipation @ Vdd = 5.25 V Freq = 33 MHz	1.5 W maximum

For More Information

To learn more about pricing and availability of the DECchip 21071 and DECchip 21072 core logic chipsets, contact your Digital sales representative, or, in the United States, call our Semiconductor Information Line:

1-800-332-2717
1-800-332-2515 (TTY)

Outside North America, call:

+1-508-568-6868

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