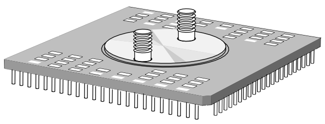
DECchip 21064A Alpha AXP Microprocessor Product Brief

October 1993



Description

Digital's DECchip 21064A microprocessor is a member of the 21064 family of microprocessors, which all implement Digital's Alpha AXP architecture. The DECchip 21064A microprocessor is a 0.5 micron CMOS based superscalar superpipelined processor using dual instruction issue and cycle times of either 233 or 275 MHz. The Alpha AXP architecture is a 64-bit RISC architecture designed with emphasis on speed, multiple instruction issue, multiple processors, and multiple operating systems.

Features

- 64-bit, fully pipelined, advanced RISC architecture supported by multiple operating systems
  - Microsoft Windows NT
  - OSF/1
  - OpenVMS
- Sustained leadership performance
  - 233 MHz and 275 MHz operation
  - Superscalar (dual issue)
  - Peak instruction execution rate of 466/550 million instructions/s (MIPS)
  - 0.5 µm CMOS technology
- Pipelined floating-point unit
  - IEEE single- and double-precision, VAX F_floating and G_floating, longword and quadword data types
  - Improved FP Divide
- Memory management
  - Demand-paged
  - 12-entry instruction-stream translation buffer (TB), eight entries map 8-KB pages, four entries for 4-MB pages
  - 32-entry data-stream TB, each entry map 8-KB, 64-KB, 512-KB, or 4-MB pages
- Main memory physically addressed up to 16G byte
- On-chip write buffer with four 32-byte entries
- Selectable data bus width
  - 64 or 128 bit
- Internal clock generator provides:
  - High-speed CPU clock
  - Pair of programmable system clocks (CPU/2 to CPU/17)
- External cache memory supports:
  - Programmable size (256K byte to 16M byte)
  - Programmable latency 3 to 16 CPU cycles
  - Flexible cache coherency
- Privileged architecture library code (PALcode) supports:
  - Optimization for multiple operating systems
  - Flexible memory management implementations
  - Multi-instruction atomic sequences
- Advanced packaging technology for superior thermal management performance
- On-chip 16-KB, direct-mapped, write-through data cache with parity
- On-chip 16-KB direct-mapped instruction cache with parity
  - Improved branch prediction logic
- Serial ROM (SROM) interface
  - Loads instruction cache after reset
  - Software-controlled serial port after initialization
- On-chip parity and ECC generators and checkers
- Chip- and module-level test support
- 3.3 V chip I/O supply voltage
  - Chip interfaces directly to 5 V logic
- Software compatible with DECchip 21064, DECchip 21066, and DECchip 21068
- Pin compatible with DECchip 21064

DECchip 21064A Microarchitecture

The DECchip 21064A microprocessor uses a 7-stage pipeline for integer operate and memory reference instructions, and a 10-stage pipeline for floating-point operate instructions. The instruction fetch and decode unit (Ibox) maintains state for all pipeline stages to track outstanding register writes.

Figure 1 shows the Block Diagram of the DECchip 21064A.

The DECchip 21064A CPU contains:

Instruction Cache (Icache)—The Icache contains 16 KB with parity protection. It is a direct-mapped, physically addressed cache with 32-byte blocks.

Instruction Fetch and Decode Unit (Ibox) —The Ibox includes the instruction translation buffers (ITBs) and the branch prediction logic (branch unit). The Ibox performs instruction fetch, resource checks, and dual instruction issue to the Ebox, Abox, FPU, or branch unit. The Ibox also controls pipeline bypasses, stalls, aborts, and restarts.

Integer Execution Unit (Ebox) —The Ebox contains a 64-bit fully pipelined integer execution data path including: adder, logic box, barrel shifter, byte extract and mask, and independent integer multiplier. The Ebox also contains the 32-entry 64-bit integer register file (IRF).

Floating-Point Unit (FPU) —The FPU contains a fully pipelined floating-point unit and independent divider. IEEE single-precision and double-precision floating-point data types are supported. VAX F_floating and G_ floating data types are fully supported, with limited support for the VAX D_floating data type. The FPU also contains a 32-entry 64-bit floating-point register file (FRF).

Load and Store Unit (Abox) —The Abox contains four major sections: address translation data path, which includes the data translation buffer (DTB); load silo; write buffer; and Dcache interface. The Abox supports all integer and floating-point load and store instructions, including address calculation and translation, and cache control logic.

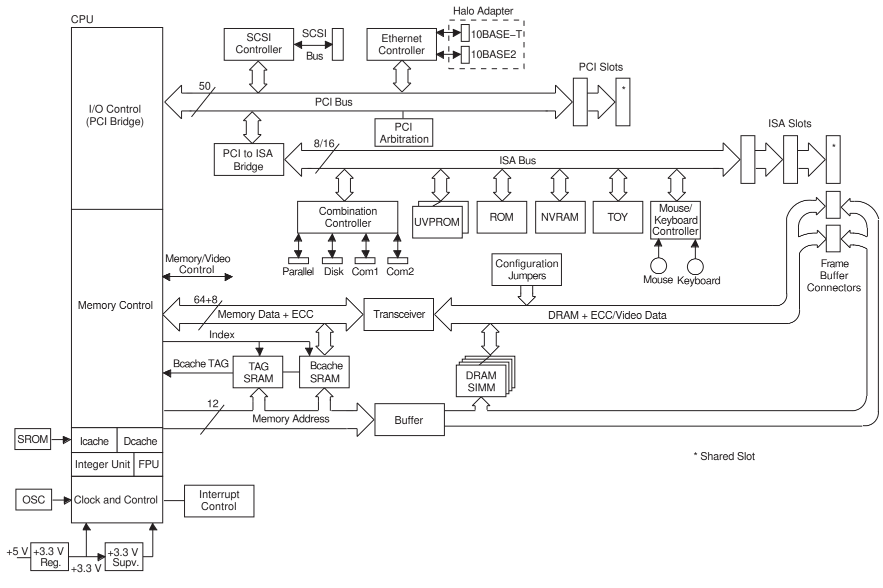
Data Cache (Dcache) —The Dcache contains 16 KB with parity protection. It is a write-through, read allocate, direct-mapped, physically addressed cache with 32-byte blocks.

External Cache —The DECchip 21064A supports an optional external flexible cache built from off-the-shelf SRAMs. The external cache is a write-back, read-allocate cache with 8-byte blocks. This allows each implementation to select its own external cache speed and configuration. The programmable interface supports cache sizes from 256 KB to 16 MB and latency of 3 to 16 CPU cycles.

Virtual Address Space —The virtual address is a 64-bit unsigned integer that specifies a byte location in the virtual address space. The microprocessor implements a 43-bit subset of the virtual address space and supports a 34-bit, 16-GB physical address space.

Serial ROM (SROM) Interface — This interface loads the instruction cache after reset. It has a software-controlled serial port, which is activated after initialization. The SROM supports system-level design debugging.

Figure 1 DECchip 21064A Block Diagram



Alpha AXP Architecture Summary

As implemented in the DECchip 21064A, Alpha AXP architecture supports:

- A fixed 32-bit instruction size
- Separate integer and floating-point registers
  - 32 64-bit integer registers
  - 32 64-bit floating-point registers
- 32-bit (longword) and 64-bit (quadword) integer data types
- 32-bit and 64-bit IEEE and VAX floating-point data types
- Memory accesses using a 64-bit virtual byte address
- Privileged architecture library code (PALcode)

Instruction Set

All instructions are 32 bits long and use one of four different instruction formats (see Figure 2). Each format uses a 6-bit opcode and 0, 1, 2, or 3 5-bit register fields.

CALL_PAL Instructions—These instructions vector to a privileged layer of software that atomically performs both privileged and unprivileged functions.

Branch Instructions—Conditional branch instructions test a register for positive/negative, zero/nonzero, or even/odd, and perform a PC-relative branch. Unconditional branch instructions perform either an absolute or PC-relative jump using an arbitrary 64-bit register value. They can update a destination register with a return value.

*Load and Store Instructio*ns—These instructions can move either 32-bit or 64-bit quantities. 8-bit and 16-bit load/store operations are supported through an extensive set of in-register byte manipulations. The I/O bus directly supports byte and word operations in hardware.

Operate Instructions —Integer operate instructions manipulate full 64-bit values and include a full complement of arithmetic, compare, logical, and shift instructions. There are also three 32-bit integer operations: add, subtract, and multiply.

In addition to conventional RISC operation, the instruction set provides: scaled add and subtract for quick subscript calculation; 128-bit multiply for multiprecision arithmetic and division by a constant; conditional moves for avoiding branches; and an extensive set of in-register byte manipulation instructions.

Floating-point operate instructions include four complete sets of instructions for IEEE single-precision, IEEE double-precision, VAX F_floating, and VAX G_floating arithmetic. In addition to arithmetic instructions, there are instructions for conversions between floating and integer values, including the VAX D_floating data type.

PALcode

PALcode is a privileged layer of software that automatically performs such functions as the dispatching and servicing of interrupts, exceptions, task switching, and additional privileged and unprivileged user instructions as specified by operating systems using the CALL_PAL instruction.

PALcode is the only method of performing some operations on the hardware. In addition to the instructions defined by the Alpha AXP architecture, a set of implementation-specific instructions is provided.

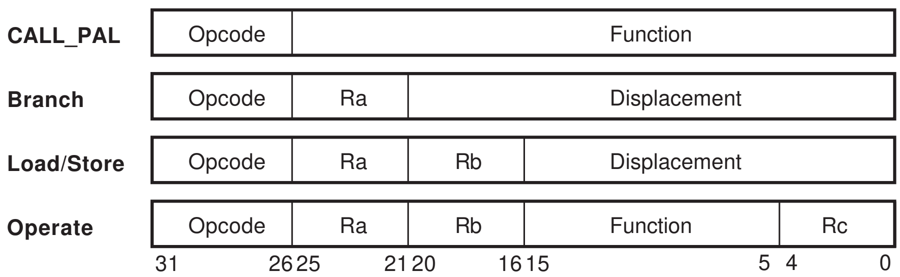
PALcode runs in an environment with privileges enabled, instruction stream mapping disabled, and interrupts disabled. Disabling memory mapping allows PALcode to support functions such as translation buffer miss routines. Disabling interrupts allows the instruction stream to provide multi-instruction sequences as atomic operations.

Memory Management

The memory management architecture provides:

- A large address space for instructions and data
- Convenient and efficient sharing of instructions and data
- Independent read and write access protection
- Flexibility through programmable PALcode support

Figure 2 Alpha AXP Instruction Formats



Adding the DECchip 21064A to Your Design Strategy

The DECchip 21064A reduces the overall cost of system development, provides for easier system design, and provides the benefits of high performance by bringing the Alpha AXP architecture to systems spanning the range from high-end desktop to enterprisewide servers.

By using the DECchip 21064A, your designs can benefit in the following ways:

Easy Migration of DECchip 21064 Module
DECchip 21064A is pin compatible with the existing family of DECchip 21064 products. This allows current DECchip 21064 customers to improve performance significantly, without the inherent costs associated with redesigning motherboards.

DECchip 21064A system clock frequency is a programmable divider of 2 to 17 of the CPU clock. A system using DECchip 21064-150 can plug in DECchip 21064A, increase the CPU clock frequency to 233 MHz or 275 MHz, and program the system clock frequency divider to keep the same system timing. This provides significant performance increase for no extra cost.

Module Flexibility for Performance Optimization
DECchip 21064A has a programmable external interface supporting a complete range of system sizes and performance levels, while maintaining peak CPU execution speed.

DECchip 21064A is capable of addressing 16G bytes of physical memory. The bus width is selected as either 64 bits or 128 bits to provide flexible module designs.

DECchip 21064A has the logic to support board-level cache including programmable cache size—256K byte to 16M byte, programmable latency—3 to 16 CPU clock cycles, and multiple cache coherency schemes. Cost versus performance trade-offs are made by selecting smaller to larger cache size, longer to shorter latency, and single versus symmetric multiprocessing.

Flexibility of Design
The DECchip 21064A interfaces directly to components operating at a supply voltage of either 3.3 V or 5 V. This means that you can use the standard components that best fit your applications and market demands.

ISO 9002 Certification
All of Digital's semiconductor manufacturing sites adhere to the stringent ISO 9002 standards, and are ISO 9002 certified.

Longevity of Design
All DECchip microprocessors are designed to the Alpha AXP architecture. So, whether your design requires the high performance of the DECchip 21064A, the price/performance of the DECchip 21066, or the low power of the DECchip 21068, your designs are assured of compatibility across this family of high-performance Alpha AXP microprocessors.

Technology Leadership
Designing with Digital's Alpha AXP microprocessors puts you in a place of leadership in the industry. Your products benefit from the unbounded capacity of 64-bit technology, the built-in longevity of the Alpha AXP architecture, and Digital's commitment to constant improvement in price/performance through the company's investment in semiconductor design and fabrication.

DECchip 21064A Characteristics

Power supply	Vss 0.0 V, Vdd 3.3 V ±5%
Operating temperature	Tj = 90°C
Storage temperature range	−55°C to 125°C
Power dissipation	233 MHz = 28 W 275 MHz = 33 W
Package	431 ceramic PBA with 0.10-in grid spacing and advanced thermal technology

If you want to order this 21064 family member...	Frequency	Then ask your Digital Sales representative for...
DECchip 21064–150	150 MHz	DECchip 21064–AA
DECchip 21064–166	166 MHz	DECchip 21064–CA
DECchip 21064–200	200 MHz	DECchip 21064–BA
DECchip 21064–233	233 MHz	DECchip 21064–BB
DECchip 21064–275	275 MHz	DECchip 21064–DB

For More Information

To learn more about availability of the DECchip 21064A microprocessor, contact your Digital sales representative. To learn more about Digital's semiconductors, contact the Semiconductor Information Line:

1-800-332-2717
1-800-332-2515 (TTY)

Outside North America, call:

+1-508-568-6868

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