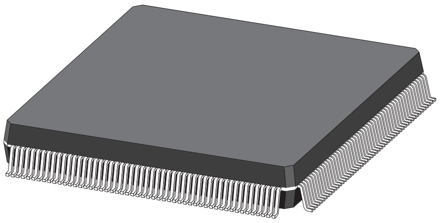
Digital Semiconductor

DECchip 21130
PCI Integrated Graphics and Video Accelerator

Product Brief

March 1995



Description

The DECchip 21130 is a 64-bit DRAM-based graphics and video accelerator for PCI local bus and Windows desktop systems. The 21130 integrates a 2D graphics accelerator, VGA controller, 24-bit RAMDAC, and phase-locked-loop (PLL) timing generator. A multimedia pipeline assists rendering PCI-sourced video data streams by scaling, filtering, and converting to the color space used by the RAMDAC.

Features

- Highly integrated, high-performance, Windows acceleration
  - 64-bit 2D graphics accelerator
  - VGA controller
  - 256-color look-up tables
  - 24-bit true-color DAC
  - PLL timing generator
  - 64 × 64 × 2 hardware cursor control
- Multimedia pipeline for real-time video display acceleration
  - YUV-to-RGB index color space conversion
  - Image scaling to arbitrary integral sizes
  - VESA advanced feature connector (VAFC) input or output channel
- AccuVideo imaging technology
  - Digital's patented imaging technology
  - Converts 24-bpp to 8- or 16-bpp
  - Converts 16-bpp to 8-bpp
- Fully compliant with *PCI Local Bus Specification, Revision 2.0*
  - One PCI-load graphics subsystem
  - Onchip glueless PCI interface
- 32- or 64-bit DRAM display memory controller
  - 1, 2, or 4MB frame buffer
  - Extended data out (EDO, hyperpage mode)
  - Linear frame-buffer addressing
- Separate access to external BIOS ROM
- Supports VESA standards for:
  - 75 Hz noninterlaced resolutions:
    1280 × 1024 8-bpp
    1024 × 768 8- and 16-bpp
    800 × 600 8-, 16-, and 24-bpp
    640 × 480 8-, 16-, and 24-bpp
  - Display power-management signaling (DPMS) for EPA Energy Star (Green PC) requirements
  - Display data channel (DDC) for monitor identification
- Generic peripheral port for simple connection to one other 8-bit device
- 208-pin PQFP
- An evaluation board (EB130) is available for module test and development

Software Features

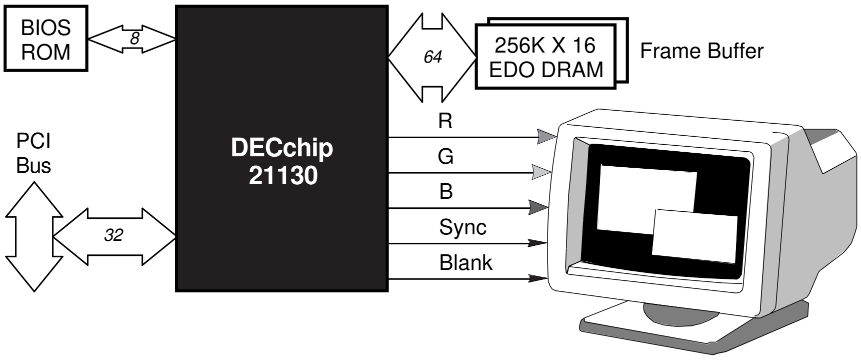
- Software driver support
  - Windows 3.1
  - Windows 95
  - Windows NT 3.5
  - AutoCAD
  - OS/2 2.1
- Supports industry-standard video CODEC formats:
  - MPEG-1
  - Motion JPEG
  - Px64 (H.261)
  - Indeo
  - Cinepak
  - Video 1
- Supports Microsoft DCI for video acceleration (Video for Windows)
- Video BIOS for x86 architecture

1MB Entry-Level to 4MB High-Performance Graphics System

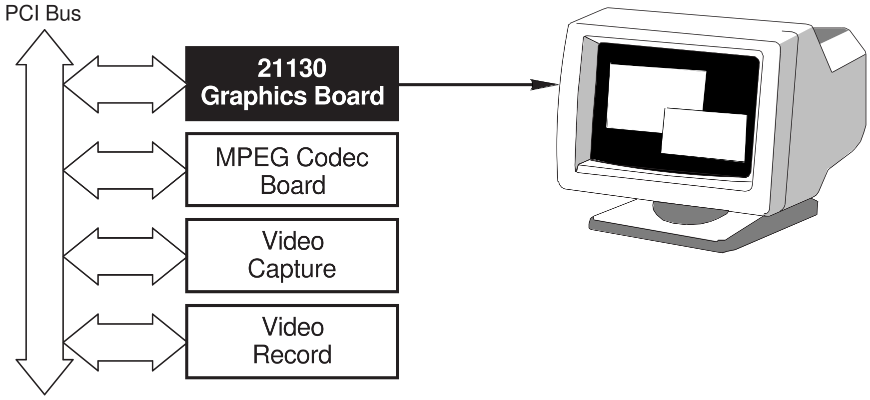
The only VLSI components needed to build a 21130 module for an entry-level multimedia system are the 21130, two 256K × 16 EDO DRAMs, and a 256K × 8 BIOS ROM. The 21130 also requires a 14.31818-MHz crystal to internally synthesize the high-speed memory and pixel clocks. Improved graphics performance, better screen resolutions, and greater color depths are easily possible by increasing frame buffer memory size to 2 or 4MB simply by using four or eight DRAMs; additional external logic is not required.

The 21130 also accepts decompressed YUV 4:2:2 digital video from the PCI local bus, and it scales, filters, and dithers the YUV video stream through AccuVideo. The onchip color space converter then converts the YUV video to RGB indexes for frame buffer storage and computer monitor display.

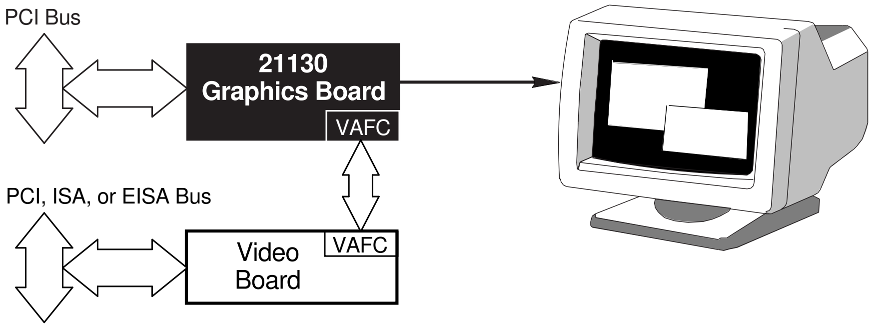
Entry-Level System



PCI Multimedia System



Multimedia System with VAFC Support



Architecture

The 21130 defines a new industry standard for delivering graphics and video in a Windows desktop system. The highly integrated architecture simplifies the merger of graphics and video windows without redundant components and unnecessary connectors.

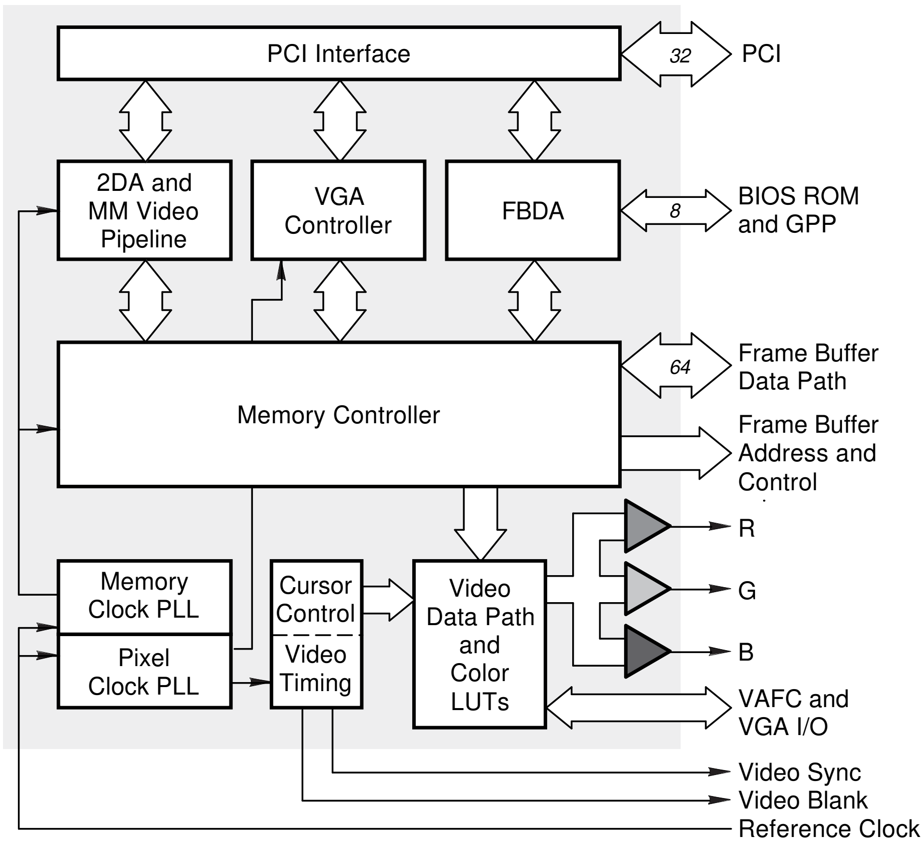
PCI Interface

The PCI interface supports PCI master and target transactions and DMA read capability. It includes the PCI registers and separate access to the BIOS ROM. Command and data FIFOs optimize the bandwidth performance between the PCI and the graphics and multimedia engines.

VGA Controller

The VGA controller supports standard VGA modes through 13_{16} and a subset of SVGA modes. It includes the standard and extended VGA registers and provides a PCI-to-ISA VGA interface. The video timing function is part of the VGA controller.

DECchip 21130 Block Diagram



2DA and MM Video Pipeline

The 2D graphics accelerator (2DA) and multimedia (MM) video pipeline performs line drawing, color expansion, BitBlt, host-to-screen stretchBlt, and text operations in support of the higher-resolution VESA-standard modes. It also operates on YUV 4:2:2 video from the PCI bus, providing real-time filter, scale, dither, and YUV-to-RGB index conversion for video display in a window or full-screen video display. It includes the command FIFO, DMA read FIFO, copy buffer, and graphics registers.

The 64-Dword command FIFO accepts PCI burst writes to prevent bus stalls while graphics operations complete. The 64-Dword DMA read FIFO provides a similar capability for large data transfers from host memory to the frame buffer. The copy buffer is a 64-byte FIFO that allows frame buffer burst reads and writes at the full bandwidth of the EDO DRAMs.

FBDA

The frame buffer and device access (FBDA) function provides asynchronous access to the BIOS ROM (optionally an EEPROM for flash updates) and additional external devices as well as direct frame buffer access. The generic peripheral port (GPP) is included in this function. The GPP provides access to one 8-bit device such as video processing circuits, audio chips, or I^2C controllers. The 8-bit GPP is multiplexed on the DRAM data path.

Memory Controller

The memory controller provides a 32-bit or 64-bit data path to the frame buffer DRAMs. It includes a pixel merge function that merges concurrent writes to different bytes in the same 64-bit location, and a write buffer that optimizes the use of the frame buffer bandwidth between drawing and refresh operations.
The VAFC port shares the upper 32-bits of the frame buffer data path. When the VAFC port is active, the memory controller is in 32-bit frame buffer mode, and the upper half of the data path is available for full-time video I/O.

Video Data Path and Color LUTs

The video data path includes two 256-color LUTs feeding a 24-bit DAC. The graphics color palette is in a RAM LUT and the video color palette is in a ROM LUT. Allocating a 256-color LUT to video allows simultaneous, nonshared full-color graphics.

Video Timing and Cursor Control

The cursor control function supports a 3-color, Windows or XGA, or X-windows cursor.

Memory and Pixel Clock PLLs

Both PLLs are normally driven by the same 14.3181-MHz reference clock. The memory clock PLL provides the 66-MHz (nominal) memory clock and half-speed core clock. The pixel clock PLL also provides the pixel clock and VGA dot clock and is programmable over a range of frequencies from 8 to 135 MHz.

VAFC

External video is input through the VAFC to the video data path for display on the monitor. Scaled video is output through the VAFC to an NTSC/PAL encoder for video monitor display or VCR storage. The VAFC port shares the upper 32 pins on the frame buffer data path.

Applications

The 21130 provides leadership in desktop multimedia system performance for applications such as:

- Multimedia authoring
- Multimedia presentations
- Desktop publishing
- CD-ROM video playback
- Office productivity suites
- Video teleconferencing
- Image processing

Supported High-Resolution VESA Display Modes

	8–bpp	16–bpp	24–bpp*	24–bpp
640 X 480	31.50 *101*	63.00 *111*	94.50 *112*	126.00 *112*
800 X 600	49.50 *103*	99.00 *114*	148.50 *115*	198.00 *115*
1024 X 768	78.75 *104*	157.50 *117*		
1280 X 1024	135.00 *107*			

*Packed pixels, not accelerated

Legend:

31.50	Peak memory bandwidth (MB/s)
101	VESA Int10 mode (hexadecimal)

(unshaded)	1 MB frame buffer
(shaded)	2 MB frame buffer

The peak memory bandwidth is the product of the pixel rate and pixel depth.

The PCI Advantage

By integrating the PCI interface, the 21130 graphics and video accelerator enables systems designers to build multimedia and graphics subsystems for a wide variety of platforms and applications with little or no glue logic.

In addition to the 21130, Digital Semiconductor offers the following PCI peripheral components:

- DECchip 21030 PCI 3D Graphics Accelerator
- DECchip 21041 PCI Ethernet LAN Controller
- DECchip 21140 PCI Fast Ethernet LAN Controller
- DECchip 21050 PCI-to-PCI Bridge

Peak Hardware Performance

Operation (Mpixels/s)	**8-bpp**	**16-bpp**	**32-bpp**
Copy: Screen-to-screen	92	46	23
Copy: Host-to-screen	102	50	23
Fill	185	92	46
Lines 10-pixel, random orientation	TBD	TBD	TBD

Characteristics

Characteristic	**Specification**
Power supply	5.0 V ±5%
Operating temperature	T_j = 55°C maximum
Storage temperature range	–55 to +125°C
Power dissipation @ Vdd = 5.0 V Frequency = 33 MHz	3.5 W maximum
Package	208-pin PQFP

For More Information

To learn more about the availability of the DECchip 21130 PCI Integrated Graphics and Video Accelerator, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

1-800-332-2717
1-800-332-2515 (TTY)

Outside North America, call:

+1-508-568-6868

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